A 5 GHz LOW POWER, LOW JITTER AND FAST SETTLING PHASE LOCKED LOOP ARCHITECUTRE FOR WIRELINE AND WIRELESS TRANSCEIVER

By

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To the Faculty of Washington State University:

The members of the Committee appointed to examine the thesis of PARAG UPADHYAYA find it satisfactory and recommend that it be accepted.

_____
Chair

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A 5 GHz LOW POWER, LOW JITTER AND FAST SETTLING PHASE LOCKED LOOP ARCHITECUTRE FOR WIRELINE AND WIRELESS TRANSCEIVER

ABSTRACT

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While significant research has already been poured into signal generation via the phase locked loop (PLL) and circuit methods to improve the PLL phase noise, constant desire for further improvement and higher data bandwidth demands more rigorous and novel improvements . In both wireline and wireless communication, the data bandwidth is heavily dependent on the quality of the PLL; however, PLLs come with their own unique set of challenges. They inherently take a long time to lock and require a very low phase noise voltage controlled oscillator (VCO) performance in a potentially noisy environment. They consume significant DC power, demand large silicon die area and force many trade-offs between key performance parameters. This intricacy puts wireless and wireline applications in an unenviable position, as they are strictly driven by highly integrated low power, low cost and high performance operations. Low-power constraints demand PLLs to be turned off during inactivity, but then require it to acquire lock swiftly when turned back on. Therefore, investigation of low cost, low power and high quality novel fast locking PLLs are driven by the insatiable demand of state-of-the-art wideband applications.

This dissertation presents a low power PLL architecture with adaptive bandwidth control to enable fast settling and lock time, a novel load independent switched LC VCO, a low spur and glitch compensated dynamic replica-based current steering charge pump and an optimized very low power frequency divider to achieve sub-*ps* jitter performance in a 0.18-µm process CMOS technology. Consuming 11mW of total power from 1.5V supply, the PLL achieves sub-*µs* settling time, worst case reference spurs below 64 dB with worst case integrated RMS jitter of less than 2 *ps* and deterministic jitter of less than 7 *ps* in a noisy packaged environment. The PLL phase noise is lower than –120 dBc/Hz, at 1 MHz frequency offset from the carrier, over the tuning range. The PLL is designed with nominal loop bandwidth of 1 MHz.

This dissertation consists of theoretical details of several novel VCO designs, novel glitch compensated charge-pump architecture and novel adaptive bandwidth mechanism for the PLL. The dissertation includes culmination of works from published or to be published peer review journal and conferences.

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Dedication

This thesis is dedicated to my parents

who dared to dream big for their kids

and

to my wife and newly born twin daughters

LIST OF ABBREVIATIONS

BER	Bit Error Rate
BPF	Band Pass Filter
BW	Bandwidth
CDR	Clock and Data Recovery
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CP	Charge Pump
DCR	Direct Conversion Receiver
DCT	Direct Conversion Transceiver
DIV	Frequency Divider
DJ	Deterministic Jitter
DSB	Double-Sideband
EVM	Error Vector Magnitude
F	Noise Factor
f_T	Unity Gain Frequency
FET	Field Effect Transistor
FOM	Figure of Merit
FM	Frequency Modulation
Gbps	Gigabits per Second
g_m	FET Transconductance
IF	Intermediate Frequency
JT	Peak to Peak Receive Jitter Tolerance Range
IIP_2	Second order Input Intercept Point
IIP_3	Third order Input Intercept Point
IMD_2	Second order Intermodulation Product
IMD_3	Third order Intermodulation Product
IP	Intercept Point
P_{1dB}	Input 1dB Compression Point
PD	Phase Detector
PDF	Probability Density Function
PFD	Phase Frequency Detector
PLL	Phased Locked Loop
PN	Phase Noise
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MOS	Metal Oxide Semiconductor
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing
OIP_2	Second order Output Intercept Point
OIP_3	Third order Output Intercept Point
OOK	On Off Shift Keying

PA	Power Amplifier
PDF	Probability Density Function
PLL	Phase Lock Loop
PM	Phase Modulation
PN	Phase Noise
PSD	Phase Spectral Density
PSRR	Power Supply Rejection Ratio
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RJ	Random Jitter
RMS	Root Mean Square
RPS	Resonant Phase Shift
RX	Receive
SER	SERDES (Serializer and Deserializer)
SNR	Signal to Noise Ratio
SSB	Single-Sideband
Sigma	Standard Deviation
TL	Transmission Line
TR	Transmit/Receive
TX	Transmit
U-NII	Unlicensed National Information Infrastructure
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator
WiMax	Worldwide Interoperability for Microwave Access

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1. P. Upadhyaya, M. Rajashekharaiah, D. Heo, Y. E. Chen, "A New 5-GHz ISM Band CMOS Doubly Balanced Sub-Harmonic Mixer for Direct Conversion Receiver," *Proceeding, IEEE European Conference on Wireless Technology*, pp. 65-68, October 2004.

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CHAPTER ONE

1.0. INTRODUCTION

Wireless and wireline communication technologies are at the forefront of human innovation enabling the current and future development in health care, social interaction, and all areas of our IT-infused society. Wireless communication including mobile TV, mobile internet, remote sensing and wireless telemetry are fast growing areas to feed our insatiable demand for information at a push of a button. Wireline technologies have always has set standards for speedy communication and have allowed fast information exchange at high data rate for internet and data transfer. Together these market areas have grown exponentially in recent years and are expected to grow at similar rates into the very distant future. The unquenchable desire for higher bandwidth and data rates have challenged the hardware industry, which forms the backbone of both wireline and wireless communication, to develop faster and innovative low cost integrated chip solutions to help foster this growth. In the fast growing wireless industry 54 Mbps data rates are already achieved and are driven further via IEEE 802.11a, UWB (Ultra Wide Band), and Wimax industry standards utilizing 2 to 10 GHz frequency bands. In wireline industry, the developments driven by integrated circuits have already achieved 10 Gbps and 40 Gbps data rates and are now in developmental phase for even higher communication data rates. The low cost integrated circuit solutions for these markets are therefore significant engine for future growth and the one that requires constant innovations.

The data bandwidth or speed is a high volume term commonly used in communication industry. Everyone wants it but what are the limitations? Is it physical in nature and is it something that can be tackled to achieve even higher data rates. In essence there exists two

limitations, one is sheer speed, which is governed by unity gain frequency, f_T, of the technology in use, and the other is noise, which can be both intrinsic and extrinsic in nature.

For wireline transceiver shown in Figure 1-1, the noise, degrades the signal to noise ratio (SNR) which can directly be measured in terms of bit error rate (BER) a mechanism that limits the data bandwidth for high quality communication. The noise is measured as timing jitter which can be deterministic (DJ) in nature or random (RJ) [1]. The DJ is deterministic, in principle, because you can accurately predict the jitter of each signal edge if you know enough about the system and it's probability density function (PDF), which gives probability for a given logic transition to deviate from ideal by certain amount, is bounded. Since the PDF is bounded, the DJ can be measured as a peak-to-peak value from eye diagram as shown in Figure 1-2. The RJ's PDF, in another hand, is unbounded and is described by Gaussian distribution and its' standard deviation, σ , as shown in Figure 1-2. The RJ is caused by culmination of large number of random process with small magnitudes such as device thermal noise, shot noise and flicker noise.

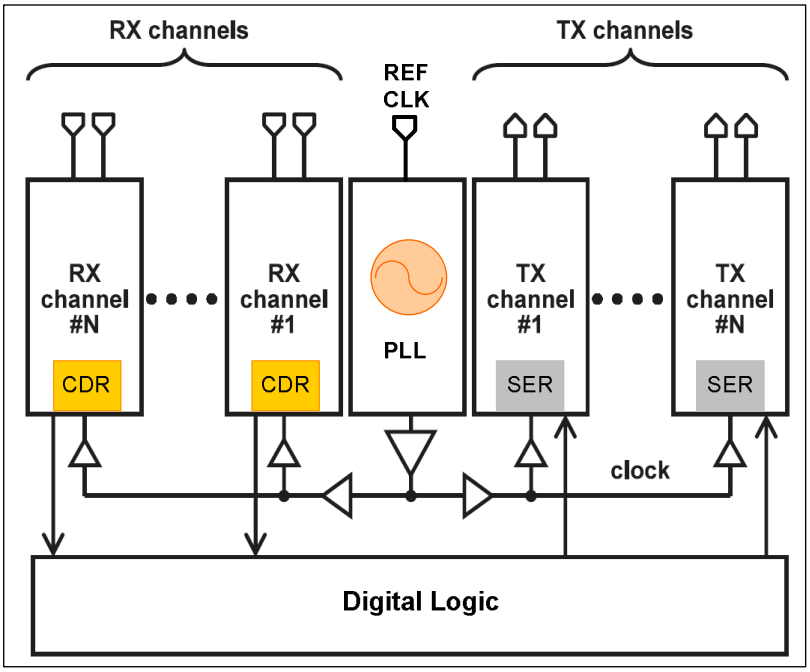


Figure 1-1. Block diagram of *N*-Channel wireline transceiver

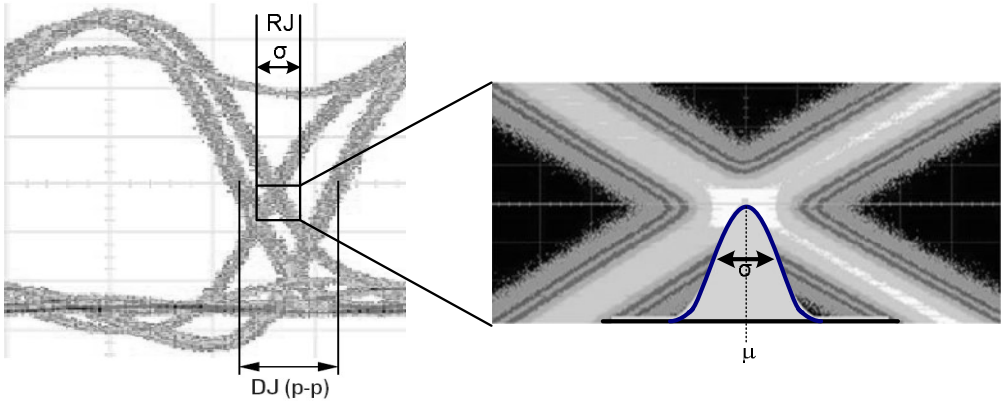


Figure 1-2. Deterministic (DJ) and random jitter (RJ) characteristics

In transceiver application, the PLL, a key component, is the primary source of RJ and is dominated by its phase noise (PN). Figure 1-3 shows the phase spectral density (PSD) of a signal source from which RJ can be calculated. $S_\varphi(f_\varphi)$ is the square of the average phase deviation per unit of frequency offset from signal carrier, $f_\varphi = f - f_c$ [2]. Integrating it over desired bandwidth and taking square root yields the standard deviation, σ, of the RJ Gaussian distribution as in (1.1).

$$\sigma = \sqrt{\int_{f_1}^{f_2} s_\varphi(f)\, df} \approx \sqrt{\int_{f_1}^{f_2} 2L(f)\, df} \qquad (1.1)$$

The *L(f),* is the single side band (SSB) noise spectrum or the SSB phase noise spectrum which is related to $S_\varphi(f_\varphi)$ by,

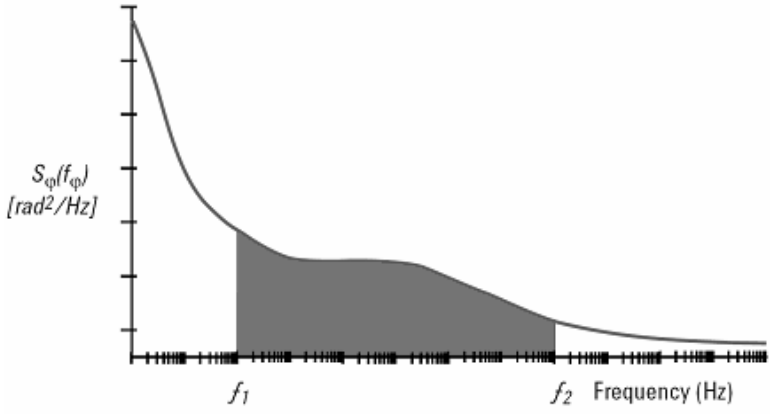


Figure 1-3. Phase noise integrated over bandwidth (f_2–f_1) yields RJ

$$L(f)\left[dBc/Hz\right] \approx \frac{\Delta\varphi_{rms}^2}{2\Delta f_\varphi} \approx 1/2\, S_\varphi(f_\varphi)\left[rad^2/Hz\right] \tag{1.2}$$

The relationship between jitter and BER is quite complicated but a simplified model for the wireline transceiver can be used to approximate it as,

$$BER = 2Q\left(\frac{T}{2\sqrt{\sigma^2}}\right) \tag{1.3}$$

where, T, is unit interval and Q function is defined as,

$$Q(x) = \left(\frac{1}{\left(1-1/\pi\right)x + 1/\pi\sqrt{x^2+2\pi}}\right) \bullet \frac{1}{\sqrt{2\pi}} e^{-\frac{x^2}{2}} \tag{1.4}$$

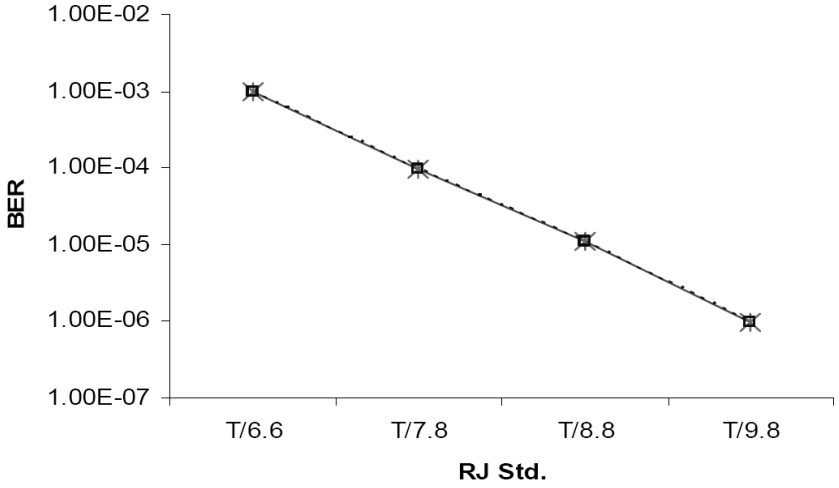


Figure 1-4. BER as a function of RJ [σ = *T/x*] [3]

Figure 1-4 shows BER as a function of RJ. Eq (1.3) and Figure 1-4 suggest that to achieve lower BER, lower RJ is required. To lower RJ, one must lower the phase noise of the signal source as evident from (1.1) and (1.2).

In wireless transceiver as shown in Figure 1-5, the RJ or the phase noise of the PLL also affects the BER. The PLL generated local oscillator (LO) is used for down-conversion of RF signal via the mixer. The presence of phase noise in the LO spreads the carrier noise. When the receiver is tuned to a frequency near the strong carrier, the power density in the carrier sidebands

may exceed the noise floor of the receiver, and thus, degrades the SNR [4]. Even if the noise floor is not exceeded, the receiver sensitivity is limited by reciprocal mixing, where the weak carrier is nearly masked by the phase noise of the LO at the intermediate frequency (IF) as shown in Figure 1-6. The degraded SNR lowers the BER for the wireless transceiver and its' the data bandwidth.

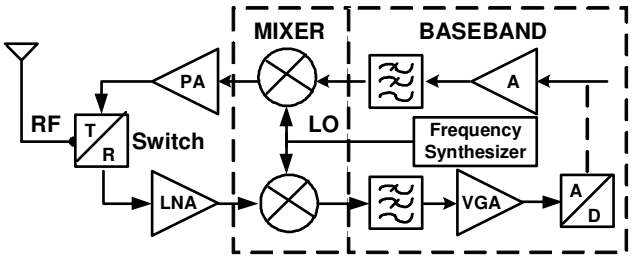


Figure 1-5. Block diagram direct conversion wireless transceiver

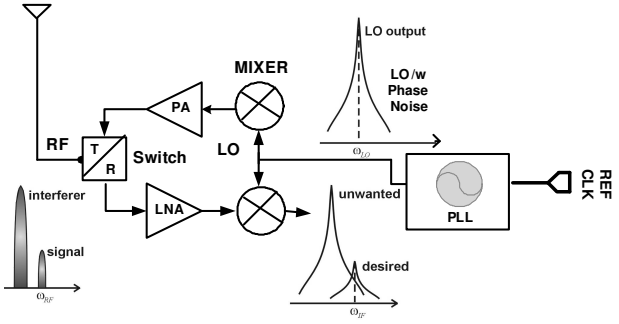


Figure 1-6. Reciprocal mixing and degradation of SNR in wireless transceiver

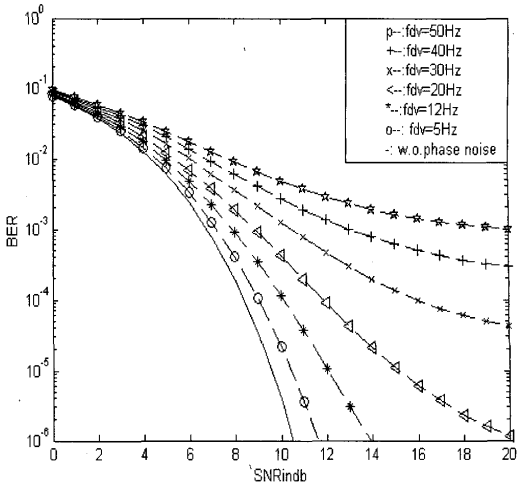


Figure 1-7. BER vs. SNR for different frequency deviation due to phase noise on LO [5].

Figure 1-7 shows the plot of BER vs. SNR for different frequency deviation due to LO phase noise in OFDM communication system employing QPSK and 16 QAM modulations. The BER for the wireless receiver degrades with higher LO phase noise which yields higher frequency deviation [5].

Now that we have established the links between noise in PLL and BER, it is the objective of this thesis to advance the state-of-the-art in phase noise of the PLL to enable low BER wireline and wireless transceiver to further improve the data rate. Figure 1-8 shows the block diagram of a typical integer-*N* PLL.

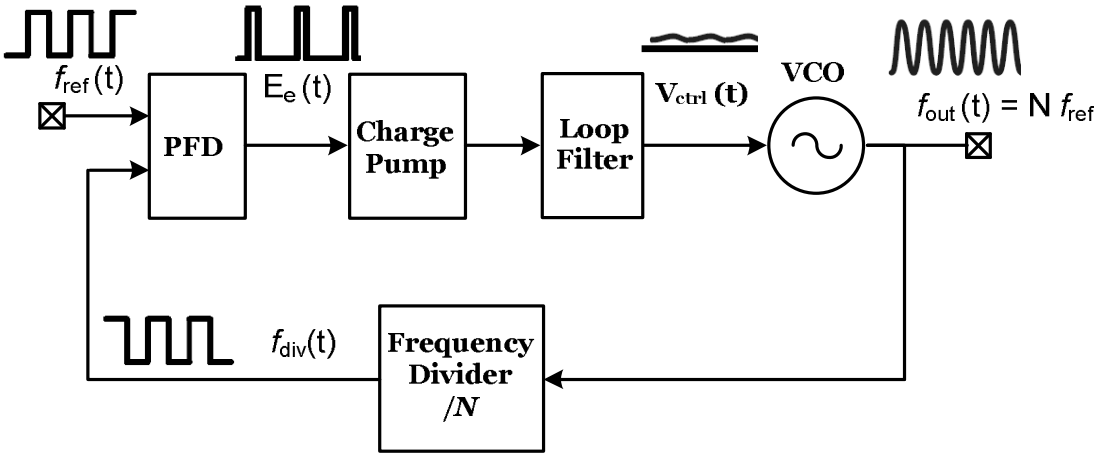


Figure 1-8. Block diagram typical phase locked loop

The PLL consists of a phase frequency detector (PFD) that compares the phase and frequency error between reference clock and feedback divider clock, a charge-pump (CP) which adds and subtracts charge depending on magnitude of phase and frequency error from the PFD, a loop filter that integrates the charge from CP into a control voltage that tunes a VCO and a frequency divider that divides the VCO output frequency such that the divided frequency is near or at reference frequency band. A PLL can be thought of as a reference frequency multiplier with output in phase or phase locked with the reference input.

1.2. Thesis Objective

The primary objective is the investigation of a novel low power adaptive fast settling phase locked loop architecture with novel low phase noise LC VCO, low static offset and low glitch dynamic charge pump and very low power divider to achieve sub-ps jitter performance in a 0.18-µm process CMOS technology. The phase noise of the VCO and charge pump/loop filter contributes to RJ in the PLL and limit the BER for both wireline and wireless transceiver. Therefore, significant part of this thesis work will examine several VCO architectures to achieve low phase noise. The thesis will also investigate low spur and low glitch charge pump architecture to suppress reference spurs. Low power fast locking and fast settling adaptive bandwidth mechanism will be investigated to result in state-of-the-art low power PLL architecture. The outcome of this work includes innovative high performance IPs and design methodologies relevant to wireline and wireless communication applications. The research presented in this thesis is inline with current trends for PLLs, specially for battery powered application, including

I. New architecture with high level of integration

II. Low voltage and very low power design at higher carrier frequencies

III. Fast settling/locking with quick wake-up time

IV. Novel low phase noise VCOs for low jitter performance

V. High spur suppression

VI. Very low power high speed frequency dividers

1.3. Thesis Organization

The thesis is organized into 7 chapters. Chapter 2 will discuss PLL dynamics and noise for low jitter fast locking/settling PLL architecture. Chapter 3 will discuss choice for phase

frequency detector while Chapter 4 will discuss low spur glitch compensated replica bias charge pump architecture. Chapter 5 will examine several VCO IPs that achieve low phase noise performance with high FOM factor. Chapter 6 presents the proposed low power, fast settling and low jitter PLL architecture including details of divider with simulation and measured performance results. Chapter 7 will comprise of future research improvements and possibilities.

CHAPTER TWO

2.0. Phased Locked Loop Dynamics and Noise Consideration for Low Jitter Signal Generation

To push the performance limits of PLL, especially in relation to jitter, it is important and imperative to understand the governing fundamentals and dynamics. Significant research already exists in literature to cover PLL fundamentals; therefore, in this chapter we will directly delve into important concepts for low jitter and low noise design.

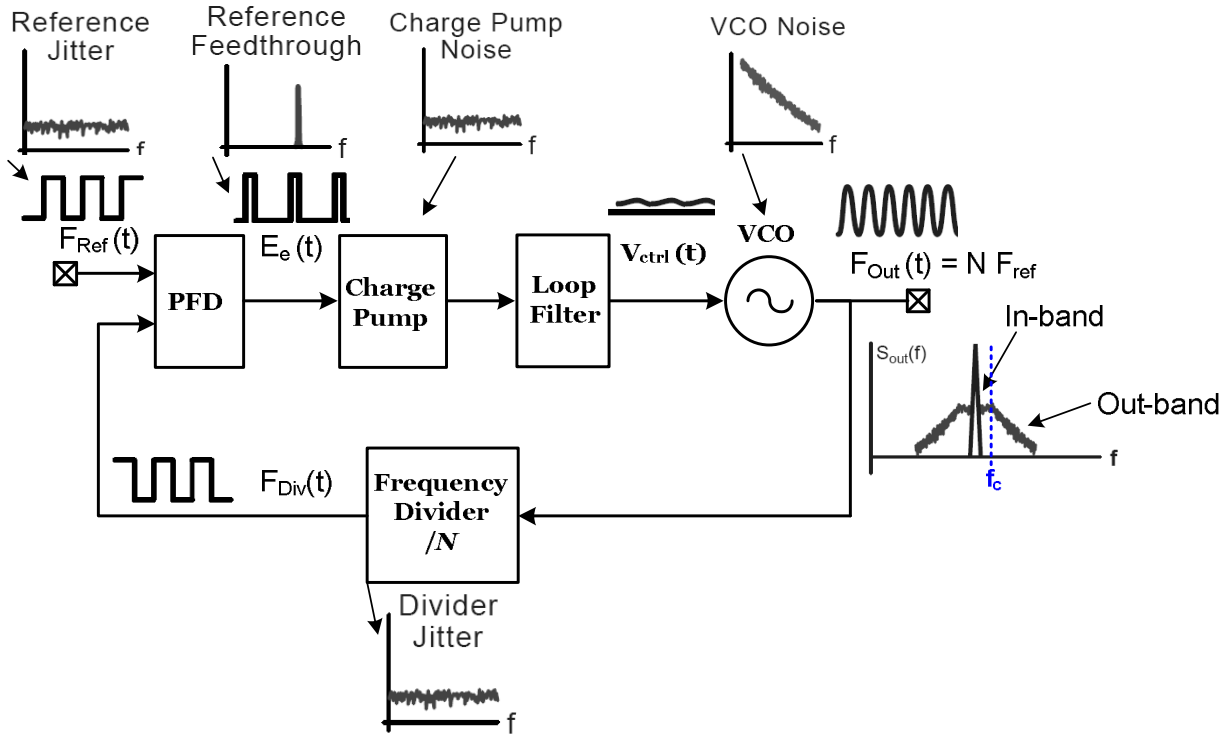


Figure 2-1. Noise in Integer-N PLL

Figure 2-1 shows the typical noise spectrum [6] in frequency domain of each component and the resultant output carrier signal with phase noise. In time domain, the noise from the PLL, with main contribution from random jitter (RJ) is measured as timing jitter. If the PLL is un-locked or jitter is allowed to accumulate without reset, the jitter in unbounded and the standard deviation increases as shown in Figure 2-2. In short term, the jitter is proportional to the square

root of the time, $\sigma_t \propto \sqrt{t}$. In the long term, the jitter varies linearly with time, $\sigma_t \propto t$. When the PLL is locked the jitter or the standard deviation levels out beyond the loop time as shown in Figure 2-3 [4]. Significance of this is that the PLL is a filter and with proper choice of loop bandwidth, one can control the noise level and thus the timing jitter.

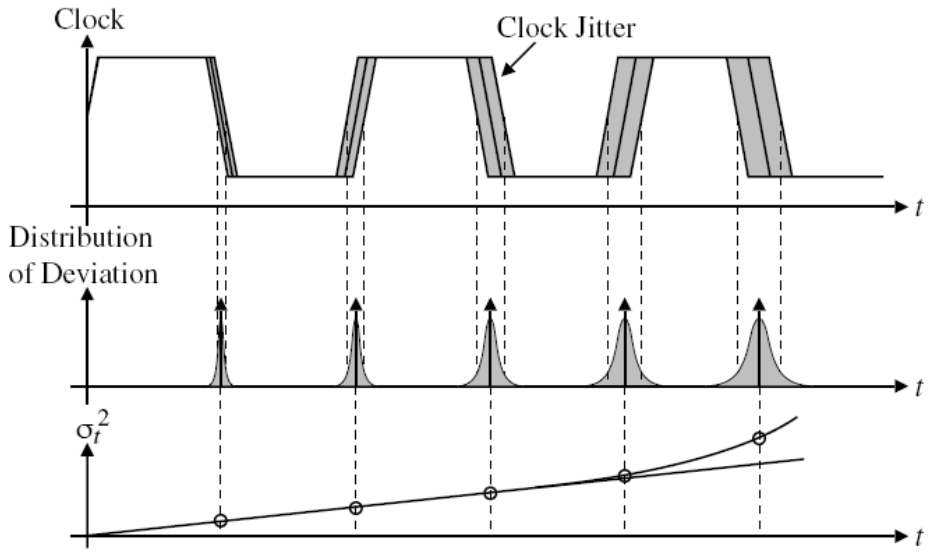


Figure 2-2. Time domain jitter with free running VCO or PLL with jitter accumulation [4]

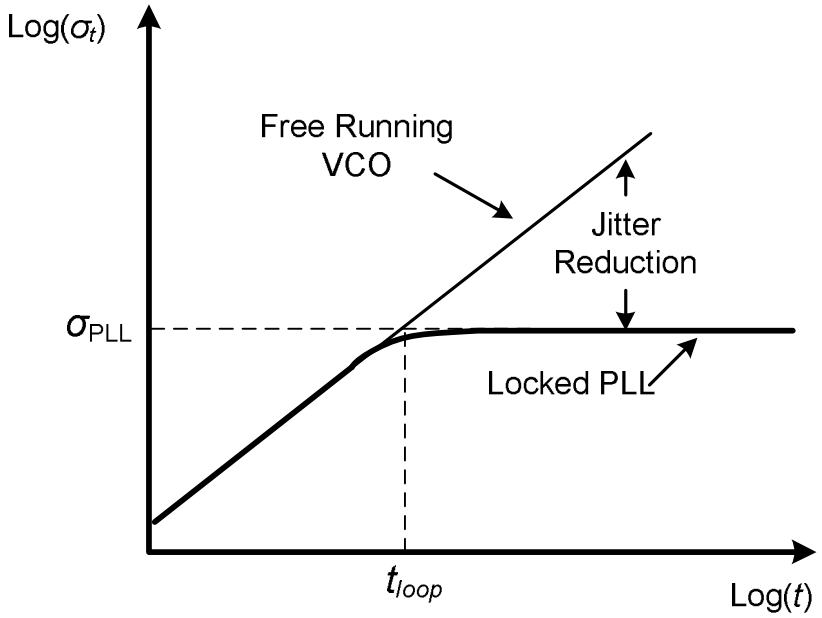


Figure 2-3. Time domain jitter with phase locked PLL vs. free running VCO.

2.1. PLL Noise Transfer Function and Design for Low Noise

The PLL is a closed loop control system, and thus, we can develop a linear mathematical model to better understand signal and noise loop dynamics. Let us represent a PLL in Figure 2-1 by its linear Laplace model in Figure 2-4.

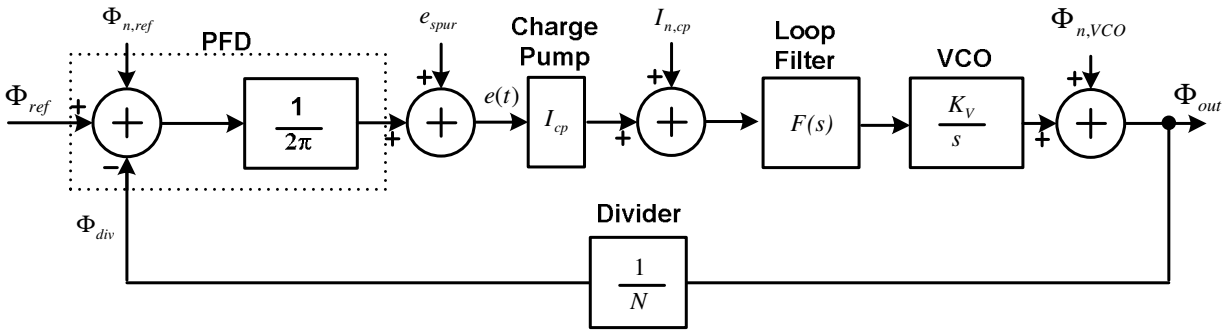


Figure 2-4. Linear model for the PLL with noise

where,

$\Phi_{n,ref}$ is the noise from the PFD

e_{spur} is the noise due to reference spur

$I_{n,cp}$ is the noise from the charge-pump

$\Phi_{n,VCO}$ is the noise from the VCO

Φ_{ref} is the reference signal

Φ_{div} is the VCO divided signal

$e(t)$ is the output phase error signal between reference and divider input from PFD

I_{cp} is the charge-pump current

$F(s)$ is loop filter transfer function

K_V is the VCO gain

Φ_{out} is the PLL output, N is the divide ratio and $s = j\omega$.

Keeping track of all noise transfer function from each noise source is possible but we can simplify the PLL model further by referring all noise except for $\Phi_{n,VCO}$ to PFD output to get Figure 2-5.

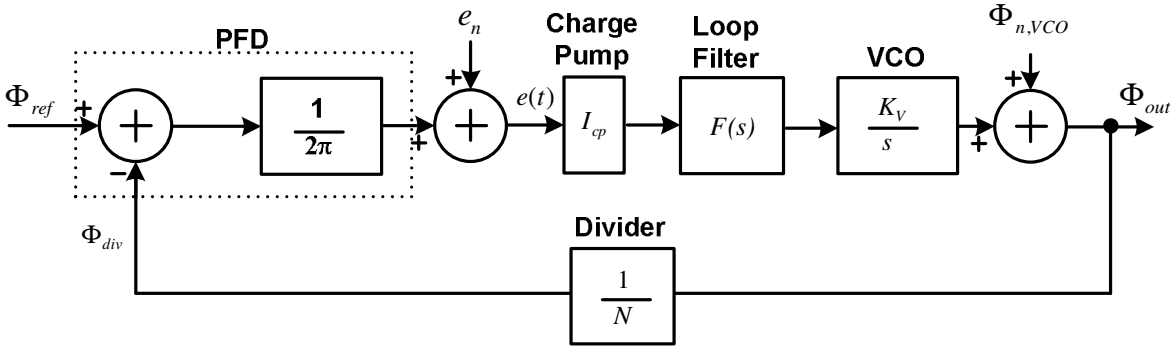


Figure 2-5. Simple PLL model with all noise referred to the PFD output except for the VCO noise

The PFD output referred noise, e_n, includes noise source from the divider, the PFD, the reference spur and the charge-pump. Now the transfer function from PFD output referred noise to the PLL output can be derived using black's formula,

$$\frac{\Phi_{out}(s)}{e_n(s)} = \frac{I_{cp}F(s)\,K_V/s}{1 + 1/2\pi\, I_{cp}\, 1/N\, F(s)\,K_V/s} \tag{2.1}$$

Similarly, noise from VCO-referred noise can be written as,

$$\frac{\Phi_{out}(s)}{\Phi_{n,VCO}(s)} = \frac{1}{1 + 1/2\pi\, I_{cp}\, 1/N\, F(s)\,K_V/s} \tag{2.2}$$

Let's simplify (2.1) and (2.2) by defining open loop transfer function, *A(f),* and the closed loop transfer function, *G(f),* for the PLL as,

$$A(s) = 1/2\pi\, I_{cp}\, 1/N\, F(s)\,K_V/s \tag{2.3}$$

$$G(s) = \frac{A(f)}{1 + A(f)} \tag{2.4}$$

and write (2.1) and (2,2) as,

$$\frac{\Phi_{out}(s)}{e_n(s)} = 2\pi NG(s) \tag{2.5}$$

$$\frac{\Phi_{out}(s)}{\Phi_{n,VCO}(s)} = 1 - G(s) \tag{2.6}$$

G(s) is a low pass response with DC gain, and therefore, the PFD referred noise source, $\frac{\Phi_{out}(s)}{e_n(s)}$, is low-pass filtered by the PLL, given *F(s)* is a low pass filter transfer function. Similarly, the VCO referred noise, $\frac{\Phi_{out}(s)}{\Phi_{n,VCO}(s)}$ is high-pass filtered. Both responses for the PLL have same transition frequency values defined by the PLL bandwidth (f_c). The total PLL noise transfer function, therefore, can be thought of as a band-pass response since the PLL combines a low-pass filtering and high-pass filtering effects as shown in Figure 2-6. Below the PLL bandwidth (f_c), the in-band noise is dominated by the PFD referred noise while the out-of-band or out-band noise is VCO dominated, assuming the reference signal phase noise is better than the VCO phase noise. *A very low noise PLL can be achieved with proper choice of loop bandwidth based on determination of dominant noise region, in-band or out-band noise*. If the PFD referred noise is higher than the VCO noise then narrow bandwidth is preferred and visa-versa.

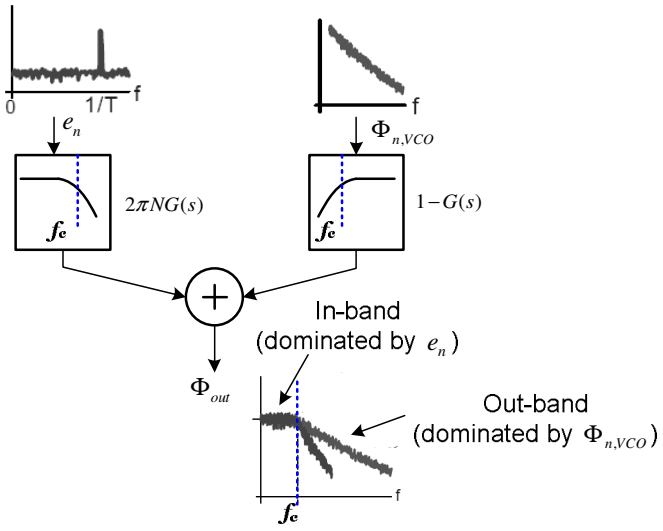


Figure 2-6. PLL output noise spectrum contribution from the PFD referred noise and the VCO noise

Eq. (2.7) infers the impact of charge-pump noise to overall PLL output noise from PFD referred noise.

$$\frac{\Phi_{out}(s)}{I_{n,cp}} = \left(\frac{1}{I_{cp}}\right)\frac{\Phi_{out}(s)}{e_n} = \frac{2\pi NG(s)}{I_{cp}} \tag{2.7}$$

Then the magnitude square of (2.7) shows the contribution of charge pump noise on the output spectrum,

$$s_{\Phi_{out}}(s) = \left(\frac{2\pi N}{I_{cp}}\right)^2 |G(s)|^2 \, s_{I_{n,cp}}(s) \tag{2.8}$$

The significance of (2.8) is that the output noise of the PLL can be reduced with *large charge-pump* current and *lower divide ratio*.

2.2. The 3rd order PLL Dynamics

From noise perspective, we have established mechanism for PLL bandwidth selection which addresses our major corner stone for the low noise PLL design Let us now explore a 3rd order PLL loop dynamics to have a careful look at PLL bandwidth and identify key parameters for the low noise, low jitter and fast settling PLL. Figure 2-7 shows the 3rd order PLL block diagram with 2nd order loop low pass filter. The low pass filter response *F(s)* is shown in (2.9)

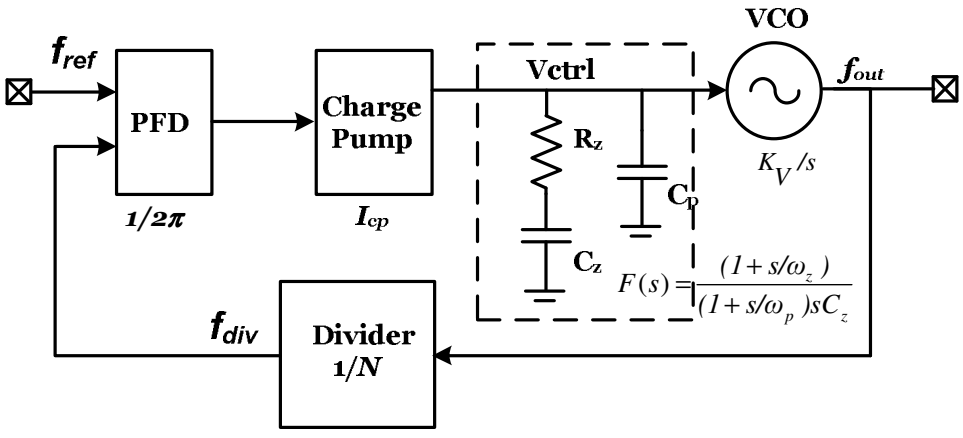


Figure 2-7. A 3rd order PLL with 2nd order loop low pass filter, *F(s)*.

can be used to derive the open and the closed loop transfer function for the PLL [7].

$$F(s) = \frac{(1 + s/\omega_z)}{(1 + s/\omega_p)sC_z} \tag{2.9}$$

$$A(s) = \frac{I_{cp}K_V\ (1 + s/\omega_z)}{2\pi N C_z\ s^2(1 + s/\omega_p)} \tag{2.10}$$

$$\begin{aligned} G(s) &= \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/(K_D K_V) + s^3/(\omega_p K_D K_V)} \\ &\approx \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/(K_D K_V)} \; for \quad K_D = \frac{I_{cp}}{2\pi N C_z} \end{aligned} \tag{2.11}$$

Let us represent the denominator of (2.11) in normalized form,

$$Denom = s^2 + 2\zeta\omega_n s + \omega_n^2 \tag{2.12}$$

then we can define, ω_n, the natural frequency and the damping factor, ζ as,

$$\omega_n = \sqrt{\frac{I_{cp}K_V}{2\pi N C_z}} \tag{2.13}$$

$$\zeta = \frac{\omega_n}{2\omega_z} = \frac{R_z}{2}\sqrt{\frac{I_{cp}K_V C_z}{2\pi N}} \tag{2.14}$$

where ω_z, the PLL zero frequency, is defined as,

$$\omega_z = \frac{1}{R_z C_z} \tag{2.15}$$

The natural frequency and the damping factor play a critical role in PLL settling/locking time and stability. We will explore that little further, but, let us first define the crossover frequency which is approximately the PLL loop bandwidth, the pole frequency and the phase margin as,

$$\omega_c = \sqrt{\omega_z\omega_p} = \omega_z\sqrt{\frac{C_z}{C_p} + 1} = \frac{I_{pump}K_V R_z C_z}{C_z + C_p} \approx \frac{\omega_n^2}{\omega_z} \tag{2.16}$$

$$\omega_p = \frac{1}{R_z\dfrac{C_p C_z}{C_p + C_z}} \approx \frac{1}{R_z C_p} \tag{2.17}$$

$$\Phi_{PM} = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_p}\right) \tag{2.18}$$

2.3 Fast Locking and Settling Time

The PLL settling time is critical for wireless transceiver where fast frequency hopping is required and for lower power battery operated application. When PLL is not used, it can be powered down or shut off to extend battery life since the PLL consumes significant portion of the system power. Currently, for most applications, this is not possible because the wake-up time for the PLL is long and in the order of milliseconds (*ms*) to several microseconds (μs). The PLL settling time, t_s,

$$t_s = \begin{Bmatrix} \frac{1}{\zeta\omega_n}\ln\frac{\Delta f}{\alpha f_o\sqrt{1-\zeta^2}} & 0<\zeta<1 \\ \frac{1}{\zeta\omega_n}\ln\frac{\Delta f}{\alpha f_o} & \zeta=0 \\ \frac{1}{(\zeta-\sqrt{\zeta^2-1})\omega_n}\ln\frac{\Delta f(\sqrt{\zeta^2-1}+\zeta)}{\alpha f_o\sqrt{\zeta^2-1}} & \zeta>1 \end{Bmatrix} \tag{2.19}$$

is a function of damping factor, ζ, natural frequency, ω_n, frequency step, Δf, starting frequency, f_o, and settling accuracy, α [8]. Eq. (2.19) gives insight into fast locking and settling PLL. Maximizing the product $\zeta\omega_n$ can result in fast settling time and if we take (2.16) and (2.14) we find $\zeta\,\omega n \approx \omega_c/2$, i.e., which means wider the PLL loop bandwidth faster the setting time. Since the bandwidth and settling time are related for fast settling architecture a wide PLL bandwidth is desired. However, since bandwidth also affects the noise of the PLL, finding an optimum design with low noise and fast settling is challenging, without added circuits in the PLL. An adaptive bandwidth approach can allow both low noise and low jitter PLL and fast settling time as we will discuss in more detail in Chapter 6.

CHAPTER THREE

3.0. Phase Frequency Detector (PFD)

Phase frequency detector (PFD) output the magnitude of error in phase and frequency between reference signal and the divided feedback signal. It outputs a pump-up or pump-down pulse with pulse width approximately equal to the magnitude of the error. The pump-up and pump-down signal drives a charge-pump which linearly adds or removes charge for the duration of the pulse to increase or decrease the control voltage driving the VCO. In this way, the phase and the frequency of the feedback signal is adjusted until the feedback signal is synchronized or locked with the reference signal. At near lock condition, the error pulse is narrow since the phase difference between reference and feedback clock is small. If this pulse is sufficiently narrow a dead zone exists because the charge-pump cannot react to the phase difference between the reference signal and the feedback signal. Therefore, in the locked condition, the PFD generates a

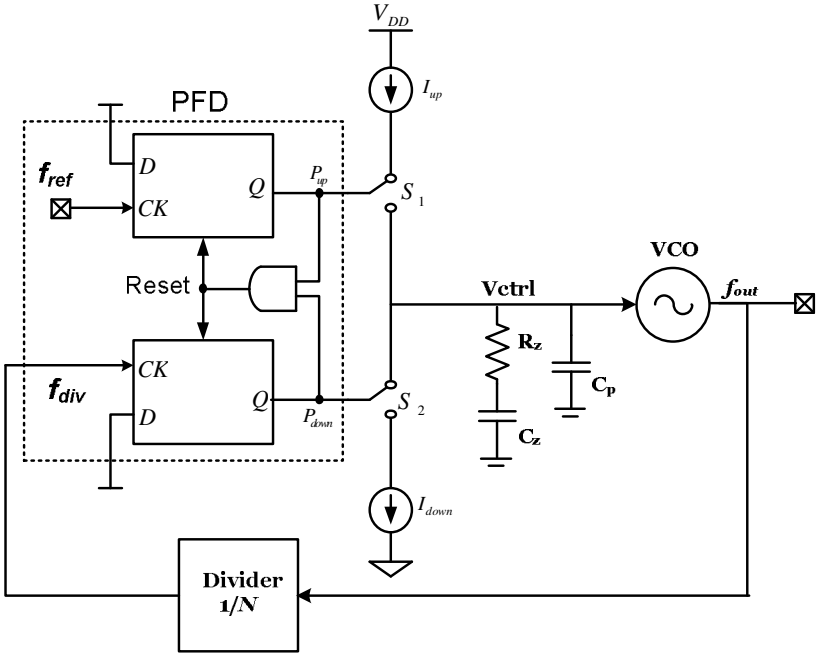


Figure 3-1. PFD block diagram in a PLL

short and equal pump-up and pump-down pulses to drive the charge-pump to prevent dead-zone which causes static offset and adds jitter in the PLL. Figure 3-1 shows a block diagram of digital PFD consisting of two edge-trigged D flip-flops.

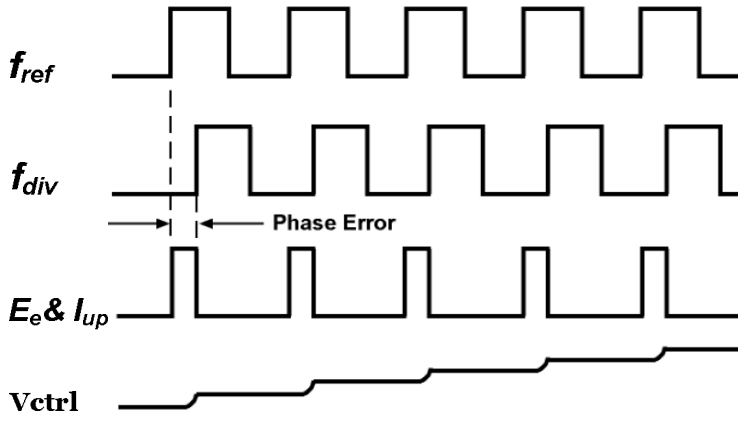


Figure 3-2. PFD/CP timing diagram in the PLL

Figure 3-2 shows an open loop example of the PFD when reference signal, f_{ref}, leads the divided feedback signal, f_{div}. The error signal, E_e, generates a pump-up (P_{up}) signal with pulse width equal to the phase error that injects pump-up current, I_{up}, into the loop filter to increases the control voltage, V_{ctrl}. When the PFD works in a close loop system any increase in V_{ctrl} yields phase shift in f_{div} signal and the E_e or the proportional P_{up} pulse width will vary to change V_{ctrl} until it longer varies indicating the PLL is locked.

Ideally, the PFD should have linear characteristics for the entire range of the input phase difference from -2π to 2π, i.e., the error signal pulse width should vary linearly. When there is frequency difference, the phase difference changes each cycle by $2\pi\frac{\left((1/f_{ref})-(1/f_{div})\right)}{\max\left((1/f_{ref}),(1/f_{div})\right)}$. As the frequency error approaches the lock-in range, the phase varies linearly until cycle slipping stops over the 0 to ±2π range and the PLL phase is acquired via the integrated loop filter voltage. Due

to delay of the reset, however, the linear range of the PFD is limited and less than -2π to 2π. The range is reduced by $\Delta = 2\pi t_{reset} f_{ref}$. *The significance of this is that the PFD will give wrong information when it approaches lock-in range and it fails to acquire frequency lock which affects settling time of the PLL, since, the PLL needs to acquire lock again.*

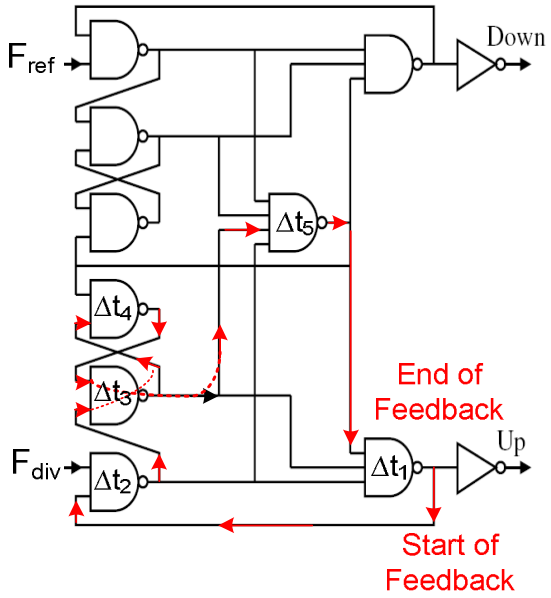


Figure 3-3. Reset path for conventional PFD using NAND based D-FFs

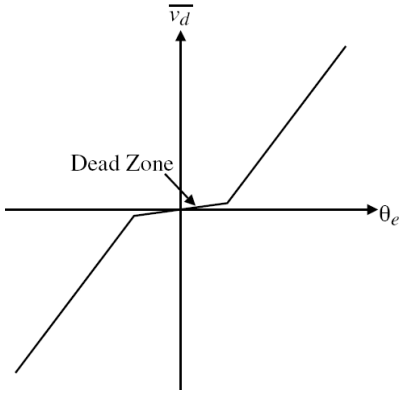


Figure 3-4. Graphical representation of dead zone in PFD

Figure 3-3 shows the reset path for conventional PFD that uses NAND based D flip-flops (D-FF). The reset path delay, $t_{reset,NAND} = \Delta t_1 + \Delta t_2 + 2\Delta t_3 + \Delta t_4 + \Delta t_5$, is large since the signal must go

through 6 gate delays. This delay limits the speed of the PFD and also sets the dead zone for the PFD [9]. A graphical representation of the dead zone is shown in Fig 3-4.

To lower reset delay, a faster true single phase clock (TSPC) D-FF can be used in the PFD. TSPC D-FF can be implemented with just a few transistors instead of a few gates [9]. Figure 3-5 shows the proposed TSPC based pre-charged PFD.

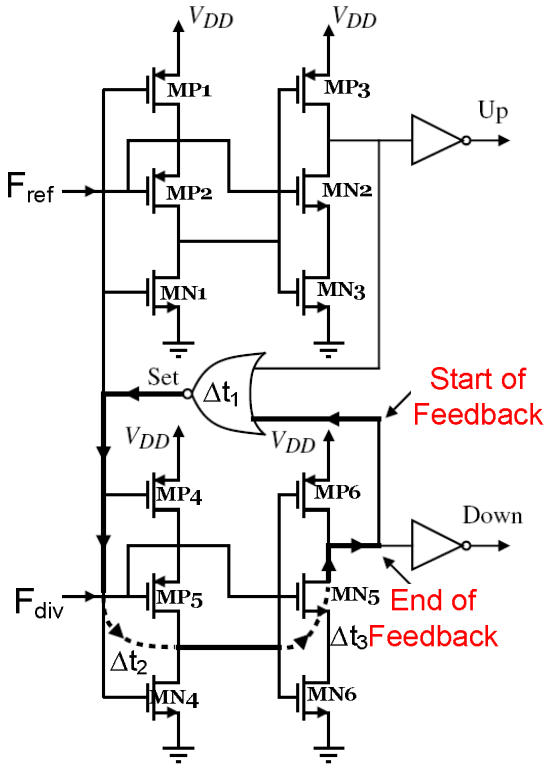


Figure 3-5. Proposed pre-charged TSPC PFD with smaller reset delay

The circuit operation is simple with reset and f_{ref} initially at logic low state so that transistors MP1 and MP2 are turned on. The drain of MN1 is pre-charged to a logic high state as a result. When a rising edge at f_{ref} turn on MN2, and since MN1's drain is pre-charged to a logic high state, MP3's drain will be at a logic low state. Signal at MP3 drain is then inverted to generate the pump-up, *Up,* signal. The bottom latch works the same as top latch but with the feedback clock, f_{div}. Both latches produce the inverse of the desired logic outputs, therefore, a

NOR gate is used for reset instead of a NAND gate used in conventional design. The reset delay path include one gate and two transistor delays, $t_{reset,TSPC} = \Delta t_1 + \Delta t_2 + \Delta t_3 \ll t_{reset,NAND}$ which is significantly less than conventional NAND based PFD in Figure 3-3.

Compared to conversional PFD, the reset delays are short and TSPC implementation provides higher operation frequencies. Fig. 3-6 shows the characteristics of conventional NAND based PFD and proposed pre-charged PFD. Figure 3-7 shows that the pre-charged PFD has higher operational frequency than conventional NAND based PFD.

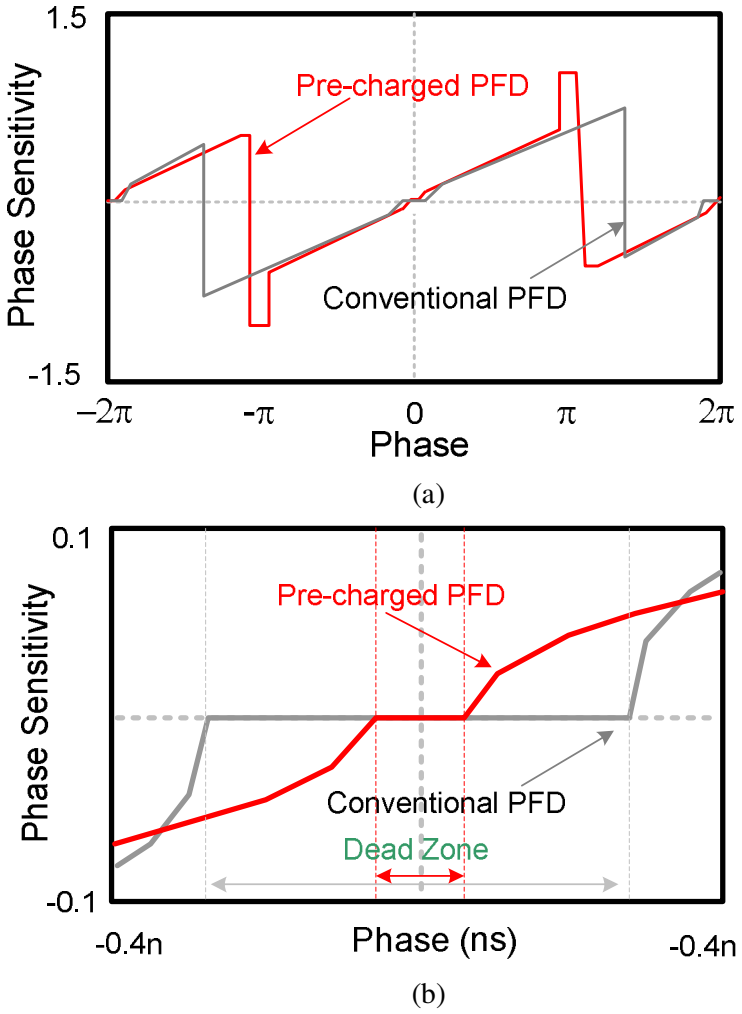


Figure 3-6. (a) Phase sensitivity characteristic (b) dead zones for NAND based PFD and proposed pre-charged PFD.

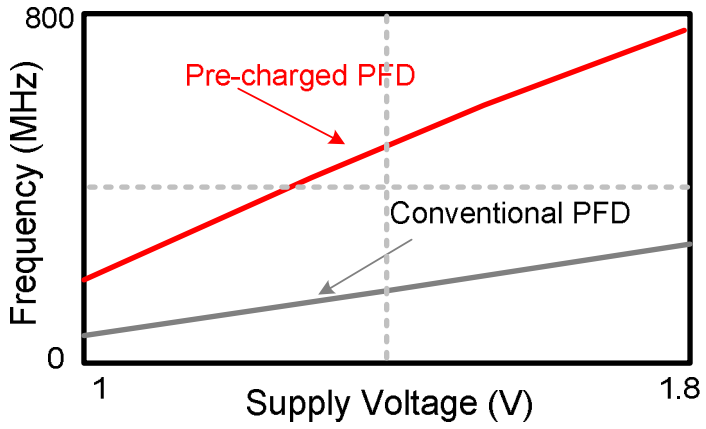


Figure 3-7. Operational frequencies for NAND based PFD and proposed pre-charged PFD.

Fast reset time enables pre-charged PFD to achieve minimum pump-up and pump-down pulse of below 200ps in 0.18µm technology to avoid dead zone. Figure 3-8 shows the simulation results of proposed pre-charged PFD in locked condition. This minimum pulse generated to mitigate dead zone is critical in reducing reference spurs in the PLL. We will discuss this in the next chapter.

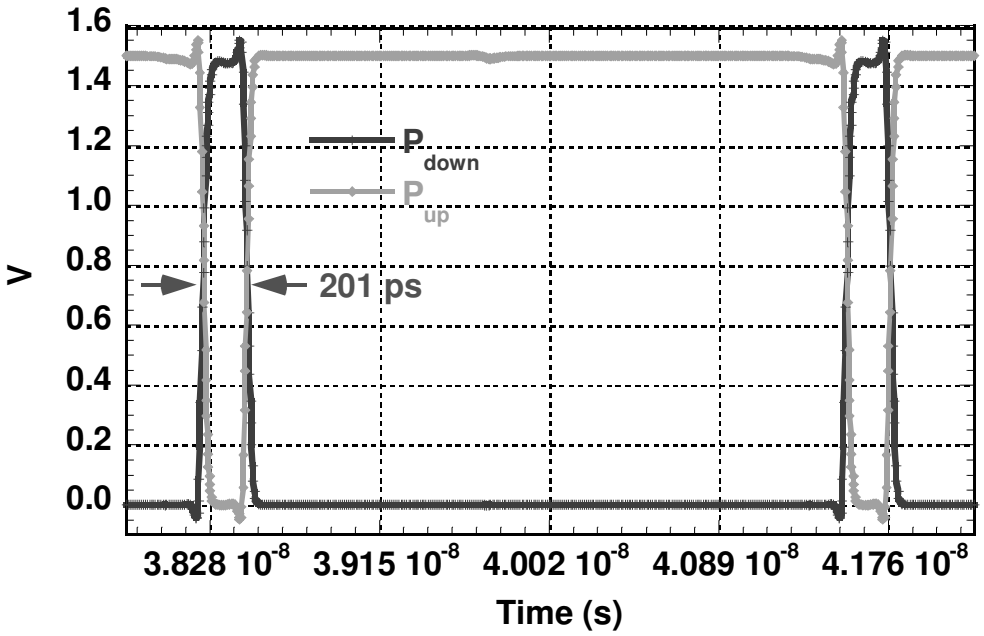


Figure 3-8. Simulation of pre-charged PFD showing output pulse (pulse width ~200ps) during locked condition for dead-zone avoidance

CHAPTER FOUR

4.0. Charge Pump and Spur Suppression

For PLLs, in high speed application, the charge-pump (CP) plays a significant role especially in regards to the reference spur and jitter. CP takes the pump-up and pump-down signal from PFD to inject or remove corresponding amount of charge into or from the loop filter of the PLL. The loop filter does current to voltage conversion via integrating loop filter to get control voltage, V_{ctrl}, that drives the VCO as shown in Figure 4-1. If the delay and pulse width of the PFD are matched and CP has no mismatches between up and down currents, then, the static phase error in the PLL is zero and there is very little reference spur.

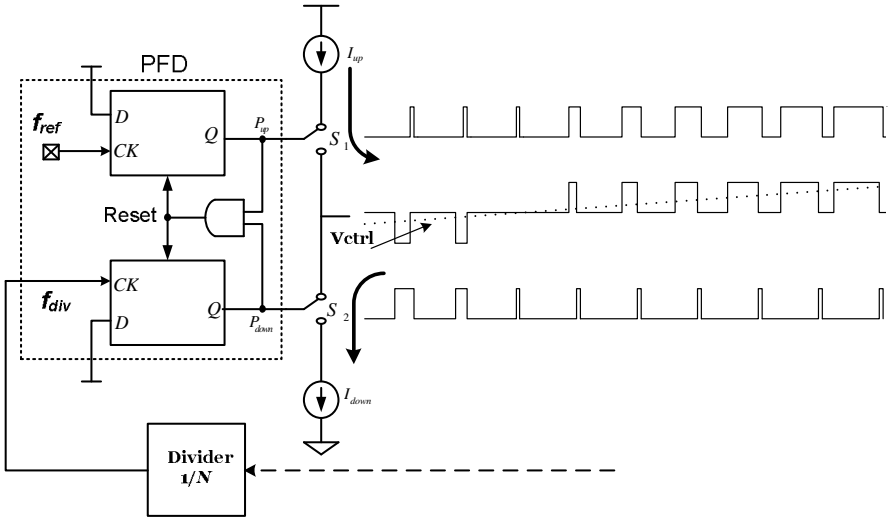


Figure 4-1. Charge-pump operation in PLL

Unfortunately, in the real world, there are non-idealities in both PFD generated pump-up and pump-down pulses and in the CP that contribute to phase error, generate reference spur that adds to jitter. The major phase error contributors are: the leakage currents, the mismatch between pump-up and pump-down currents and the switching time mismatch between the pump-

up (P_{up}) and pump-down (P_{down}) pulses. We can measure the non-idealities in terms of reference spurs with respect to the output carrier which is given by [10]

$$P_r = 20\log\left(\frac{R_z \Delta t_{on} \Delta I_{cp} K_V}{\sqrt{2}}\right) - 20\log\left(\frac{f_{ref}}{f_p}\right)[dBc] \tag{4.1}$$

where, R_z is the loop resistance, Δt_{on} is the minimum PFD P_{up} and P_{down} pulse in locked state, ΔI_p is the current mismatch between P_{up} and P_{down} currents, K_V is the VCO gain, f_{ref} is the reference frequency and f_p is 2nd pole frequency of the loop bandwidth.

From (2.8), to lower the noise contribution from the charge-pump, the I_p should be large. In light of (4.1), one can see larger I_p also suppresses reference spurs by minimizing $\Delta I_p / I_p$ ratio. From (4.1) high spur suppression requires the PLL design to consider lower loop bandwidth resistance, lower VCO gain, minimum PFD output pulse and most importantly good charge-pump current matching.

Aside from spur suppression, both the intrinsic and extrinsic noise of the charge-pump should also be considered. The intrinsic noise exists as flicker or *1/f* noise and thermal noise which are both geometry dependent. Large device width helps reduce both the flicker noise and thermal noise since both have inversely proportional relationship. To reduce extrinsic noise the output impedance of the charge pump should be kept high in order to keep both the power supply rejection ratio (PSRR) and the common-mode rejection ratio (CMRR) high.

4.1. Charge Pump Architecture

Several charge-pump architectures can be chosen for the PLL design. The charge-pumps only differ in architecture by the position of the switches with respect to the current mirrors as shown in Figure 4-2.

A. Drain Switched Charge Pump

One of the most common types is the medium speed drain-switch charge-pump as shown in Figure 4-2(a). There are several drawbacks to this architecture, one of them is the high clock feed-through due to the switches directly connected to the loop filter [11]. The high amplitude current spike which results from the clock feed-though appears at transition of pump-up/down signal due to its triode region operation. Another problem is that in high bandwidth PLLs the loop filter capacitors are comparable with the device parasitic capacitances, making the charge sharing effect a significant source of errors. A dummy switches, as shown in Figure 4-3, can be added to minimize the charge sharing effects, however, this comes with increased clock feed-through. The charge-pump is single-ended, therefore, it is more susceptible to extrinsic noise sources.

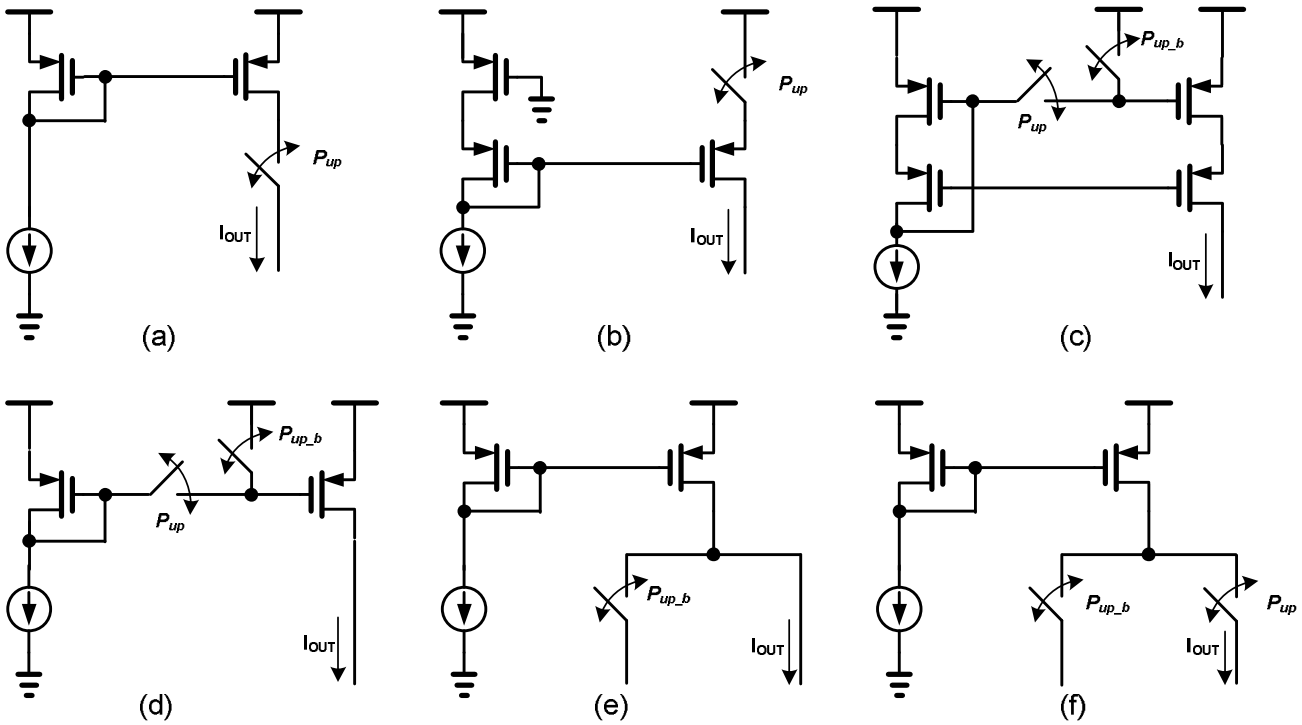


Figure 4-2. Basic charge pump (CP) architectures

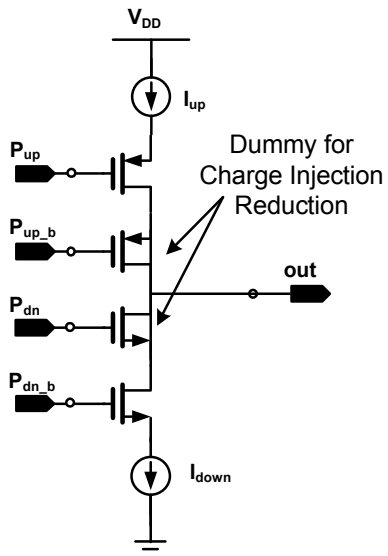


Figure 4-3. Drain switched CP with dummy FETs for charge injection supression

B. Source Switched Charge Pump

Source switching, as shown in Fig. 4-2 (b), have lower clock feed-though when compared to the drain switched, since the current source adds some isolation between the switch and the loop filter output. The current source, which have large geometry for low head room and to lower flicker/thermal noise, are at the drain of the switch, therefore, the switching time are not as fast either. Additionally, there are lower switching spikes since the device switch between off and on states in the saturation region [11]. This charge-pump architecture is single-ended, and as in the previous case, susceptible to extrinsic noise sources.

C. Gate Switched Charge Pump

The gate-switch charge-pump shown in Figure 4-2 (c) and (d), eliminates the current spikes by keeping the current mirrors either in off or saturation state. Its downside is that this architecture in inherently low speed due to the high gate capacitance connected at the switching nodes. The output impedance can be increased with cascode current source to reduce susceptibility of extrinsic noise sources since it operates at lower frequencies. The cascode

current source has high output impedance at low frequencies but it drops off fast at higher frequencies, since it is a two pole system, when compared to single FET current source.

D. Differential Input Singled-Ended Output Current Steering Charge Pump

A higher switching speed is achieved with a differential switch, as shown in Figure 4-2 (e) and (f), which uses the current steering technique. Since the current source does not have to turn-off the charge-pump, it is inherently very high speed. Fully differential charge-pumps [11] are preferred in low-voltage low-jitter PLLs due to their high supply and substrate noise rejection and higher voltage swings capability. However, they require differential loop filter that occupies large silicon real estate, they are not very desirable or low cost. Therefore, a differential input single-ended output current steering charge pump offers the best performance which includes lower susceptibility of extrinsic noise due to noise rejection, high speed, and good matching.

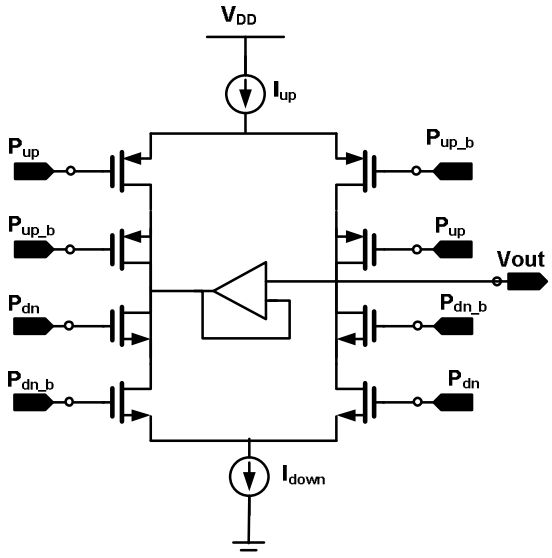


Figure 4-4. Differential input singled-ended output current steering charge pump

A unity gain buffer is required to keep the dummy output at the same potential as the loop filter output to avoid charge sharing. Half-sized dummy transistors can be added to compensate for the charge-injection since the charge splits roughly half and half between source

and drain of the switching FET as shown in Figure 4-4. Since the dummy transistors are at cut-off region, the charge cancellation is not perfect. A better charge cancellation technique is proposed for the implemented charge pump as described section 4.2. In addition, the CP matching in also enforced over control voltage range for the PLL

4.2. Proposed Charge Pump Architecture with Adaptive Current Control

A dynamic replica biased current steering change pump is proposed to reduce current mismatches across the control voltage range to suppress reference spurs as shown in Figure 4-5.

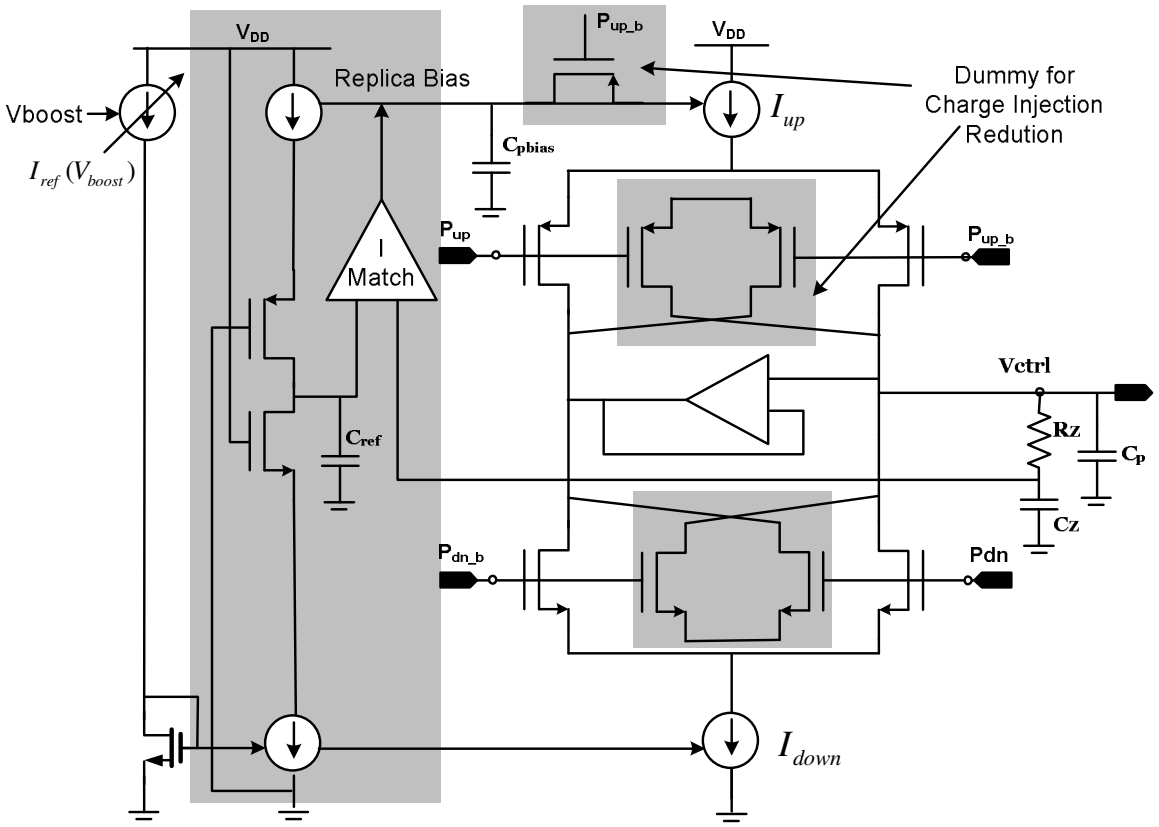


Figure 4-5. Proposed current steering replica biased charge-pump with glitch compensation and adaptive current control for fast settling PLL

The CP introduced spurs in PLL contribute to RMS jitter (RJ) in the PLL. The reference spurs in the PLL are results of mismatch, charge-injection or glitch and current leakage. In the proposed charge pump architecture to deal with current mismatch a dynamic replica baising with

a feedback amplifier is applied to insure good current matching of currents over all control voltage values at the charge-pump output. Figure 4-6 shows the graphical representation of pump-up and pump-down currents over the control voltages with and without the replica bias. This insures the DC current levels are matched.

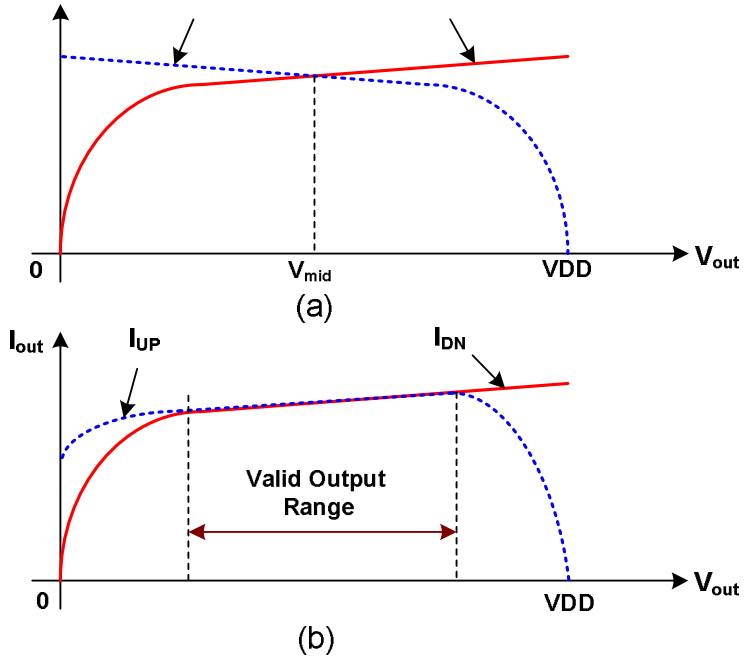


Figure 4-6. (a) Pump-up (I_{up}) and pump-down (I_{down}) current match at V_{mid} (b) I_{up} & I_{down} with replica bias OPAMP (I Match) match very well over valid CP output range.

The dynamic currents due to charge-injection also need to be considered to achieve well matched currents. The current glitch and offset is compensated in the proposed design by feeding back loop filter voltage to the replica OPAMP while using cross-coupled dummy FETs that are sized same as CP switches for simultaneous charge injection cancellation. The current glitch however, vary over the control voltages and they are too fast for feedback compensation, therefore, a dummy FET driven with pump-up pulse is added to the gate bias of the PMOS current source to insure good glitch cancellation as shown in Figure 4-5. The proposed CP has programmable currents which adaptively vary as a function of V_{boost} to achieve adaptive bandwidth control in the PLL for faster settling.

TABLE 4-I
PERFORMANCE OF PROPOSED CHARGE PUMP

Parameter	Simulated Results
Supply Voltage	1.5 V
I_{PUMP} (PLL locked) (Acquisition Max)	100 µ A 450 µ A
Mismatch (worst case)	0. 25%
Linear Range	0.2V – 1.3V
Power Consumption	540 µW
Reference Spur Suppression	>77.82 dB

The simulated performance of the proposed charge-pump shows very good results and is tabulated in Table 4-1. The worst case current mismatch over the PLL tuning range is less than 0.25%. Fig. 4-7 shows that over 50ns, in an open loop simulation, the integrated voltage only changes 76µV, while the glitches are less than 0.4mV using the proposed approach in the charge-pump. The linear range extends from 0.2V to 1.3V with total power consumption of 540µW from 1.5V supply. The reference spur suppression is better than 77.882 dB.

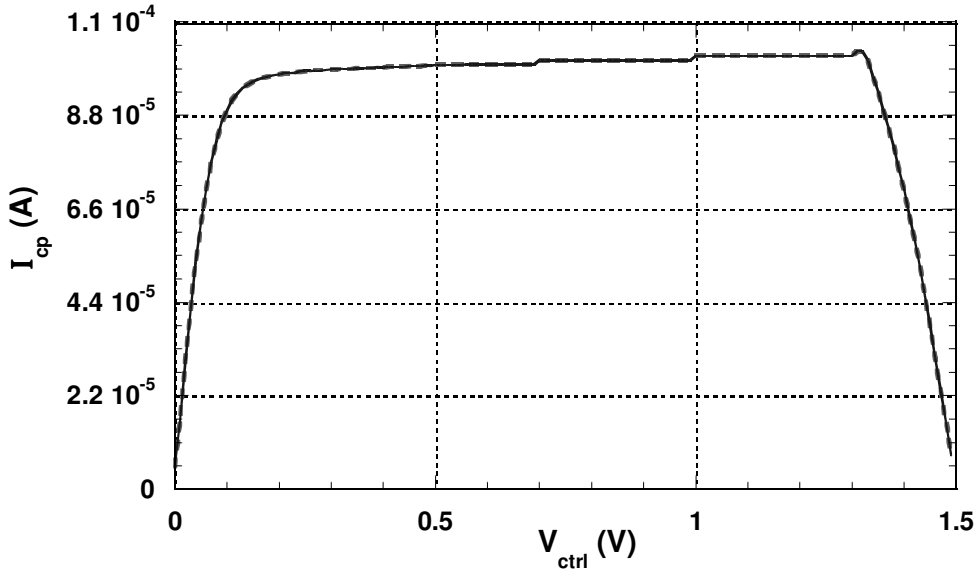


Figure 4-7. Simulated I_{up} & I_{down} for CP over control voltage.

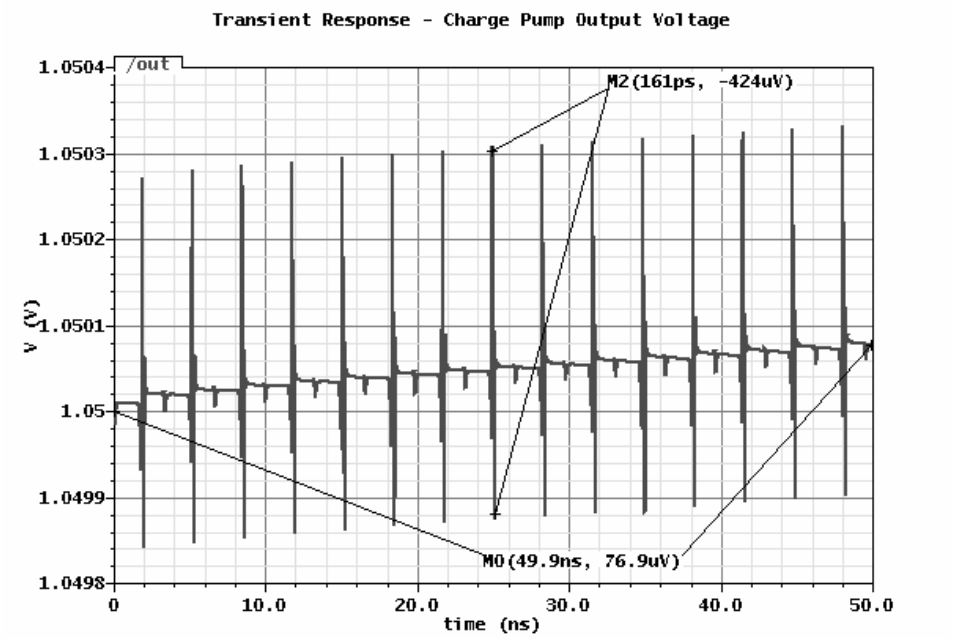


Figure 4-8. Open loop transient response, for the proposed CP, over 50ns to show robustness of glitch compensation and current matching circuits.

CHAPTER FIVE

5.0. Voltage Controlled Oscillator (VCO)

A voltage controlled oscillator (VCO) is the principal key component of a PLL and has most impact on the performance of any PLL, especially, in regards to the phase noise, spectral clarity, low power and tuning ability. As the name suggests the VCO is an oscillator that outputs a periodic signal whose frequency is voltage dependent, and thus, the voltage controlled oscillator.

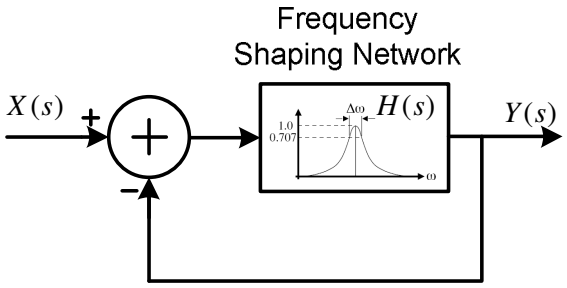


Figure 5-1. Positive feedback oscillator with frequency selective network.

An oscillator is a positive feedback system, as shown in Figure 5-1, with transfer function given by

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)} \tag{5.1}$$

An oscillator oscillates when *H(s)=1+j0* or the when the loop gain $|H(s)| = 1$ and the phase shift around the loop $\angle H(s) = 0.$ The open loop quality factor, Q, is a measure of how much the closed loop system opposes variation in the oscillation frequency [12].

$$Q = \frac{\omega_o}{2} \frac{d}{d\omega} \left(Arg\{H(s)\} \right) \tag{5.2}$$

Higher the Q of *H(s),* smaller the variation, and thus, lower the phase noise. If a VCO is linear or ideal, then we can define its output frequency, f_o, as a linear function of control voltage, V_{ctrl}, as

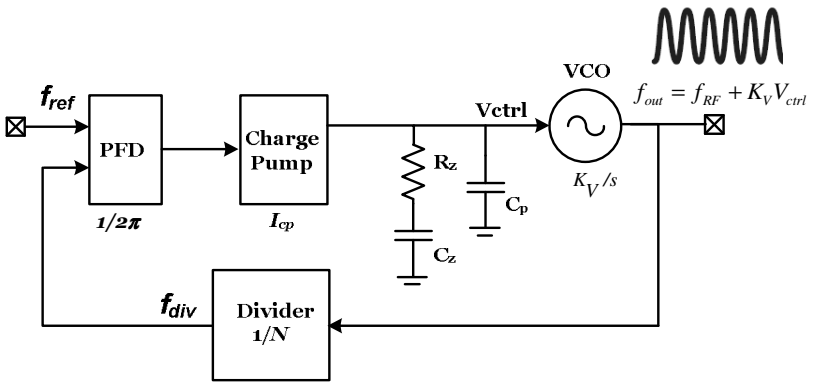


Figure 5-2. Block diagram of VCO operation in PLL.

$$f_{out} = f_o = f_{RF} + K_V V_{ctrl} \tag{5.3}$$

where, K_v, is the VCO gain and f_{FR} is the free running frequency. Since the phase is integral of frequency with respect to time, we can define the output voltage of the VCO as,

$$V_{out}(t) = A_{VCO} \cos\left(f_{RF} t + K_V \int_{-\infty}^{t} V_{ctrl}\, dt \right) \tag{5.4}$$

with VCO output amplitude A_{VCO}.

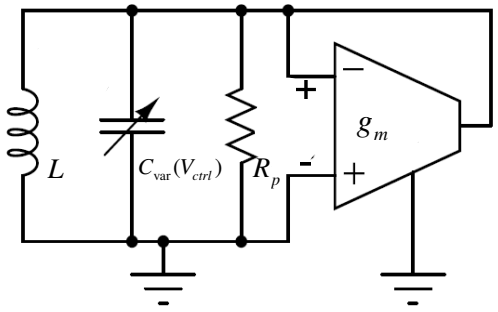


Figure 5-3. General model for LC VCO.

For high frequency application, especially for very low noise application, *LC* VCO topology is desirable owing to its high spectral quality and high quality factor at low DC power consumption. Figure 5-3 shows the general model for an *LC* oscillator, where, R_p is the equivalent parallel resistor of the *LC* tank, varactor or voltage controlled capacitor is C_{var} that

varies with control voltage $V_{ctrl,}$ and a transconductance of an active device (FET), g_m, provides a negative input resistance. When $1/g_m \geq R_p$, the oscillation is sustained at frequency,

$$f_o = \frac{1}{2\pi\sqrt{LC_{\text{var}}(V_{ctrl})}} \tag{5.5}$$

Wireline and wireless transceiver may use a single phase or a multi-phase VCO. A half rate wireline transceiver, primarily used for high data bandwidth application, such as 10Gbps, requires quadrature phases, 0º and 90º, for clock and data recovery circuits (CDRs). Similarly, most wireless transceiver topology requires quadrature phase for image rejection and to improve the SNR of the receiver. There are several ways to generate quadrature phase including

- Use of RC poly phase filter at carrier oscillation frequency
- A single phase LC VCO at twice the carrier oscillation frequency and a divide by 2 frequency divider to generate quadrature phases.
- Quadrature LC VCO at carrier oscillation frequency

In this chapter we will explore both the single phase LC VCOs and quadrature phase LC VCOs for wireline and wireless communication. We will compare several novel LC VCOs and make determination on choice of VCO for our proposed low jitter fast settling PLL architecture. To characterize the performance of each VCO let us first explore the fundamental measure of phase noise in the oscillator.

5.1. LC VCO Phase Noise Model

Intrinsic and extrinsic noise injected into an LC oscillator can be measured in frequency domain as phase noise and in time domain as timing jitter. In RF and high speed application, the phase noise is a measure most commonly used. The most well-known phase noise model is the

Leeson's model proposed by D.B. Leeson in 1966 [13]. The model accounts for phase noise in the $1/f^2$ of the phase noise curve dominated by white FM noise shown in Figure 5-4.

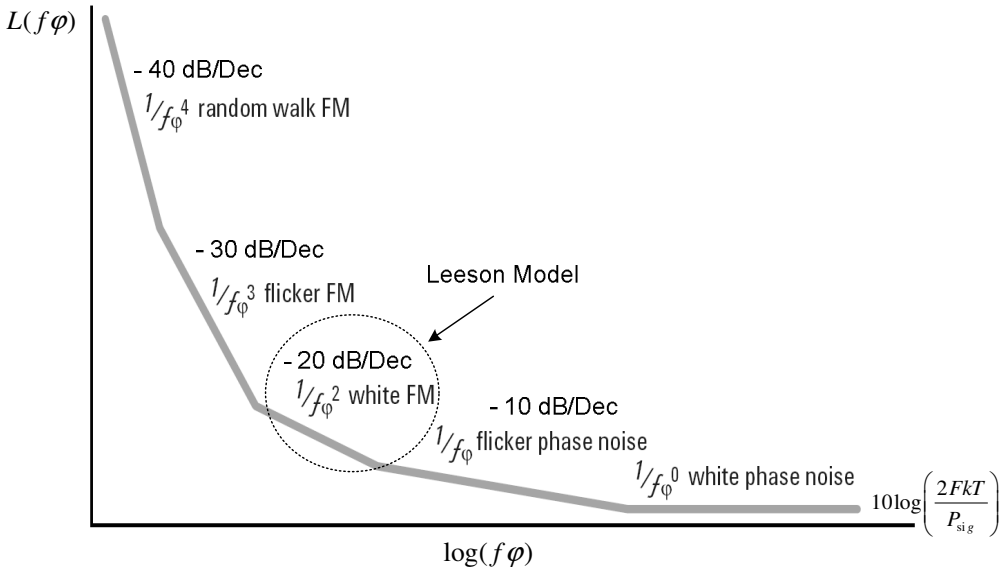


Figure 5-4. Phase noise of VCOs showing dominant noise sources

For the LC VCO tank in Figure 4-3, when $\Delta\omega \ll \omega_o$, we can compute the impedance about the resonance $\omega = \omega_o + \Delta\omega$ as,

$$\begin{aligned} Z_{tank}(j\omega) &= Z\left(j(\omega_o + \Delta\omega)\right) = j(\omega_o + \Delta\omega)L \,//\, \frac{1}{i(\omega_o + \Delta\omega)C_{\text{var}}} \\ &\approx -\frac{j\omega_o L}{2(\Delta\omega/\omega_o)} = -jR_p\frac{\omega_o}{2Q\Delta\omega} \end{aligned} \tag{5.6}$$

The total equivalent resistance then has an equivalent mean square noise current, $\overline{i_n^2}/\Delta f = 4kT/R_p$ which we can write as voltage noise, $\overline{v_n^2}/\Delta f = \left|Z_{tank}(j\omega)\right|^2\left(\overline{i_n^2}/\Delta f\right)$. By defining a noise factor, $F(\Delta f)$, as the ratio of total noise in the tank at Δf over noise in the tank due to tank loss at Δf, we can write the single side-band (SSB) output noise spectral density expression as,

$$\begin{aligned}\overline{v_n^2}/\Delta f &= \frac{4kTF(\Delta f)}{R_p}\left(\frac{R_p f_o}{2Q\Delta f}\right)^2 \\ &= 4kTF(\Delta f)R_p\left(\frac{f_o}{2Q\Delta f}\right)^2\end{aligned} \tag{5.7}$$

Then, the phase noise is defined as the ratio of noise spectral density over the power of carrier as,

$$\begin{aligned}L(\Delta f) &= 10\log\left(\frac{S_{noise}(\Delta f)}{Psig}\right) = 10\log\left(\frac{1/2\cdot\overline{v_n^2}/\Delta f}{\overline{v_{sig}^2}}\right) \\ &= 10\log\left(\frac{4kTF(\Delta f)R_p}{V_{sig}^2}\left(\frac{f_o}{2Q\Delta f}\right)^2\right)\end{aligned} \tag{5.8}$$

The factor of ½ is based on equal partition of AM and PM noise according to equipartition theorem [14]. The Leeson's model with flicker noise or *1/f*^{3} noise included is later added assuming $F(\Delta f)$ is constant over frequency to get the final phase noise expression as,

$$L(\Delta f) = 10\log\left(\frac{4kTF(\Delta f)R_p}{V_{sig}^2}\left(1+\frac{f_o}{2Q\Delta f}\right)^2\left(1+\frac{\Delta f_{1/f^3}}{|\Delta f|}\right)\right) \tag{5.9}$$

This noise model shows the essential parameters to achieve low phase noise for the LC VCO including maximizing tank swing, V_{sig}, maximizing tank Q, and reducing the flicker and thermal noise contribution. The flicker noise for FET is a function of device geometry and in saturation is given by,

$$\overline{i_{nd}^2}\Big|_{1/f} = \frac{K_f g_m^2}{f W L C_{ox}^2}\Delta f \tag{5.10}$$

The thermal noise due to the FET channel resistance is given by,

$$\overline{i_{nd}^2}\Big|_{th} = \gamma 4KTg_{do}\Delta f;\ \gamma = \begin{cases}2/3 & -Long\ Channel\\ 2\sim 3 & -Short\ Channel\end{cases} \tag{5.11}$$

where, g_{do} is the (1+g_{mbs}/g_m) [7]. The mean squared input referred voltage noise can be calculated by dividing respective noise by g_m^2. It is apparent from (5.10) and (5.11) that increasing geometry lowers flicker noise and larger g_m lowers the thermal noise.

5.2. Quadrature LC VCO

The RF wireless transceivers, superheterodyne or homodyne, require accurate quadrature VCO or a single VCO with previously mentions methods including RC poly-phase filter and divide by two circuit to generate quadrature phase LO signals. The LO quadrature phase accuracy determines the image rejection in superheterodye systems and determines the SNR as we have seen in Chapter 1. To generate quadrature phase LO signals, the quadrature VCO is preferred since it has better phase and amplitude matching over process and temperature when compared to the poly-phase filter. For homodyne systems phase mismatches leads to 2nd order intermodulation distortion (IMD_2) and DC offset, and thus, a low quadrature phase error is required, generally less than 2°. A quadrature LC VCO is the most desirable method for quadrature phase generation since the alternative, the ring VCO, has higher phase noise at frequencies of interest [15].

Quadrature LC VCO relies on the coupling of two symmetric *LC*-tank VCOs, each of which contributes 45° phase shift thereby achieving aggregate 90° or quadrature phase. Popular quadrature LC VCO architectures are shown in Fig. 5-5, where, the quadrature phase is achieved by coupling signal from one VCO core to another using either a parallel or series FET. The ratio of FET width determines the coupling factor, the VCO phase noise and the phase error. When a signal is coupled from one VCO core to another it causes phase shift in the resonator, or resonator phase shift (RPS). RPS plays a significant role in optimization of the phase noise and the phase error. Parallel coupled QVCO in Figure 5-5(a) has RPS between 90 and 180 (see Figure 5-5(d)) degrees, where, neither the phase noise nor the phase error is optimum. If you optimized for phase

noise then phase error is affected and vice-versa. For top series coupled QVCO, the RPS is 90 degrees (see Figure 5-5(b) & (e)) so the quadrature phase error is minimum and the phase noise can be reduced almost independent of phase error. The bottom series coupled QVCO in Figure 5-5 (c) has RPS of 0 degrees which mean phase noise is optimum because tank Q maximized [16] but the phase error is not as good.

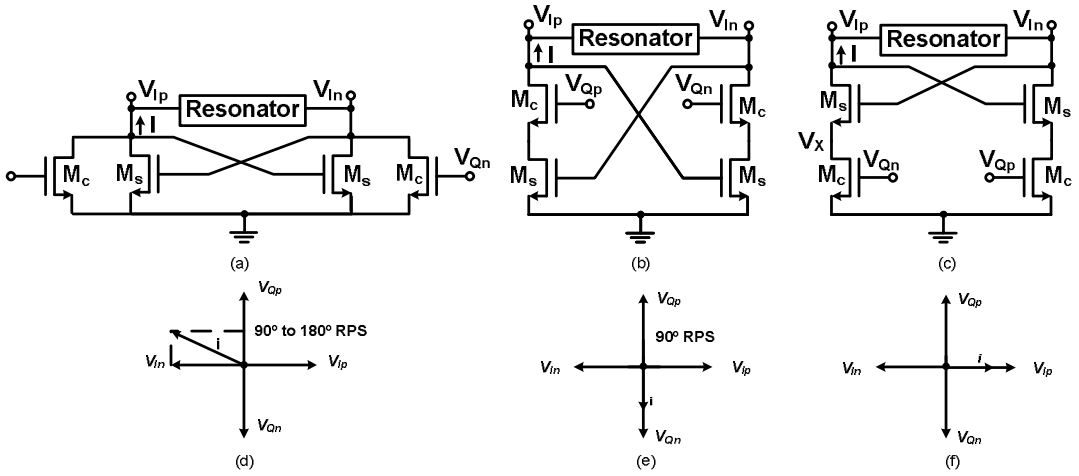


Figure 5-5. (a) Parallel coupled, (b) Top series coupled, and (c) Bottom series coupled quadrature LC VCO with corresponding resonant phase shift (RPS) of QVCO in (d), (e) and (f), respectively.

A. Top-Series Coupled Quadrature VCO

The quadrature error and the phase noise both affect the SNR of transceivers, therefore, top series coupled QVCO (TS-QVCO) can provide the optimum performance for both phase error and phase noise. Figure 5-6 shows the proposed top series coupled QVCO.

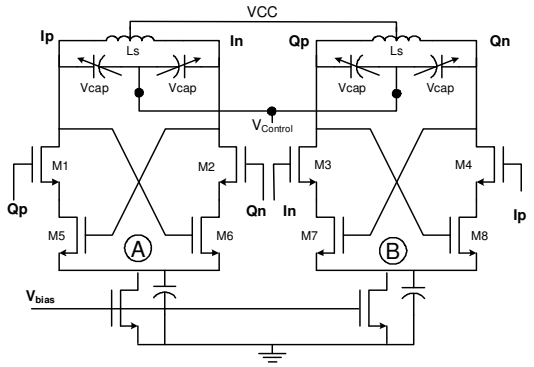


Figure 5-6. Proposed top series-coupled quadrature LC VCO (TS-QVCO) architecture

In TS-QVCO, FETs (in Figure 5-6) M1, M2 and M3, M4 are placed in series with cross-coupled FETs M5, M6 and M7, M8. The gate of FETs M1 and M2 is driven by tank voltage of LC VCO *B*, which effectively couples signal from *B* to LC VCO *A*. Similarly FETs M3 and M4 couple signal from LC VCO *A* to LC VCO *B*. By optimizing this coupling factor, the LC VCO tank quality factor (*Q*) and the flicker noise, a low phase noise and low phase error TS-QVCO can be achieved. The simulation shows that an optimum coupling factor, β, of 0.63 is able to achieve both low phase noise and low phase error.

$$\beta = \frac{(W/L)_{M1..M4}}{(W/L)_{M5..M8}} = 0.63 \tag{5.12}$$

The series coupling FET has larger geometry but smaller *W/L* ratio when compared to the cross-coupled FETs which has smaller geometry but larger *W/L* ratio. Larger *W and L* geometry is selected for the series coupling FETs since its flicker noise or the *1/f* affects the phase noise performance of the TS-QVCO much more than the cross-coupled pair which primarily works in the linear region. Additionally the series coupling FETs also work to reduce the *1/f* noise up-conversion from the current sources.

The VCO phase noise performance is highly dependent on the *Q* of the LC tank and therefore, the quality factors of inductors and varactors are important. At higher frequency the phase noise of LC VCO is inversely proportional to Q^2. The quality factor of the inductor is limited by physical phenomena that converts the electromagnetic energy into heat and radiation and is a function of size and material. If the substrate is sufficiently conductive the bulk eddy currents (shown in Figure 5-7) flow in the substrate and present itself as a dominant form of loss and therefore, limits the Q [17]. Scaling the inductor features such as the spirals inner diameter, conductor width, spacing between conductors and outer diameter can lower these substrate losses. To achieve high Q, optimization process should include keeping the inner diameter of the spiral

large, higher number of turns, larger conductor width while maintaining relatively small outer diameter. Furthermore, the spacing between conductors should be carefully selected to reduce parasitic capacitive coupling while achieving desired inductance value. ASITIC EM solver based model provided through the Jazz Semi. is used to design a differential coplanar spiral inductor with half inductance of 1.47 nH and Q = 9.9 at 2.3 GHz.

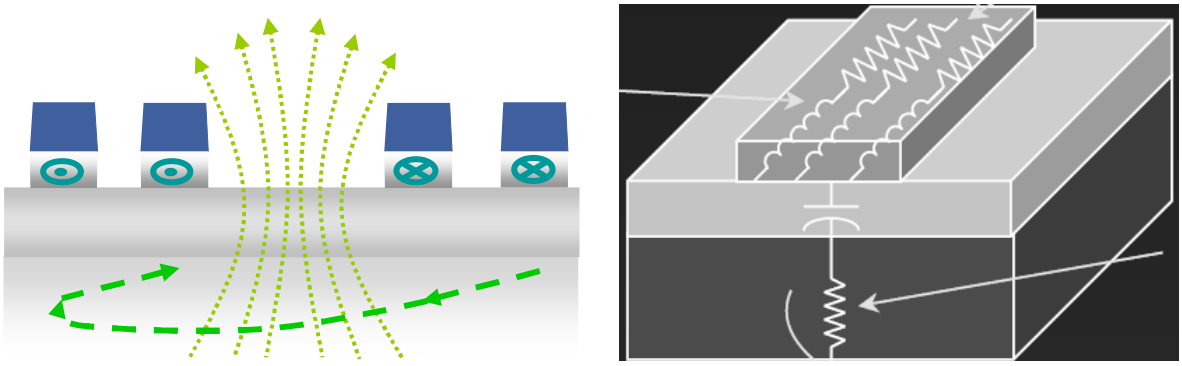


Figure 5-7. Eddy current substrate losses and parasitic losses in inductors

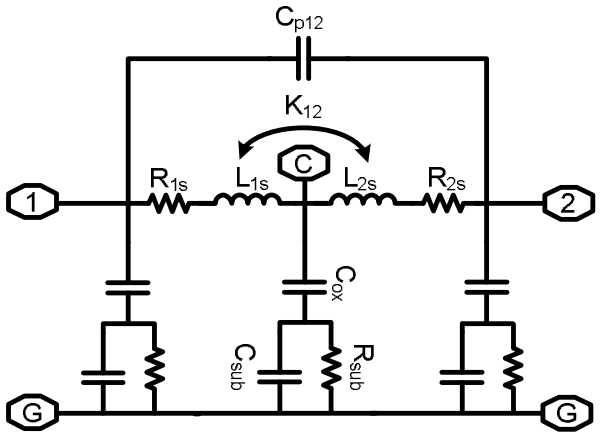


Figure 5-8. Lumped circuit model for planar differential spiral inductor.

An equivalent passive lumped model of the differential spiral inductor is shown in Figure 5-7. The optimum inductance can be selected for a given DC bias current to achieve high quality factor, Q. From Leeson formula we derived in (5.9), one can stipulate that decreasing the device noise more specifically, *1/f* and thermal noise, will improve the phase noise of the LC VCO. Large device (FET) geometries are used in TS-QVCO to reduce device noise to improve the

phase noise. In addition a low pass filter is implemented to filter out unwanted $2\omega_o$ signal at the drain of the NMOS current source. Furthermore, low pass filters is also implemented to reduce the high frequency noise in the bias node of the current source, varactor voltage control node, and the power supplies.

The CMOS TS-QVCO was fabricated in Jazz 0.18-µm SiGe-BiCMOS process. Figure 5-9 shows the micrograph of the TS-QVCO. The measurement shows that the TS-QVCO is able to achieve measured output power of –3 dBm, after compensating for the cable losses and RF probe losses (~1.6 dB), while consuming only 11.05 mW of DC power. Figure 5-10 shows the spectrum analyzer output of the measured TS-QVCO tuned to 2.3 GHz frequency. The VCO achieves the phase noise of less than –120 dBc/Hz at 1 MHz frequency offset from carrier frequency of 2 GHz, as shown in Figure 5-11(a). Fig. 5-11(b) shows measured transient signal from the TS-QVCO at 2 GHz. The VCO has a tuning range of little more than 300 MHz which translates to 14%. The measurement result correlates very well with the simulation results. The normalized phase noise has been defined as a figure of merit (FOM) for oscillators and is given by,

$$FOM\big|_{(dBc/Hz)} = 10\log\left[\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{L(f_o)P_{DC}}\right] \tag{5.13}$$

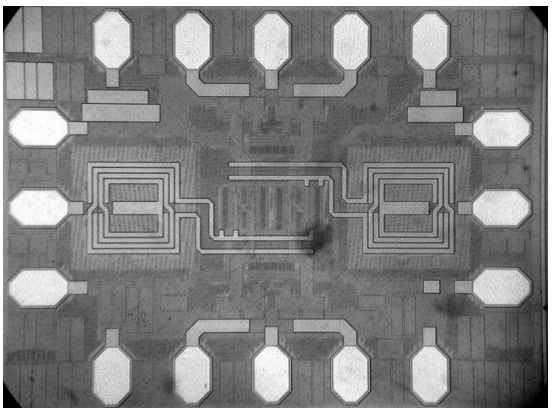


Figure 5-9. Micrograph of proposed series-coupled quadrature LC VCO (TS-QVCO)

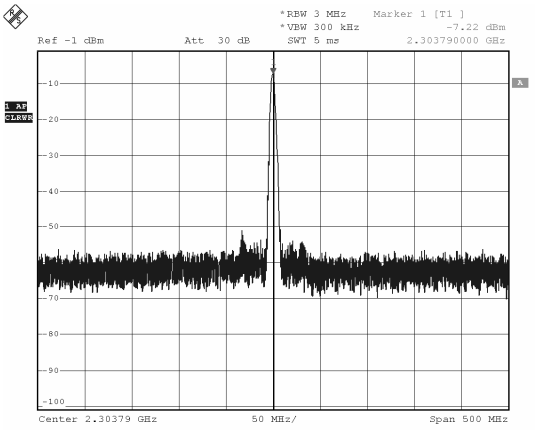
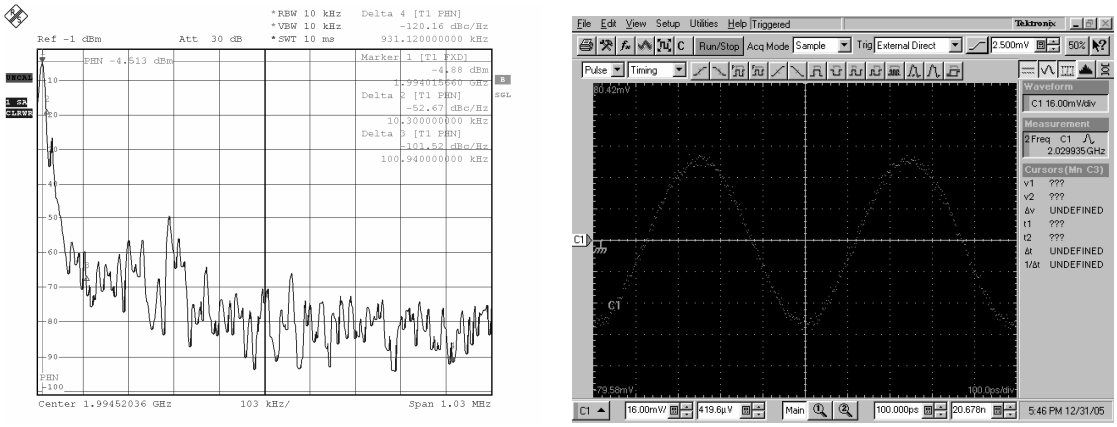


Figure 5-10. TS-QVCO tuned to maximum frequency of 2.3 GHz.



(a) (b)

Figure 5-11. Measured phase noise < –120 dBc/Hz at @ 1MHz frequency offset from 2 GHz carrier frequency (b) Transient output of TS-QVCO operating at 2 GHz frequency.

where, *P* is the total DC power consumption for the quadrature VCO. The FOM factor of -176 dBc/Hz for the TS-QVCO compares well with other works in Table 5-I while realizing higher output power, and thus, higher power efficiency.

TABLE 5-I
QUADRATURE VCO FOM FACTOR COMPARISON

Ref	f_0 *(GHz)*	*Power (mW)*	*Tuning Range*	*FOM (dBc/Hz)*
This Work	**2.0**	**11.05**	**14%**	**-176**
[18]	1.8	50	18%	-179
[19]	2.0	11	10%	-175
[20]	2.0	25	15.7%	-165

B. Top-Series Coupled Quadrature VCO with 4-Way Center-Tapped Inductor

A low voltage and low power CMOS TS-QVCO with a 4-way center tap inductor, as shown in Fig. 5-5, is realized in a 0.18-µm process to achieve even lower phase noise and phase error for WiMax and IEEE 802.11 WLAN application. A four-way center-tapped inductor helps lower phase noise in TS-QVCO.

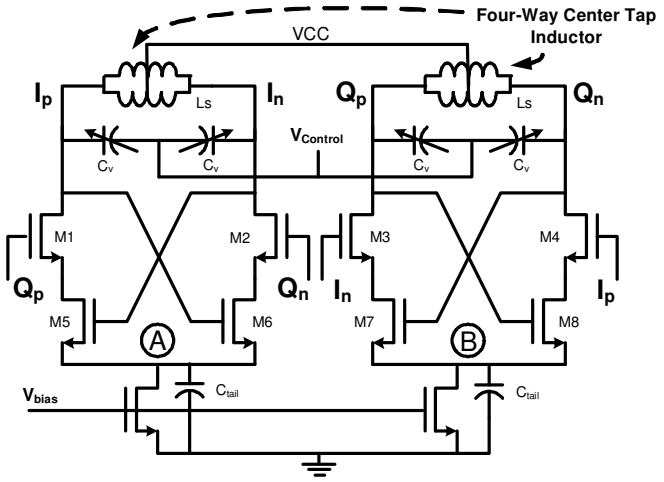


Figure 5-12. Proposed TS-QVCO with phase noise lowering 4-way center-tapped inductor architecture

In a current-limited LC VCO, the phase noise performance is highly dependent on the Q of the LC tank, and therefore, the quality factor of inductors and varactors and the bias current level, I_{bias}. It can be shown that at higher frequency, the phase noise of the current-limited LC VCO is inversely proportional to Q^2 and $(I_{bias})^2$. The optimum inductance can be selected for a given DC bias current to achieve high Q. If the substrate is conductive, the bulk eddy currents flow in the substrate and presents itself as a dominant form of loss and therefore, limits the Q. In modeling terms, the smaller the series parasitic resistance of the tank, the better the Q factor. Leeson formula (5.9) in the $1/f^2$ region which can be extended to include inductance value L, and the corresponding tank resistance R_p, to approximate the phase noise of LC VCO as

$$L(\Delta f) = 10\log\left(F\frac{2kTR_p^{\ 3}}{V_p^2 L^2 \Delta f^2} \right) \tag{5.14}$$

where F is the noise of the device excess noise factor, V_p is the peak voltage swing, Δf is the frequency offset from the carrier, k is the Boltzmann constant, and T is the temperature. Equation (5.15) gives the noise factor for a current-limited LC VCO,

$$F = 1 + \frac{4\gamma g_m R_p}{9} + \frac{4\gamma I_{bias} R_p}{V_p \pi} \tag{5.15}$$

where γ is the FET noise factor and g_m is the current source transconductance [21]. The peak oscillator swing V_p is approximately equal to parasitic resistance of the tank times the bias current, I_{bias}, multiplied by $2/\pi$ and thus, is limited for a given technology due to device breakdown issues. One can stipulate that by keeping V_p the same and reducing R_p, we can increase the bias current to achieve lower phase noise from (5.14) and (5.15).

We, therefore, propose the use of a four-way center-tapped inductor in Figure 5-13 to reduce the R_p by a factor of 4, without degrading the Q of the inductor, to potentially reduce the phase noise by a factor of 6 dB.

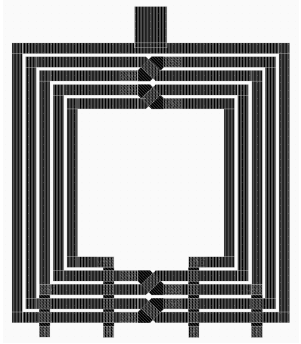


Figure 5-13. Proposed top 4-way center-tapped inductor to reduce the phase noise of TS-QVCO

In a tapped configuration, the parasitic associated with any additional circuitry do not appear directly across the LC tank. Instead, they appear solely across a portion of the inductor. Thus, the entire tank is affected by the amount of loss divided by the tapping ratio formed by the

inductors. The four-way center tapped inductor is designed and modeled using ADS momentum with a large spirals inner diameter (*100 μm*), wide conductor width (*8 μm*), optimum spacing between conductors (*2 μm*) and an optimum number of turns, 5, to lower substrate losses and achieve high *Q*. The reduced parasitic resistance via the 4-way center-tapped inductor in the TS-QVCO will allow for increased bias current to reduce the phase noise as given by (5.14).

Further reduction in the flicker noise and the thermal noise is achieved with optimum device biasing and sizing. In addition, a low pass filter is implemented to filter out an unwanted $2\omega_o$ signal seen at the drain of the NMOS current sources. Additional low pass filters is also used to reduce the high frequency noise at the current source, varactor voltage control node, and the power supplies. The micrograph of the fabricated TS-QVCO with a 4-way center taped inductor is shown in Figure 5-14.

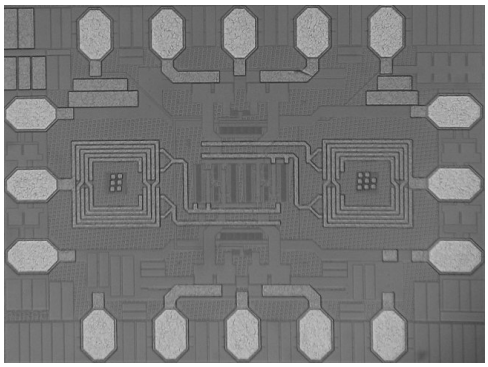


Figure 5-14. Micrograph of proposed TS-QVCO with 4-way center-tapped inductor (0.74 mm^2)

The CMOS TS-QVCO with a 4-way center-tapped inductor was fabricated in the Jazz 0.18-μm CMOS process. The measurement shows that the TS-VCO with 4-way center-tapped inductor is able to achieve measured output power of –8 dBm, while consuming only 10.5 mW of DC power (see Figure 5-15). At a frequency of 2.345 GHz, a phase noise of –122.2 dBc/Hz is measured as shown in Figure 5-16. Figure 5-17 shows the measured phase noise over the tuned frequency range. The TS-QVCO achieves the phase noise lower than –119.4 dBc/Hz at 1 MHz

frequency offset from the carrier frequency over the whole tuning range. The VCO has a tuning range of little more than 177 MHz as summarized in Table 5-II. The measured phase error with TEK TDS4000 is less than 0.6º.

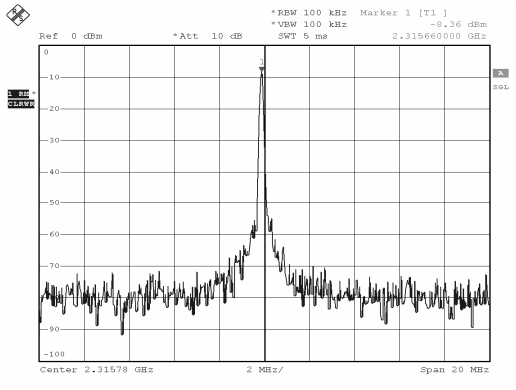


Figure 5-15. TS-QVCO with 4-way center tapped inductor tuned to frequency of 2.315 GHz.

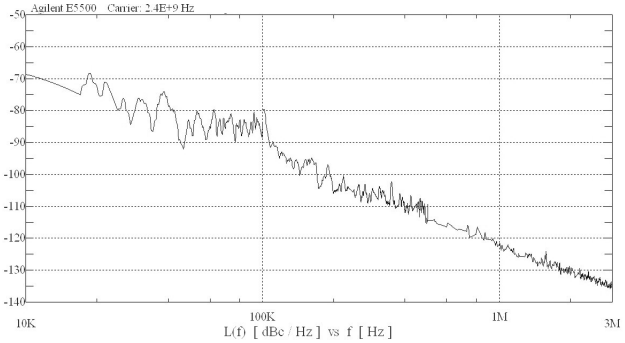


Figure 5-16. Measured phase noise of -122.2 dBc/Hz at 1 MHz offset from 2.345 GHz carrier frequency.

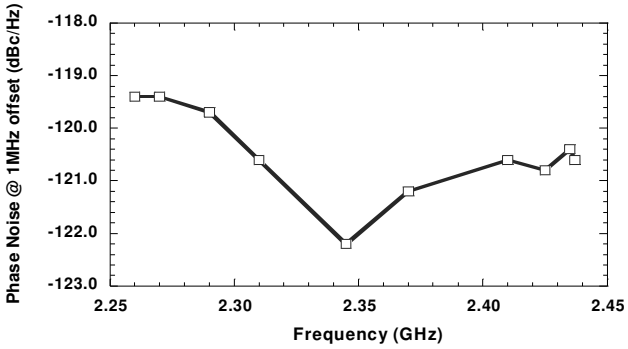


Figure 5-17. Measured phase noise at 1 MHz frequency offset over tuned carrier frequency.

TABLE 5-II
MEASURED RESULTS FOR SCQ-VCO WITH 4-WAY TAPPED INDUCTOR

Tech	*f_0 (GHz)*	*Power (mW)*	*Output Power (dBm)*	*Phase Error*	*Phase Noise (dBc/Hz)*
0.18µm	**2.345**	**10.5**	**-8**	**<0.6°**	**-122.2@1MHz**

TABLE 5-III
QUADRATURE VCO FOM FACTOR COMPARISON

Ref	*f_0 (GHz)*	*Power (mW)*	*Tuning Range*	*FOM (dBc/Hz)*
This Work	**2.345**	**10.5**	**7.5%**	-179.4
[18]	1.8	50	18%	-179
[22]	2.0	11.05	14%	-176
[19]	2.0	11	10%	-175
[20]	2.0	25	15.7%	-165

The FOM factor of -179.4 dBc/Hz for low voltage TS-QVCO with a 4-way center-tapped inductor compares well with other works in Table 5-III but with low power consumption and higher power efficiency.

5.4. Single Phase Low Phase Noise LC VCOs

Single phase LC VCO are the most commonly used VCOs in transceivers even more so than the quadrature VCOs. Significant amount of research have been published about LC VCOs since 1960s, to improve the noise performance at low DC power. There are several differential LC VCO architectures that one can consider for PLL application but there is still some room for innovation and for improved performance. Most common LC VCO architectures are the complementary and PMOS or NMOS -only VCO structures as shown in Figure 5-18.

In the following sub-sections we will discuss the design and the measurement results for several VCOs that are application specific that may not have low phase noise or high FOM factor requirements.

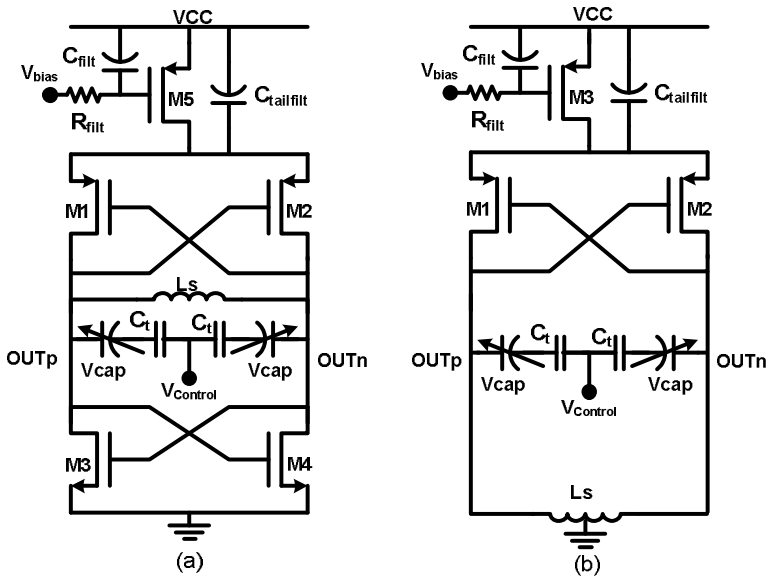


Figure 5-18. (a) Complementary and (b) all-PMOS LC VCO architecture

A. Complementary LC VCO for Neurosensory Application

The RF wireless communication systems such as for the neurosensory and biomedical application require silicon area efficient, low power, and high output power VCO operating in a low voltage environment. With this in mind, a low power and silicon area efficient 5.7 GHz complementary LC VCO (CLC VCO) was designed targeting On-Off Keying (OOK) wireless transmission for neurosensory application. On-Off Keying wireless system (as shown in Figure 5-19) requires a simple transmitter consisting of high isolation switch modulated by baseband data and carrier frequency generated via the VCO.

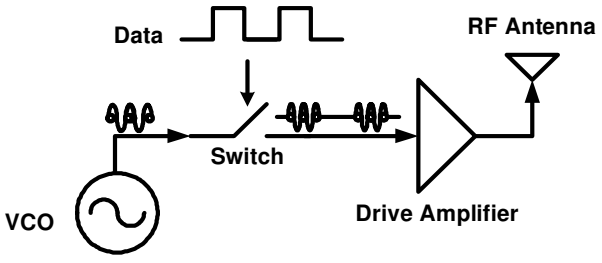


Figure 5-19. Simplified On-Off Keying transmitter with LC VCO

The modulating baseband data is the amplified analog to digital converted (ADC) neurosensory signal recorded from, for example, an animal's brain. Due to the nature of the application, the silicon real estate and power requirements are very important design considerations. In addition, for a reliable short-range communication, to deliver high data rates the output power of the carrier signal generated by the VCO has to be high but at low power consumption. Therefore, the real focus of this work is the development of VCO that is silicon real estate efficient and one with large carrier power.

A complementary LC VCO includes both the PMOS and the NMOS cross-coupled negative-g_m cells, as shown in Figure 5-18(a), contributing total $-(g_{mn}+g_{mp})$ negative resistance at a given bias current. For the same bias current, the NMOS-only or the PMOS-only VCOs, as shown in Figure 5-18(b), can only attain either $-g_{mn}$ or $-g_{mn}$ resistance. Therefore, the complementary LC VCO is power efficient. Another advantage of the complimentary VCO is the faster and symmetrical switching of the cross-coupled FETs which make the VCO less sensitive to noise including the *1/f* or flicker noise. While the tank swing is limited due to two cross-coupled cells for low power application the output power is still high.

The CLC VCO, shown in Figure 5-20, was fabricated in TSMC 0.25-µm digital process. The digital FET layout was manually done to improve the RF performance of the CLC VCO. The octagonal inductor, not available in TSMC 0.25-µm design kit, was designed using ASITIC to realize high *Q*. The CLC VCO is able to achieve measured output power of –3.7 dBm (see Figure 5-21), after compensating for the cable losses and RF probe losses (~2.5 dBm), while consuming only 5mW power over the frequency tuning range. At 600 KHz frequency offset, the VCO achieves -92.75 dBc/Hz phase noise from 5.73 GHz carrier as shown in Figure 5-22. A phase noise analyzer with low noise floor should show the VCO has lower phase noise.

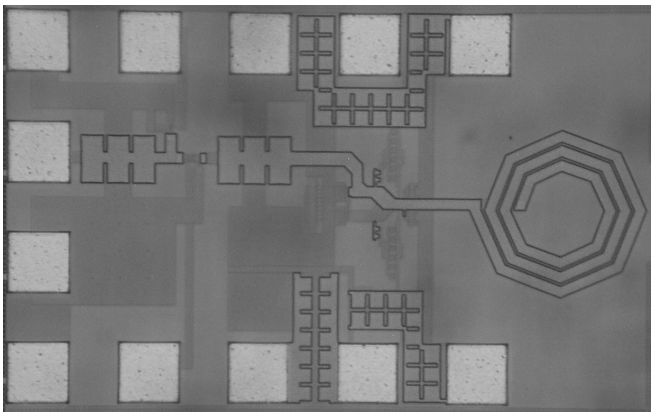


Figure 5-20. On-Off Keying transmitter with proposed complementary LC VCO

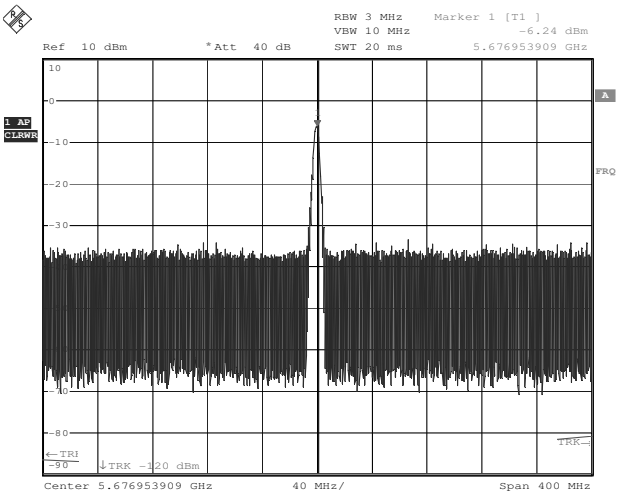


Figure 5-21. Measured output power for CLC VCO with assembly losses (~2.5 dBm) at 5.677 GHz.

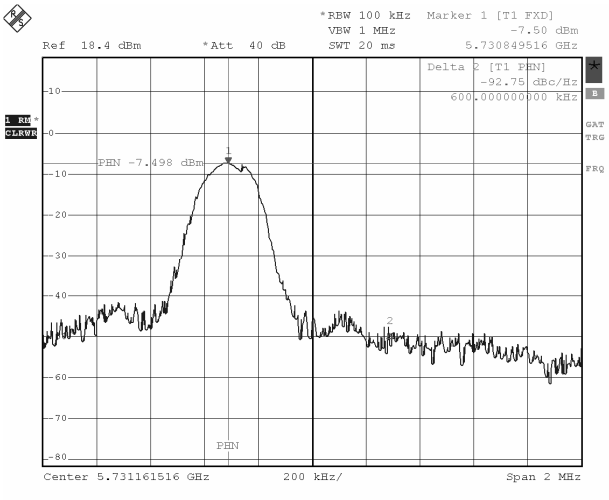


Figure 5-22. Measured phase noise at 600 KHz. at 5.73 GHz center frequency with assembly loss.

B. Novel Ultra Low Power Wide Band LC VCO with 30% Tuning Range

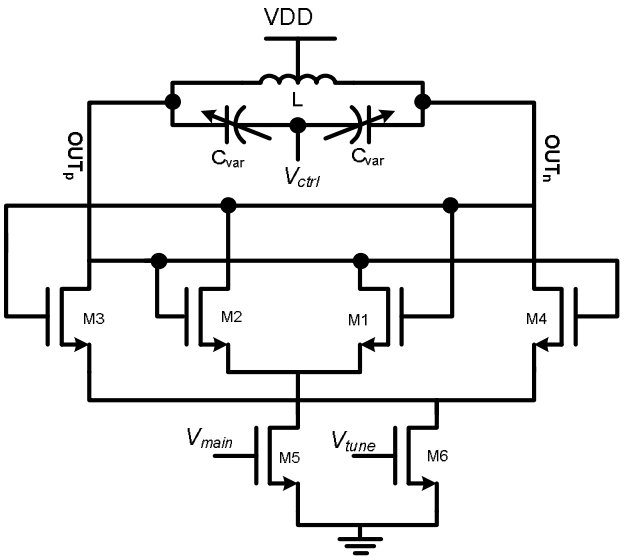


Figure 5-23. An ultra-low power wide tuning range LC VCO

Figure 5-23 shows a novel ultra-low power wide tuning range LC VCO architecture. It consists of two positive feedback cross-coupled MOS cells with independent tunable bias current source. "V_{tune}" control signal, tied to one of the negative g_m cell, is used to extend the tuning of the VCO frequency which is primarily controlled via "V_{ctrl}" control to achieve wide tuning range. The proposed VCO is intended for dual-loop PLL with coarse frequency and fine frequency control. The careful varactor and transistor optimization is done to achieve both low phase noise and large tuning capability. This architecture allows for low harmonic distortion benefiting from linearization of two transconductance cells lowering noise in the $1/f^2$ region of the VCO phase noise characteristic.

The wide tuning LC VCO was fabricated in Jazz 0.18-µm process. The VCO achieves a tuning range of 1.6 GHz covering 4.8 GHz to 6.4 GHz frequency band or 30% tuning range. During the whole tunable range, in simulation, the VCO maintains phase noise between -117dBc/Hz to -122.5 dBc/Hz at 1 MHz offset from the carrier while consuming only 1.2mW of total core power. The VCO DC power can be increased to 2.1 mW to achieve lower (-119dBc/Hz

to -125 dBc/Hz) phase noise performance over the whole tuning range. The VCO operates from a low supply voltage of 1V. The varactor control voltage ranges from 0 V to 2.4 V in Jazz 0.18-μm process, so that is exploited in this design even though the supply is limited to 1 V for the VCO. Table 5-IV summarizes the performance of the proposed LC VCO.

Figure 5-24 shows the micrograph of the wide tuning LC VCO. The measured phase noise of -116.7 dBc/Hz @ 5.87 GHz produces FOM factor of -190 dBc/Hz, which, is very competitive with state-of-the-art LC VCOs as shown in Figure 5-25. Agilent phase noise interface was used for the phase noise measurement.

TABLE 5-IV
WIDE BAND VCO PERFORMANCE SUMMARY

	Simulation	Measurement
Nominal Oscillation Frequency	4.8 ~ 6.4 GHz : (0-2.5V) 5.3 ~ 5.8 GHz : (0.3-1.5V)	4.8 ~ 6.2 GHz : (0-2.5V)
Tuning Range	30%	26 %
Supply voltage	1.0 V	1.0 V
Power consumption (core)	1.2 mW	1.4 mW
Phase noise @ 1MHz (1.2mW) Phase noise @ 1MHz (2.1mW)	-117 dBc/Hz to -122.5 dBc/Hz -119dBc/Hz to -125 dBc/Hz	-113 dBc/Hz to -116.7 dBc/Hz
FOM (1.2mW)	-195 dBc/Hz	-190 dBc/Hz

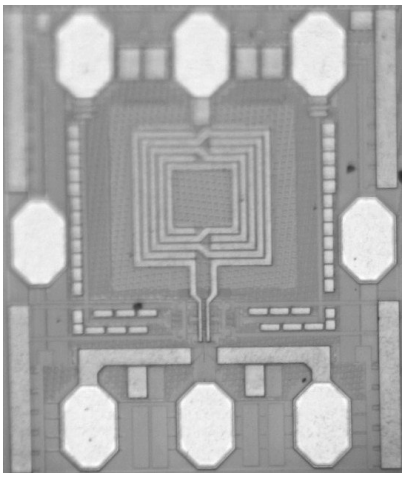


Figure 5-24. Micrograph of ultra-low power wide tuning range LC VCO

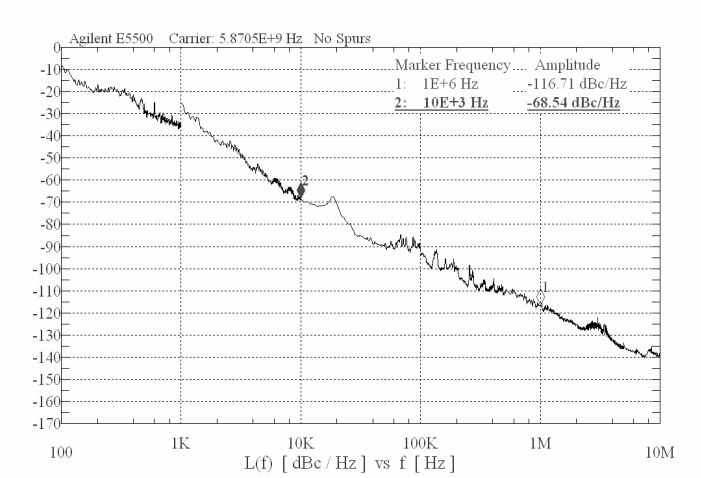


Figure 5-25. Measured phase noise @1 MHz offset from 5.87GHz carrier for the wide tuning VCO

C. Novel Low Phase Noise Load Independent Switched LC VCO

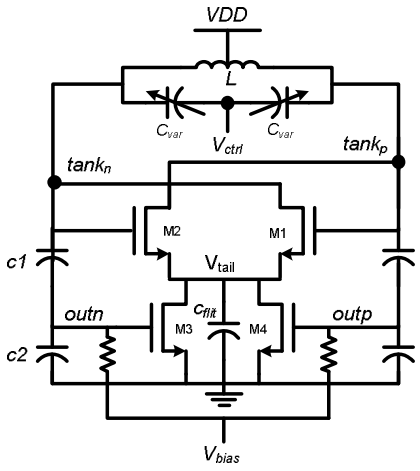


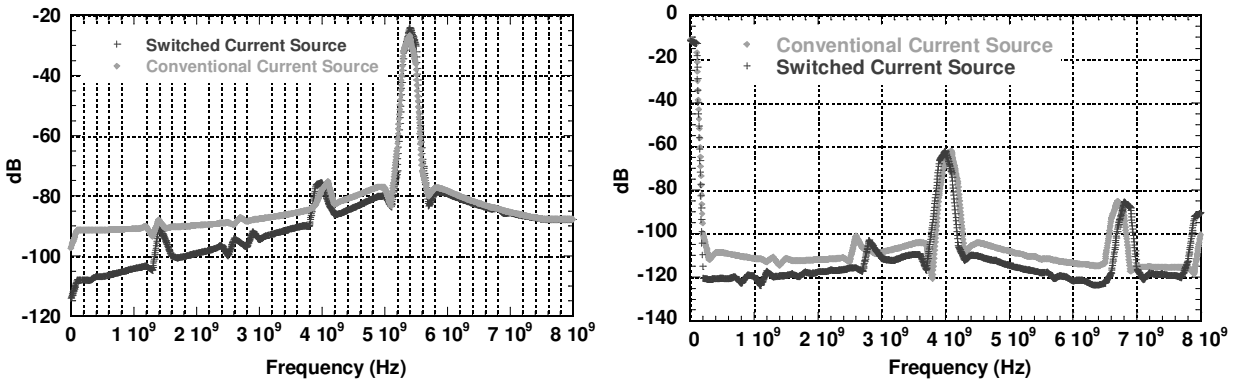
Figure 5-26. A low phase noise load independent switched LC VCO

A novel low phase noise load independent switched LC VCO is proposed in Figure 5-26. In many applications the VCO is required to drive several output loads and is subject to load pushing, and thus, conventionally VCO buffer is used to isolate VCO tank from the load. Loading can also degrade the tank loaded *Q* and vary the VCO performance. For low power application, the power level of the VCO buffer should be tailored to the drive power requirements which may mean different sized buffers. In conventional VCO, the VCO performance needs to be tweaked if the load buffer is changed. To avoid this problem, the

proposed LC VCO is made load independent, i.e., the load neither degrades the loaded Q nor changes the performance and frequency of the VCO. This is done with impedance transformation through capacitor, c_1, which is considerably smaller than capacitor, c_2. Adding extra load to c_2, causes insignificant change in VCO performance since the tank capacitance is not affected by c_2.

$$c_{tank} = c_{var} + c_{par} + \frac{c_1 c_2}{c_1 + c_2}\bigg|_{c_1 << c_2} \approx c_{var} + c_{par} + c_1 \tag{5.16}$$

The output of the VCO is now fed-back to switch the current source FETs, biased in the saturation region, to make it a dynamic current source. There are two advantages in doing this; one is that the VCO fundamental signal is boosted by this additional feedback signal as can be seen from Figure 5-27 and other is the noise shaping occurs, both of which, lower the phase noise of the VCO. Figure 5-27(a) shows the discrete fourier transform (DFT) of output signal with and without the switched current source. The spectral shaping at the output is due to noise shaping of the tail current source seen in Figure 5.27(b). The dynamic switching also lowers the flicker noise slightly, since, switching clears some memory effects in the channel. The switching of the cross-coupled transistor is also increased with switched current source.



(a) (b)

Figure 5-27. (a) DFT of VCO output shows higher output power and lower noise (b) DFT of the tail node of the current source shows noise shifting and noise shaping.

The load independent VCO shown in Figure 5-28 was fabricated in TSMC 0.18-µm process. The phase noise at 5.36 GHz carrier at 1 MHz offset is -121.3 dBc/Hz at 3.04 mW DC power consumption (see Figure 5-29). The FOM factor of -191.1 dBc/Hz is achieved making the proposed VCO competitive with state-of-the-art. The performance is summarized in Table 5-V.

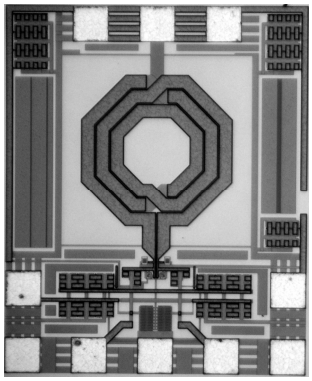


Figure 5-28. Micrograph of low phase noise load independent switched LC VCO

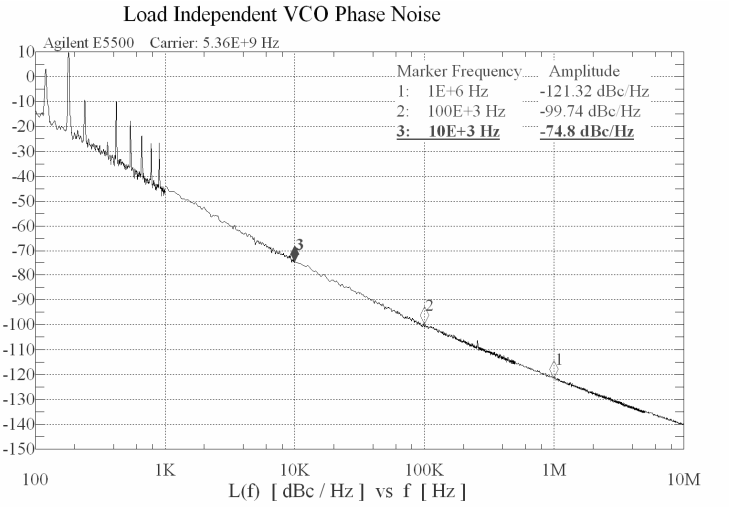


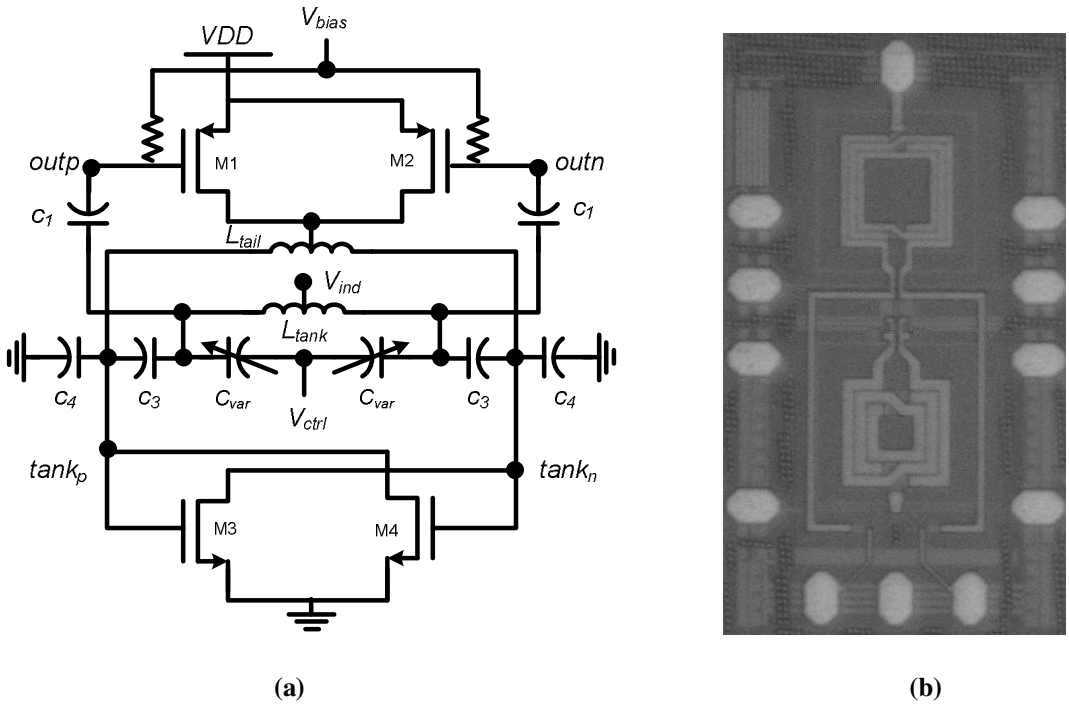
Figure 5-29. Measured phase noise of -121.3 dBc/Hz @1 MHz offset from 5.36GHz carrier

TABLE 5-V
LOAD INDEPENDENT SWITCHED LC VCO PERFORMANCE SUMMARY

	Measurement
Oscillation Frequency	5.2 ~ 5.45 GHz : (0V-1.2V)
Supply voltage	1.2 V
Power consumption	3.04 mW
Phase noise @ 100 KHz @ 1MHz	-99.7 dBc/Hz -121.3 dBc/Hz
FOM @ 5.36 GHz	-191.1 dBc/Hz

D. Novel Low Phase Noise Tapped-Load Independent Switched LC VCO

A variation of the load independent switched VCO using a PMOS current source and harmonic filtering is also proposed. Figure 5-30 shows the schematic of the proposed LC VCO and its micrograph. The architecture includes capacitor tapping of the tank to reduce swings at the drain of the cross-coupled FETs to keep transistors M1, M2, M3 and M4 in saturation and improve the loaded *Q*. The DC level of the varactor can be adjusted using V_{ind} for re-configurability and for extending the tuning range.



(a) **(b)**

Figure 5-30. (a) Schematic and (b) Micrograph of novel tapped load independent switched LC VCO

Modifying V_{ind} changes the DC operating region for MOS varactors which helps shift the tuning transfer curve for added re-configurability. The switched current source is driven directly via capacitor c_1 *to* keep output power high at *outn* and *outp* nodes. The capacitor c_3,and c_4 reduces the drain swing of the cross-coupled FET by factor of $c_4/(c_3+c_4)$ to maintain all FETs in the saturation region to preserve the loaded *Q*. A switched PMOS current source is also implemented since it's *1/f* noise is lower than the NMOS current source.

The tapped load independent VCO shown in Figure 5-27 was fabricated in Jazz 0.18-µm process. The table 5-VI summarized the measured results for the VCO. The measured phase noise is -122.42 dBc/Hz at 1 MHz offset from 5.47 GHz carrier. The VCO consumes 5mW DC power from 1.2V supply. The measured phase noise at 100 KHz offset of -102 dBc/Hz is better than the load independent VCO presented in section 5.3.C. The primary reason is due to lower flicker noise corner in the PMOS current source. The VCO consume 1.5 mW more power than in the simulation but its FOM factor of -190.2 dBc/Hz is still very competitive.

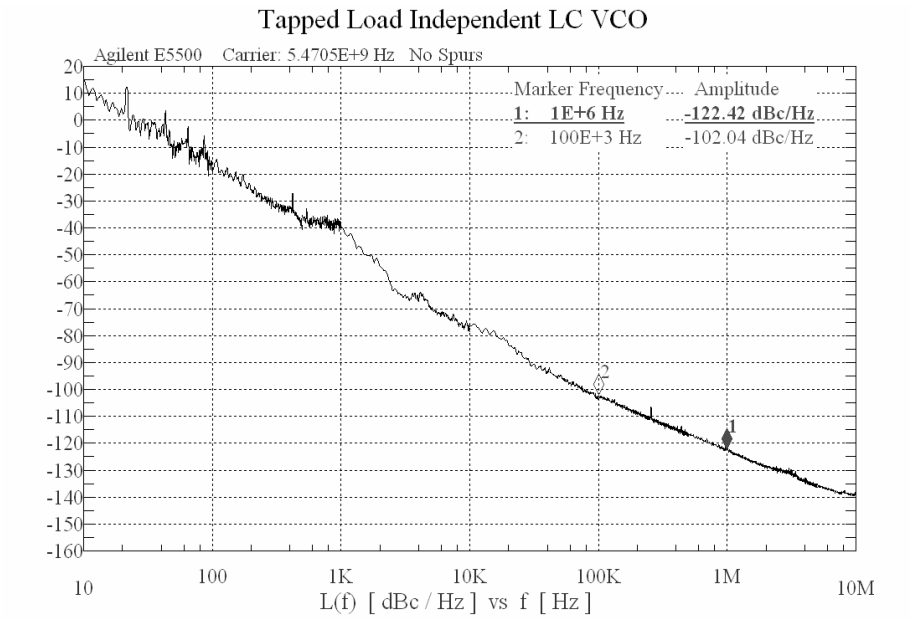


Figure 5-31. Measured phase noise of -122.4 dBc/Hz @1 MHz offset from 5.47GHz carrier

TABLE 5-VI
TAPPED LOAD INDEPENDENT SWITCHED LC VCO PERFORMANCE SUMMARY

	Measurement
Oscillation Frequency	5.3 ~ 5.7 GHz : (0V-1.2V)
Supply voltage	1.2 V
Output Power	-10 dBm
Power consumption	5 mW
Phase noise @ 100 KHz @ 1MHz	-102 dBc/Hz -122.4 dBc/Hz
FOM @ 5.47 GHz	-190.2 dBc/Hz

5.4. Proposed Load Independent Switched LC VCO for PLL

Based upon simulation and measurement data, the load independent switched LC VCO has the highest FOM factor of all VCOs presented in this thesis work, and therefore, is a good candidate for the low jitter PLL. Furthermore, it has the smallest silicon real estate requirement. An optimized load independent switched LC VCO is designed in the Jazz 0.18-µm process for the proposed fast settling and low jitter PLL as shown in Figure 5-32. The peaking amplifier is used as VCO buffer as shown in Figure 5-33. Table 5-VII summarizes the performance of the post layout simulation. Figure 5-34 shows the frequency and phase noise variation over the valid control voltage.

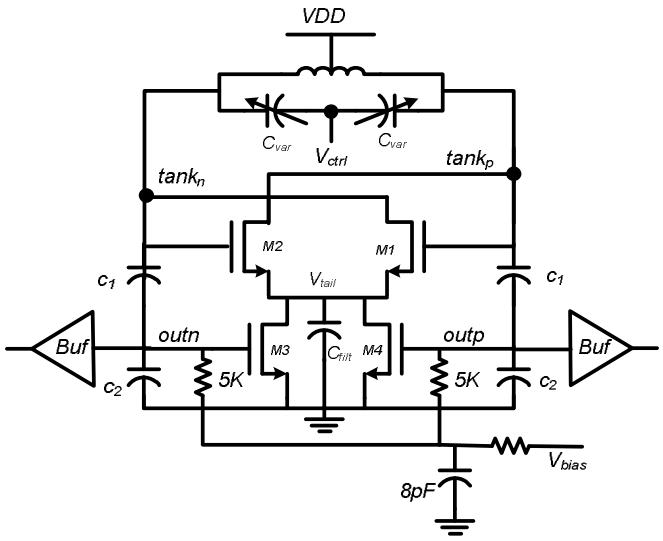


Figure 5-32. Proposed low phase noise load independent switched LC VCO for low jitter PLL

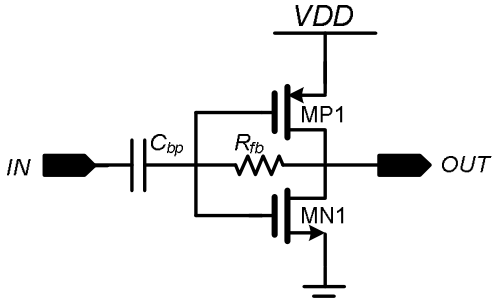


Figure 5-33. Low power VCO peaking amplifier (*Buf*) in Figure 5-32.

TABLE 5-VII
LOAD INDEPENDENT SWITCHED LC VCO FOR LOW JITTER PLL PERFORMANCE SUMMARY

	Simulated
Oscillation Frequency	5.1 ~ 5.3 GHz : (0V-1.2V)
Supply voltage	1.2 V
Output Power	-10.5 dBm
Power consumption	3.04 mW
Phase noise Min Max	-124 dBc/Hz -120 dBc/Hz
FOM @ 5.36 GHz	<-190 dBc/Hz
VCO gain (K_v)	200MHz/V

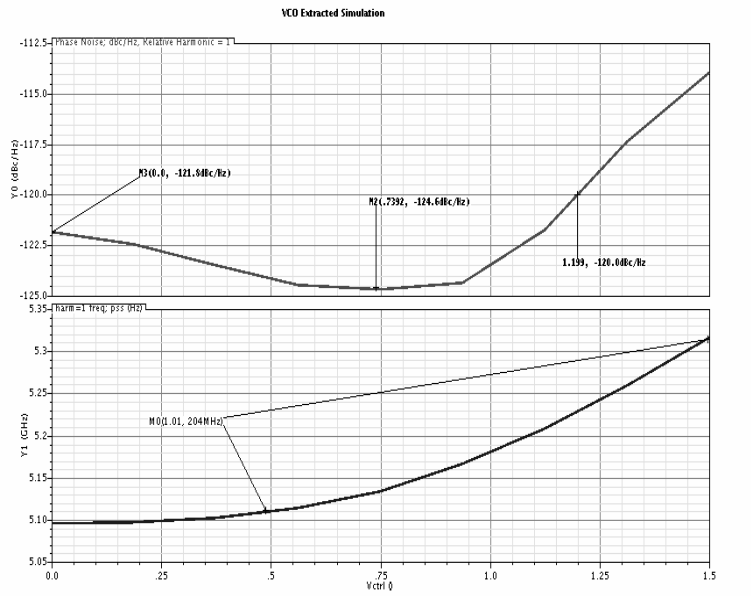


Figure 5-34. Post layout simulation of frequency and phase noise over control voltage (0V to 1.2V)

The phase noise varies between -124 dBc/Hz and -120 dBc/Hz at 3mW power consumption. The worst case FOM factor is -190 dBc/Hz.

CHAPTER SIX

6.0. Proposed Fast Settling and Low Jitter PLL Architecture

We have built a premise for the design of fast settling and low jitter PLL architecture in chapters 1-5 that included detail discussion of theory, circuit design, simulation and measurement results of each fundamental component. We have gone to great lengths to describe the PLL dynamics in-terms of bandwidth, settling time and noise transfer functions, all of which, is used to come up with a new fast settling and low jitter PLL architecture shown in Figure 6-1.

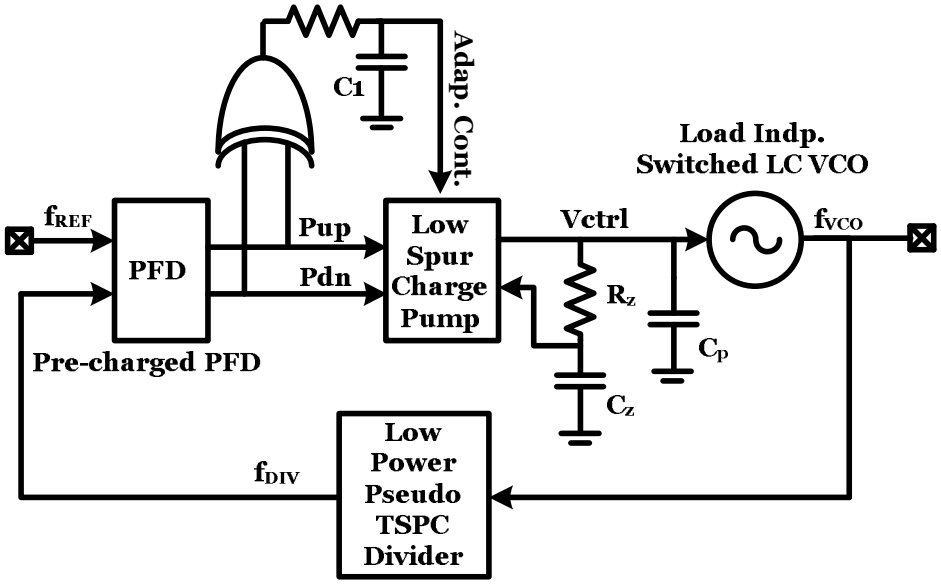


Figure 6-1. Proposed Integer-N fast settling and low jitter PLL

The proposed integer-N PLL consists of pre-charged PFD with fast reset delay to achieve minimum pump-up and pump-down pulse, very low spur and glitch compensated dynamic replica bias current steering charge-pump, load independent switched LC VCO with high FOM factor and very low phase noise, a dynamic low power divider and an adaptive bandwidth control circuitry to achieve fast settling and fast locking. Fully integrated PLL is built as a prototypical design to meet targeted specification shown in Table 6-I. The specifications are challenging but do not specifically cater to any standard.

TABLE 6-I
FAST SETTLING AND LOW JITTER PLL TARGETED SPECIFICATIONS

Parameter	Description	Min	Max
f_{REF}	Reference Frequency	318 MHz	350 MHz
BW	Closed Loop Bandwidth	1 MHz	4 MHz+
Peaking	Closed Loop Magnitude peaking		< 3 dB
Power	PLL Total Power VCO Divider PFD/CP VCO Buffer		< 10 mW 3 mW 2.75 mW 1.2 mW 3mW
T_{lck}	PLL Lock time (Max Freq Deviation)		< 1.5μS
Rs	Reference Spurs		< –60 dB
P_{noise}	VCO Phase Noise@ 1MHz offset		–120 dBc/Hz

6.1. Novel Adaptive Bandwidth Circuit for Faster Settling Time

In section 2, we showed the an PLL settling time, t_s,

$$t_s = \begin{cases} \dfrac{1}{\zeta\omega_n}\ln\dfrac{\Delta f}{\alpha f_o\sqrt{1-\zeta^2}} & 0<\zeta<1 \\ \dfrac{1}{\zeta\omega_n}\ln\dfrac{\Delta f}{\alpha f_o} & \zeta=0 \\ \dfrac{1}{(\zeta-\sqrt{\zeta^2-1})\omega_n}\ln\dfrac{\Delta f(\sqrt{\zeta^2-1}+\zeta)}{\alpha f_o\sqrt{\zeta^2-1}} & \zeta>1 \end{cases} \qquad (6.1)$$

is a function of damping factor, ζ, natural frequency, ω_n, frequency step, Δf, and settling accuracy, α [8]. In maximizing the product $\zeta\omega_n$ we can achieve fast settling time and if we take (2-16) and (2-14) we find $\zeta\ \omega n \approx \omega_c/2$, i.e., wider the PLL loop bandwidth faster the setting time. The bandwidth and settling time are related, and therefore, for fast settling is possible with large PLL bandwidth. However, the bandwidth of the PLL cannot be arbitrarily large and it has limitation dictated by the noise requirements of the PLL. Finding an optimum design with both

fast setting and low noise without any additional scheme still produces PLL with settling time in the order of couple of microseconds. This is not adequate to meet the targeted specification in Table 6-I. An adaptive bandwidth approach that allows both optimized low noise and low jitter performance while achieving fast settling time is proposed.

For the PLL linear model in Figure 6-2, we have shown in (2.16), re-written here as (6.2), the bandwidth or the crossover frequency is a function of charge-pump current, I_{cp}.

$$\omega_c = \sqrt{\omega_z \omega_p} = \omega_z \sqrt{\frac{C_z}{C_p} + 1} = \frac{I_{pump} K_{VCO} R_z C_z}{C_z + C_p} \approx \frac{\omega_n^2}{\omega_z} \tag{6.2}$$

Increasing the charge-pump current increases the loop bandwidth of the PLL. This is significant in that if we are able to adaptively change the current, then, we can achieve adaptive bandwidth.

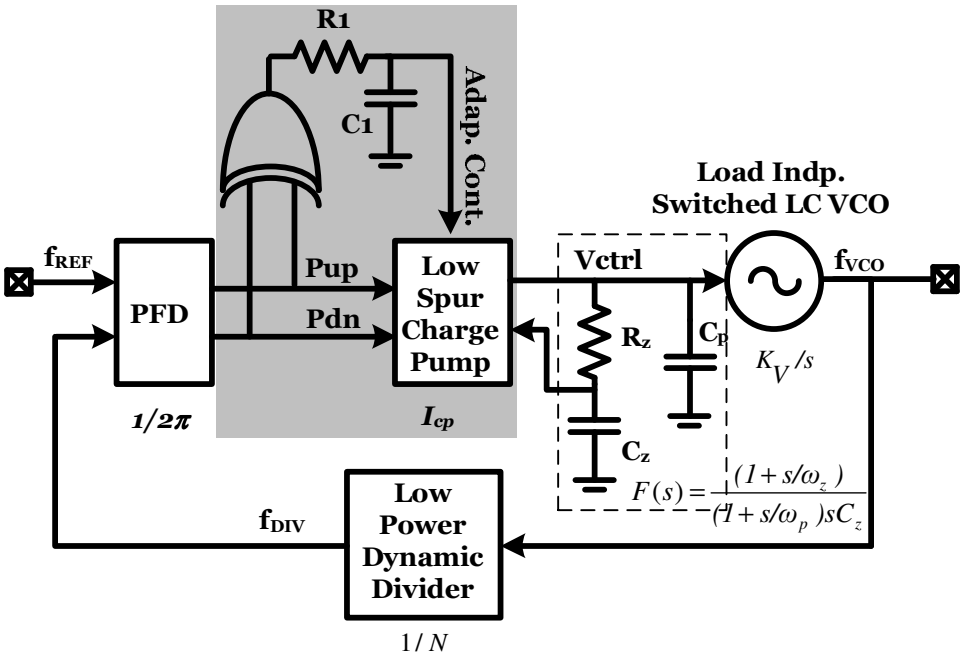


Figure 6-2. Linear model for the PLL with novel adaptive bandwidth control circuit

Typically adaptive bandwidth control is implementing with second PFD or FD circuitry in the PLL. Secondary PFD or FD is used to detect the frequency or phase and frequency error between the feedback and reference signals to change the loop bandwidth for fast acquisition of

frequency and phase. This approach, however, has some short comings in terms of switching noise, larger silicon real estate requirements and extra power consumption. The adaptive bandwidth control circuit can be made far simpler and low noise knowing the magnitude of the phase and frequency error is already available at the PFD output.

A novel adaptive bandwidth control circuitry is proposed. A minimum sized XOR gate which adds very little to the parasitic capacitance at the output of the PFD and can detect the magnitude of this phase and frequency difference. The difference can be integrated with a simple RC filter to dynamically control the charge-pump current. If there exits a large phase and frequency error, the charge-pump current can increase four to five fold that of nominal value in the locked case optimized for PLL noise. This increase in current results in adaptive increase in PLL loop bandwidth, and therefore, faster frequency and phase acquisition. When the magnitude of the phase difference is small, due to the non-linear IV characteristic of the PMOS transistor, the current is reduced non-linearly and the bandwidth approaches nominal value without affecting stability. This approach is low noise and ultra-low power, since, the minimum sized XOR can be made to consume less than 50uW of total power and it has very wide bandwidth. Figure 6-3 shows the proposed XOR structure.

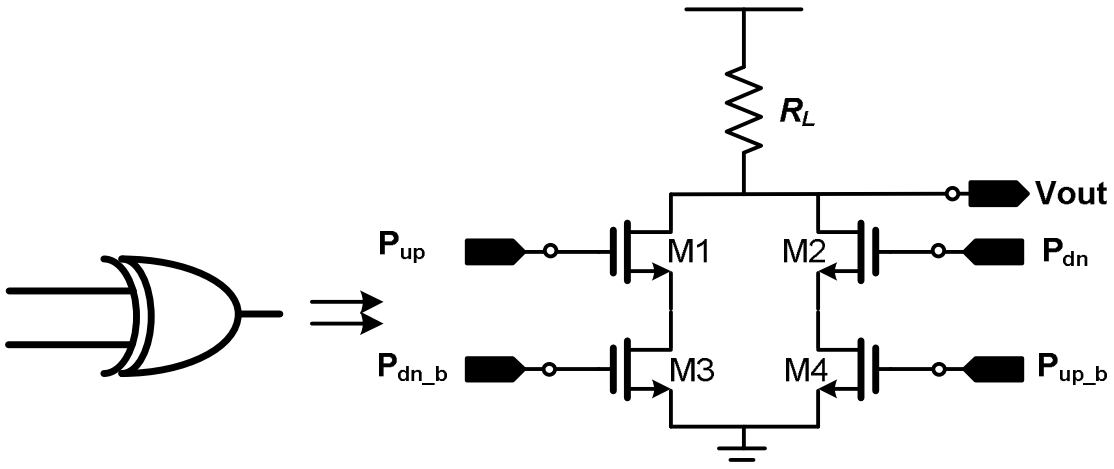


Figure 6-3. Minimum sized XOR gate for adaptive bandwidth control

6.2. Fast Settling and Low Jitter PLL Loop Dynamics

Adaptive bandwidth via adaptive change in charge-pump current allows for faster settling with proper consideration of the PLL loop dynamics. Charge-pump current affects the natural frequency, ω_n, and the damping constant, ζ, of the PLL response both of which affect the loop stability and peaking that results in random jitter in the PLL as discussed in Chapter 2. For the proposed integer-N PLL, an optimum damping constant can be selected in both current boost phase and in the nominal case, to achieve both fast settling time and to maintain loop stability. Figure 6-4 shows the plot of phase margin, a function of damping factor, and its role in settling time for the nominal I_{cp}.

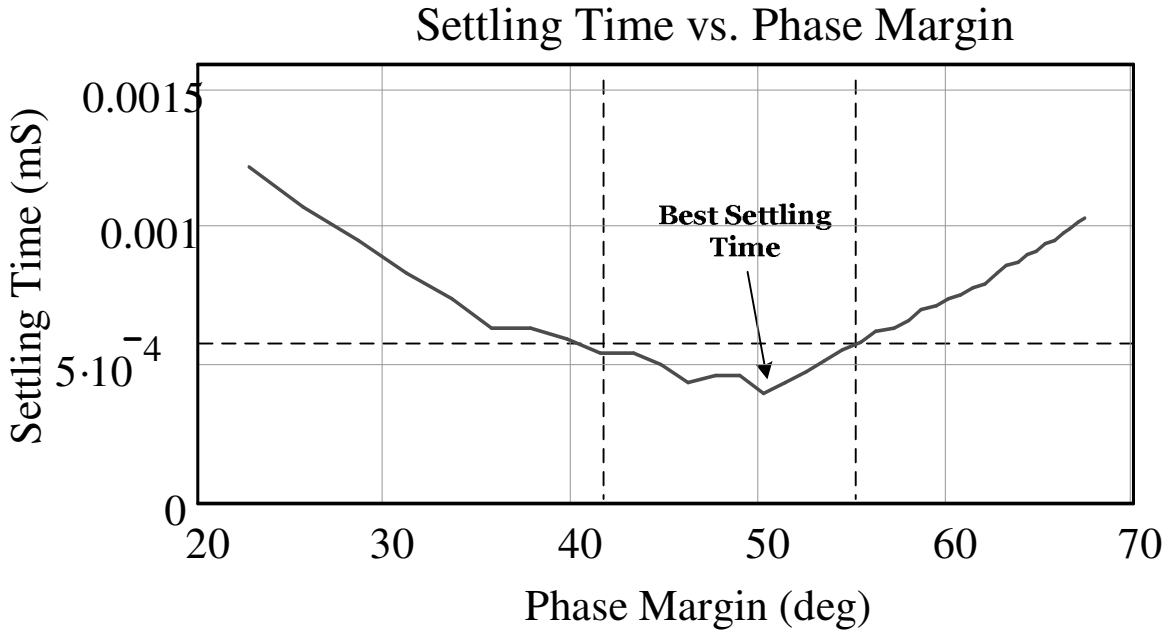
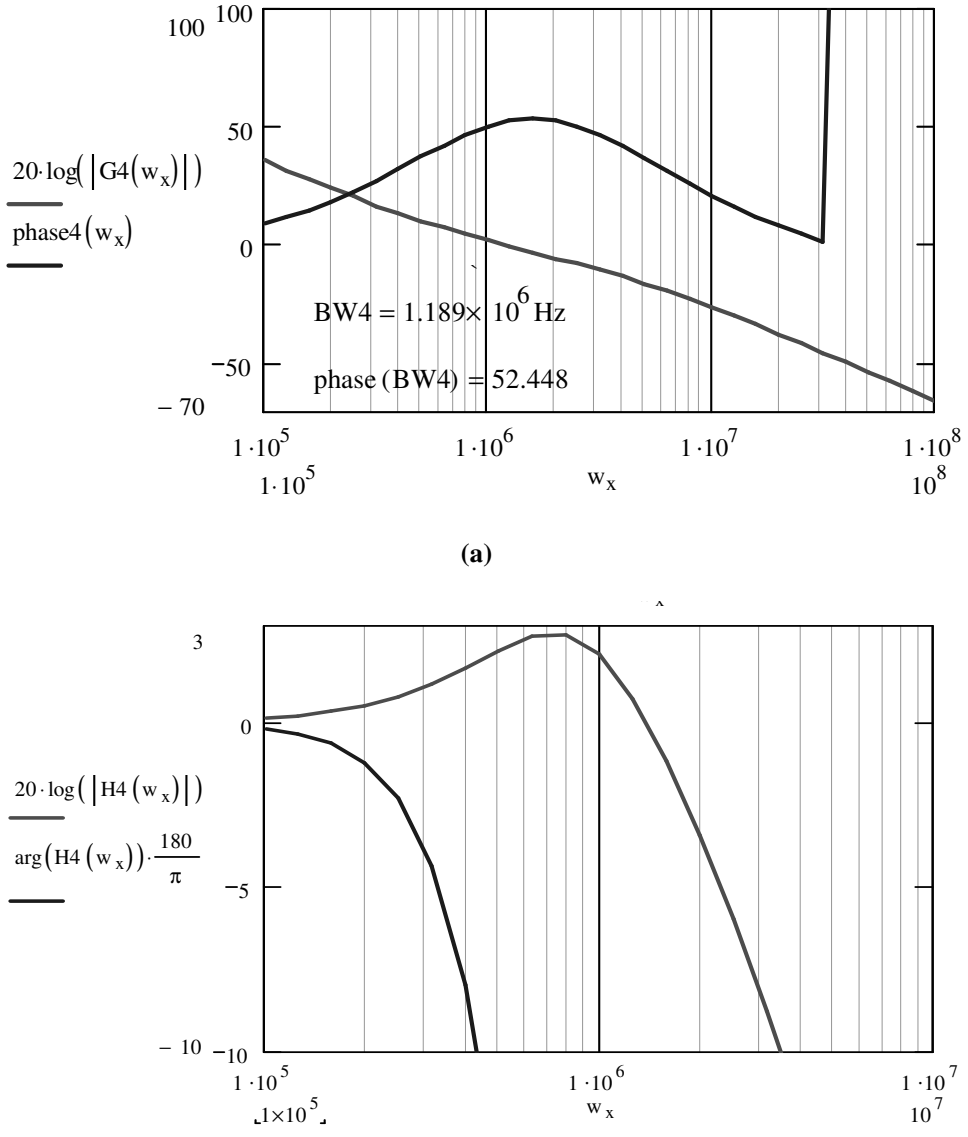


Figure 6-4. Settling time versus phase margin (PM) for nominal charge-pump current in PLL.

The stable PLL requires the phase margin should be always better than 42 degrees. From Figure 6-4, the phase margin between ~ 42° to 55° allow for fast settling time with the best settling time is achieved for PM is near 51°. Boosting current during the fast acquisition degrades the phase margin, therefore, it is determined that phase margin of near 52.5° in the nominal case

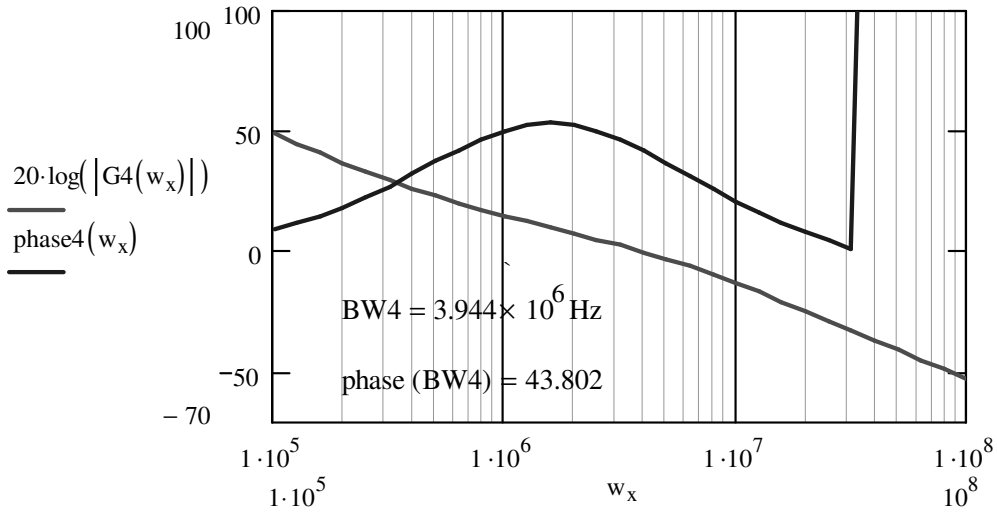
is optimal solution such that during the boost phase the worst case PM is 43.8º. Figure 6-5 shows the open and closed loop magnitude and phase response for the proposed PLL in the nominal case and while Figure 6-6 shows the loop response for the maximum boost current. The PLL bandwidth is nominally set to 1 MHz with PM of ~52.5º and in the boost phase, the bandwidth can increase up to 4 MHz with PM ~ 43.8º. The peaking which adds RMS jitter is below specified 3 dB level.



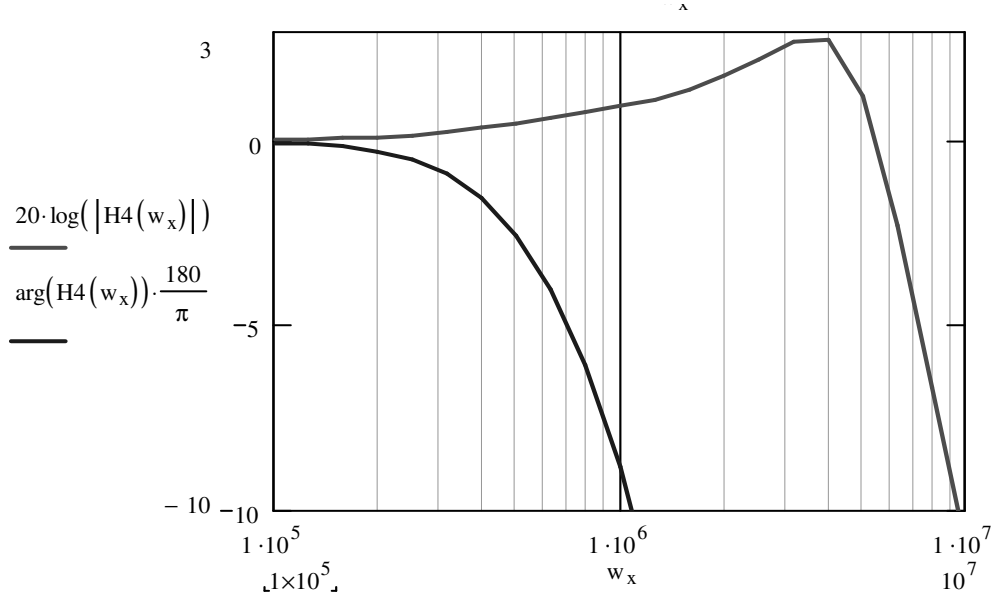
(a)

(b)

Figure 6-5. (a) Open and (b) Closed loop magnitude and phase response for nominal PLL operation



(a)



(b)

Figure 6-6. (a) Open and (b) Closed loop magnitude and phase response for maximum boost current in PLL

Figure 6-7 shows the PLL response to frequency step of 20 MHz. It shows the PLL settling time is within 700ns and frequency error reduces to below 10 KHz in less than 500ns. For most application settling time is defined for frequency error below 50 KHz [23]. Due to non-linear current in the charge pump, the adaptive bandwidth control is also non-linear and follows

PMOS IV characteristic curve. Due to this, the settling time for frequency error below 10 KHz should be greater than 500ns but less than 700ns.

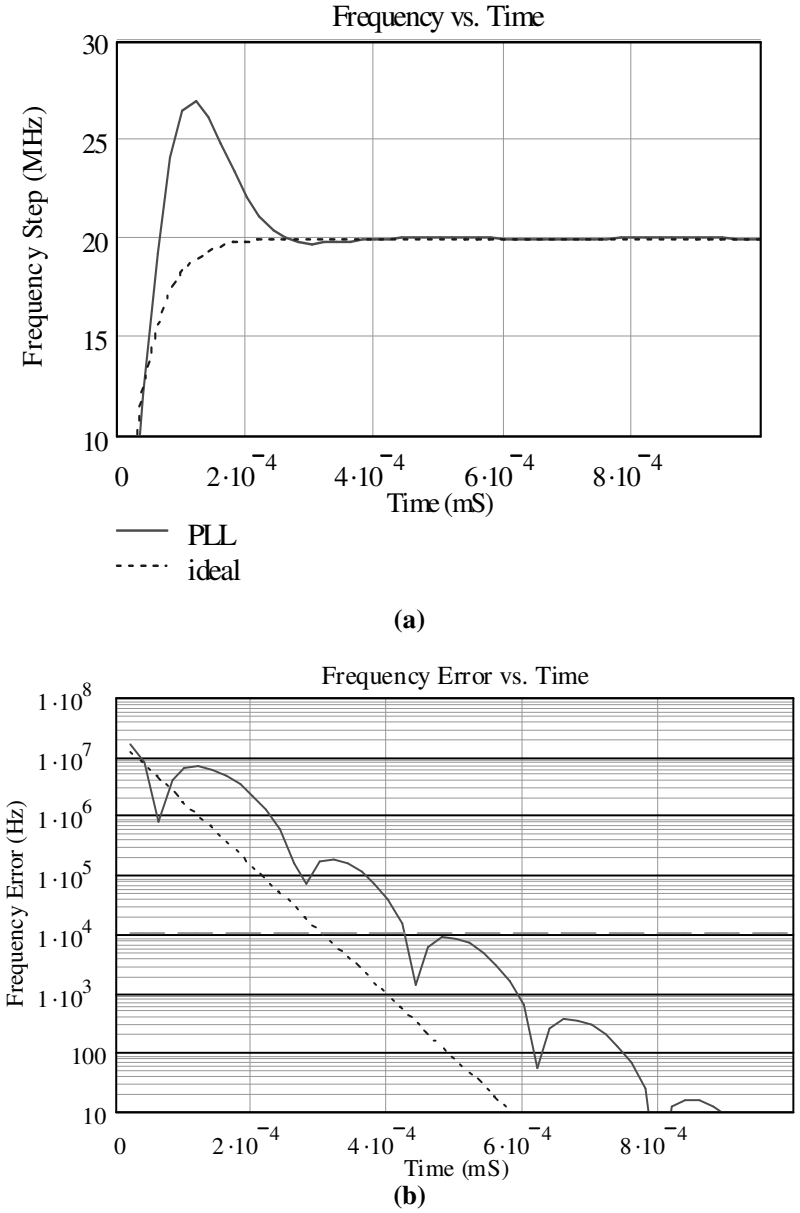


Figure 6-7. (a) Settling time (b) Frequency error PLL response with 20 MHz frequency step

6.3. Very Low Power Dynamic Frequency Divider

To meet the low power criteria for the proposed fast settling and low jitter PLL, a low power divider is a major concern since it typically is the most power hungry block in the PLL.

The front-end of the frequency divider has to be faster than the maximum VCO frequency and because of that it consumes significant amount of power, especially in low f_t process. Typically, the front-end of the frequency divider is a divide by 2 operation implemented with fast flip-flop (FF). Figure 6-8 shows the differential current mode logic (CML) D-latch commonly used for divide by 2 operations in high frequency PLL design. The CML structure is inherently fast and is largely noise insensitive, however, they consume a lot of power due to its static current. In 0.18-μm process, a single CML FF consumes roughly 3mW power to attain 6 GHz bandwidth. The later divider stages also consume power, and thus, for sub 10mW PLL this is out of consideration.

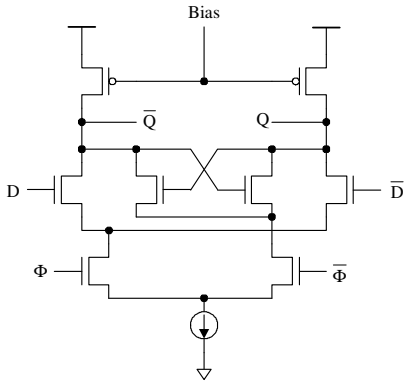


Figure 6-8. Differential current mode logic (CML) latch

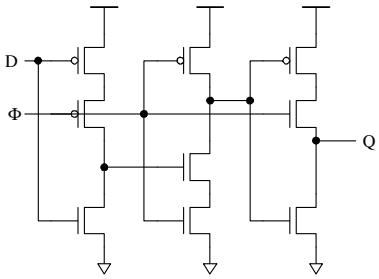


Figure 6-9. (a) Conventional pre-charged TSPC flip-flop

Another FF topology uses pre-charged TSPC flip-flop, shown in Figure 6-9, which are not as fast as CML FFs and are single ended. A conventional TSPC FF consists of three

transistor stack which limits it high frequency operation. In 0.18-μm process, a single CML FF consumes a lot of power to reach 6 GHz bandwidth.

In order to meet the power specification, a pseudo TSPC FF is used. It is a pseudo TSPC because it sheds one pre-charge FET to realize a FF that only has two transistor stacks as shown in Figure 6-10. Having only two transistor stack makes the FF very fast and since it is dynamic, it has very little power consumption and is suitable for our proposed PLL.

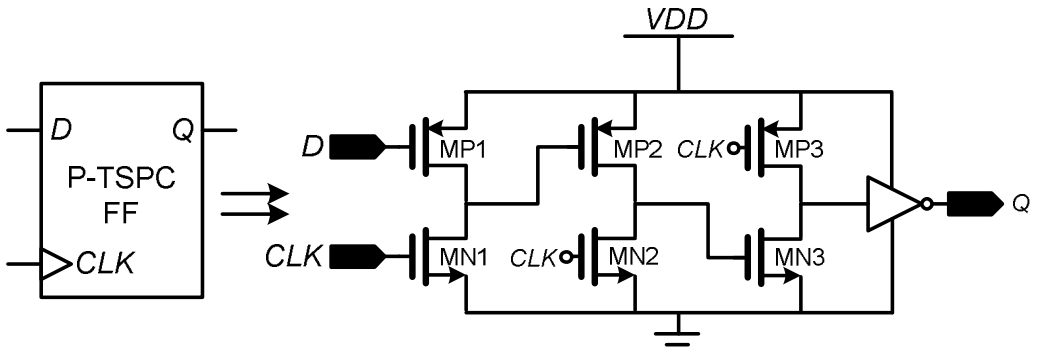


Figure 6-10. Low Power pseudo TSPC flip-flop

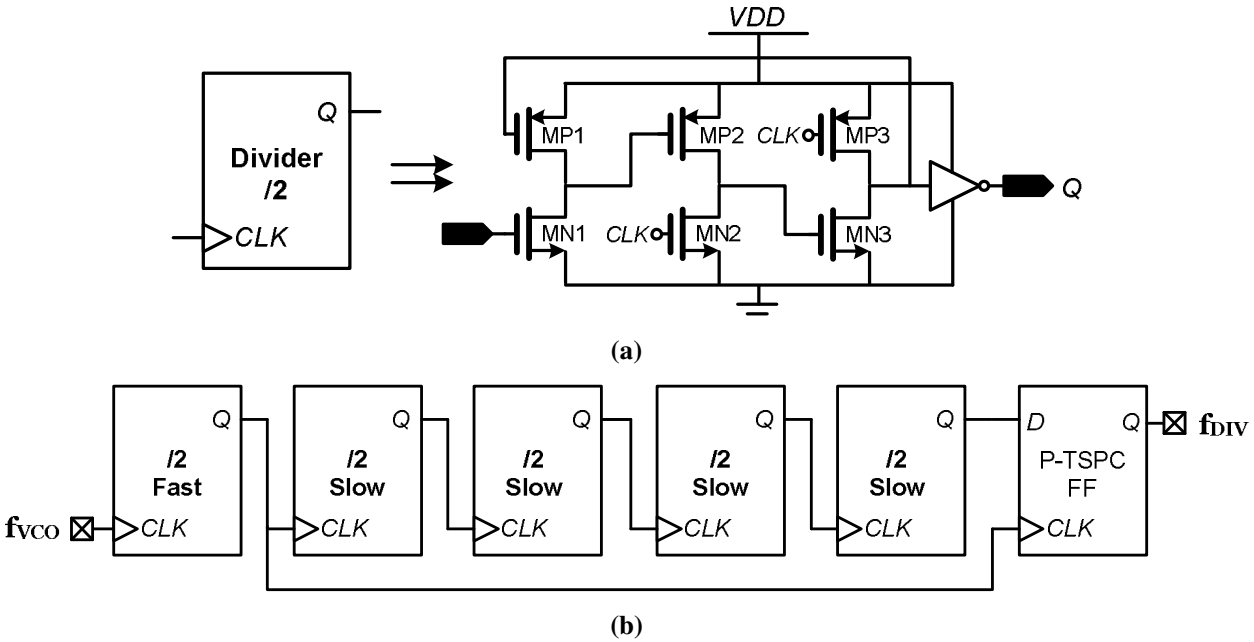


Figure 6-11. (a) Single divide by 2 pseudo-TSPC implementation and (b) Divide by 16 implementation with output sampling using half-rate clock to remove accumulation jitter in the PLL

Figure 6-11 (a) shows a single divide by 2 circuit and Figure 6-11(b) shows the divided by 16 frequency divider with re-timed output to reduce accumulation jitter in the PLL. The total power consumption for the divider is about 2.75mW from a 1.5V supply.

6.4. Low Power Fast Settling and Low Jitter PLL Performance

Fully integrated low power fast settling and low jitter PLL was design in the Jazz 0.18-µm process. Figure 6-12 shows the *0.784 mm*^{2} micro-graph of the proposed phase locked loop. For improved noise performance, in the layout, all digital block were surrounded with PTAP and NTAP ground rings. In addition, double deep-trench rings are used to isolate noise sensitive analog and RF section form the digital. All analog block use wide PTAP guard rings that are surrounded with double deep trench rings for good noise isolation.

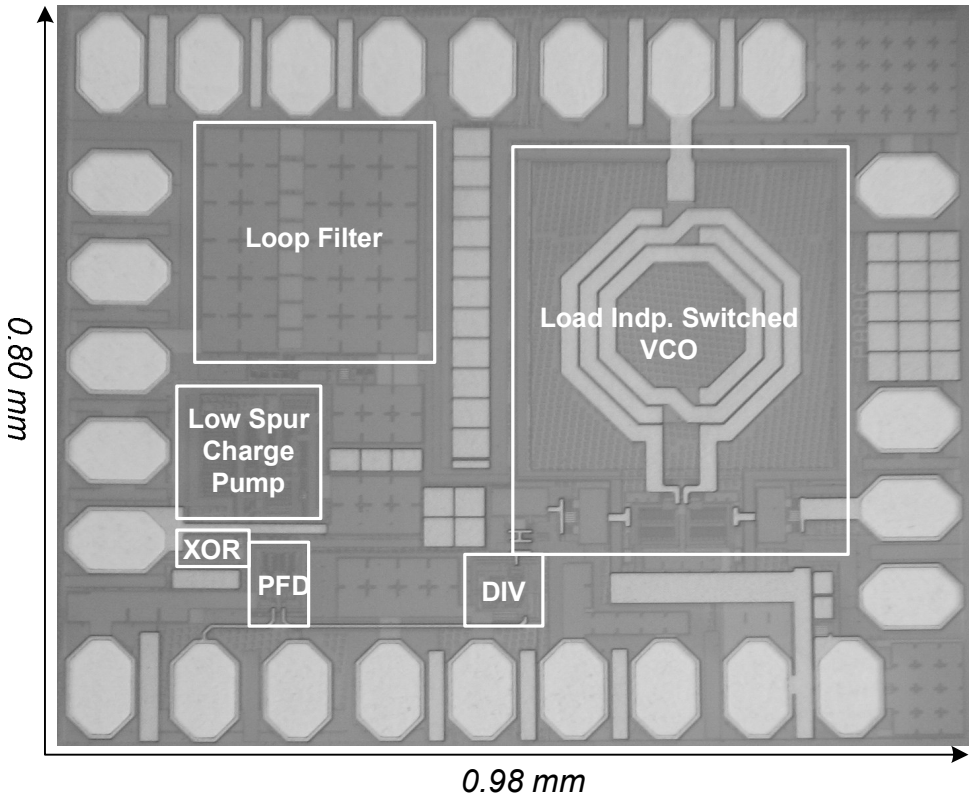


Figure 6-12. Micrograph of the proposed low power, fast settling and low jitter PLL

The performance summary for the PLL is tabulated in Table 6-II. The proposed PLL meet all targeted specification in Table 6-I and the data presented are worst case numbers for jitter and phase noise in the packaged simulation assuming 2.5mm bondwire length. Extensive post-layout simulation was done for the PLL to insure first time success.

TABLE 6-II
LOW POWER, FAST SETTLING AND LOW JITTER PLL PERFORMANCE

Parameter	Description	Typical	Max
BW	Closed Loop Bandwidth	1 MHz	4 MHz+
Power	PLL Total Power VCO Divider PFD/CP VCO Buffer		< 11 mW 3 mW 2.75 mW 1.2 mW 4mW *
T_{lck}	PLL Lock time (Max Deviation) For 20 MHz Step		< 1.7µS <700ns
Rs	Reference Spurs	< – 70 dB	< –64 dB
P_{noise}	VCO Phase Noise@ 1MHz off.	–122 dBc/Hz	–120 dBc/Hz
RJ	RMS Jitter	< 0.7 ps	<2 ps
DJ	Deterministic Jitter w/ 60 mVp-p noise@ f_{ref} on all supplies & 10 mVp-p noise on all DC bias		7 ps
f_{ref}	Reference Frequency	318 MHz	350 MHz
P_{gain}	Closed Loop Magnitude Peaking		<3 dB

*VCO buffer power consumption is kept higher for margin.

Figure 6-13 shows a post layout simulation of the proposed PLL without noise and package. The best case spur suppression is about 85 dB at 5.45 GHz carrier frequency which shows robustness of CP design. The peak to peak jitter, measured with eye diagram, is below 200fs and the RMS jitter is below 300fs. The PLL locks within 1.1us for the maximum frequency deviation. This shows, in noise-less environment, the PLL performance is very good.

In reality, significant noise exists in the PLL and for measurement PLL is packaged. Figure 6-14 shows, that in the normal environment with noise coupling with 2.5mm bondwire,

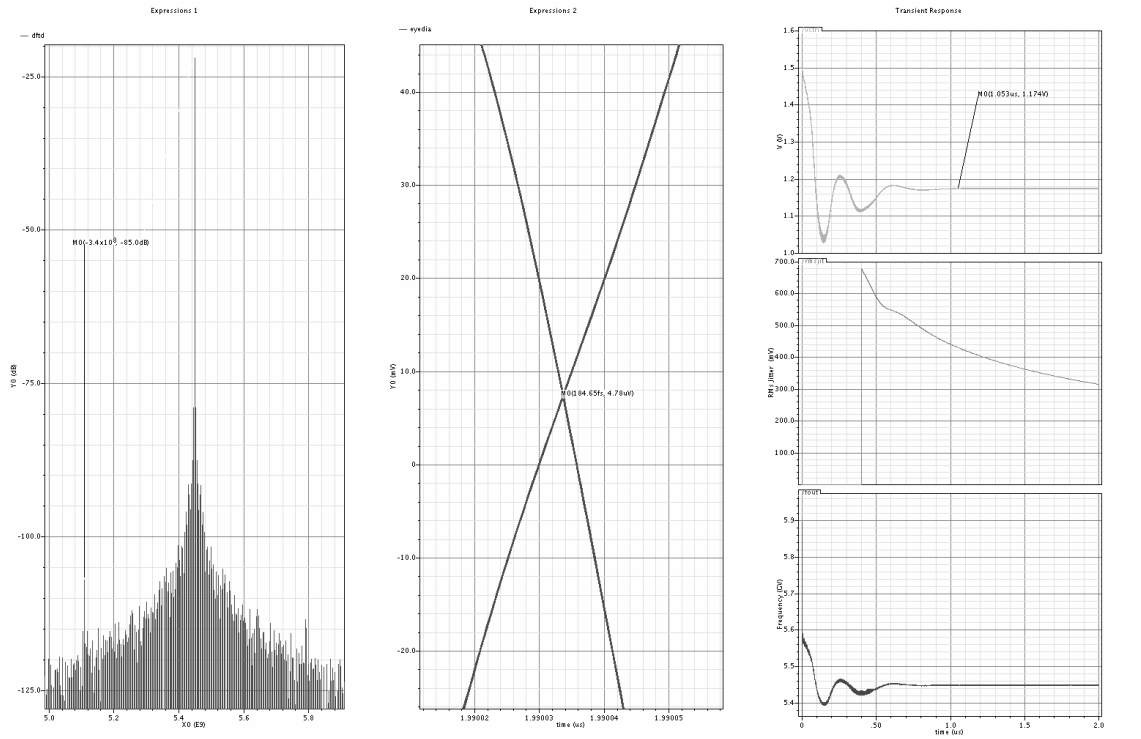


Figure 6-13. Post layout simulation without package and noise-less setting shows 85 dB spur suppression, <200 fs pk-pk deterministic jitter, <320 fs RMS jitter with PLL tuned to 5.45 GHz.

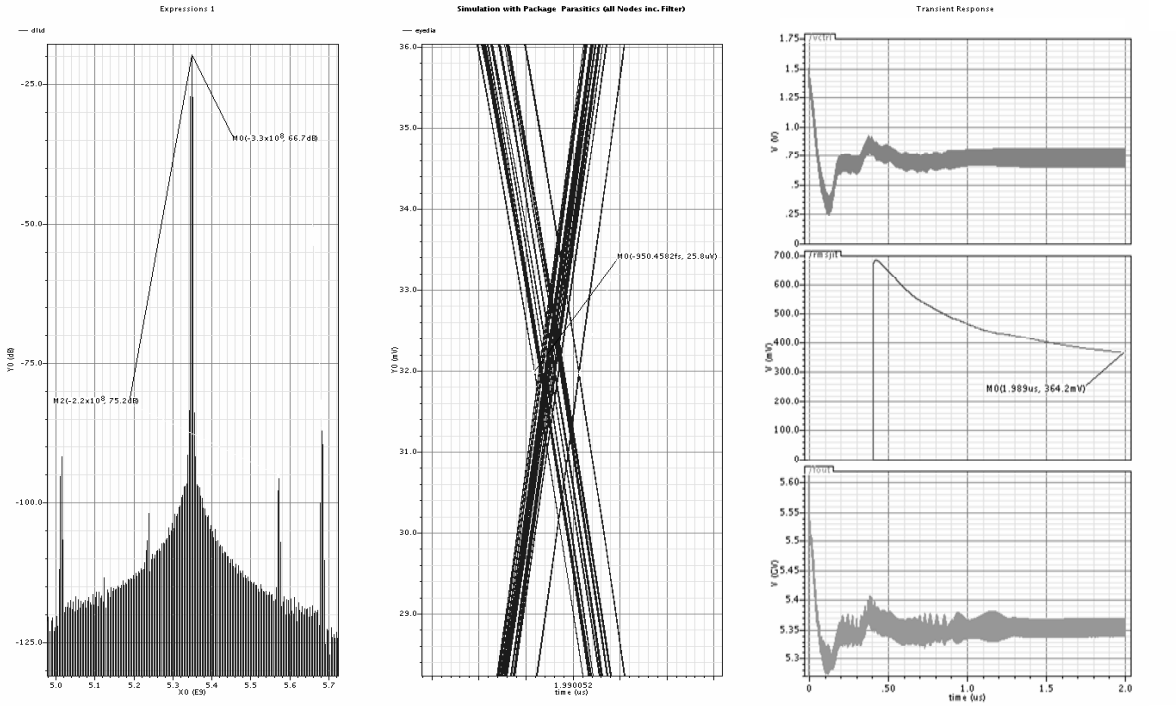


Figure 6-14. Post layout simulation with package and with nominal noise shows 66 dB spur suppression, <951 fs pk-pk deterministic jitter and <360 fs RMS jitter with PLL tuned to 5.35 GHz carrier.

the PLL performance is degraded to where the DJ is near 1ps and RMS jitter is less than 360fs. The noise coupled via the bond-wire adds noise to DC bias voltage and control voltages and as a result, the noise performance is degraded. The spur suppression at 5.35GHz is about 67 dB. Reference noise and the divider injected noise into the substrate are not always modeled in the simulation so noise simulation with 60mV peak to peak voltage is introduced in supplies and 5mVp-p noise is added on the noise sensitive DC nodes at the reference frequency. In reality, 60mVp-p noise is very significant noise but in the design process it helps to know the worst case performance. Figure 6-15 shows the result of post-layout simulations with package and aforementioned reference noise. The PLL shows good robust performance with reference spur suppression >64 dB, <6ps DJ, and <1ps RMS jitter. The PLL settle within 1us for max-deviations in frequency tuned to 5.4 GHz.

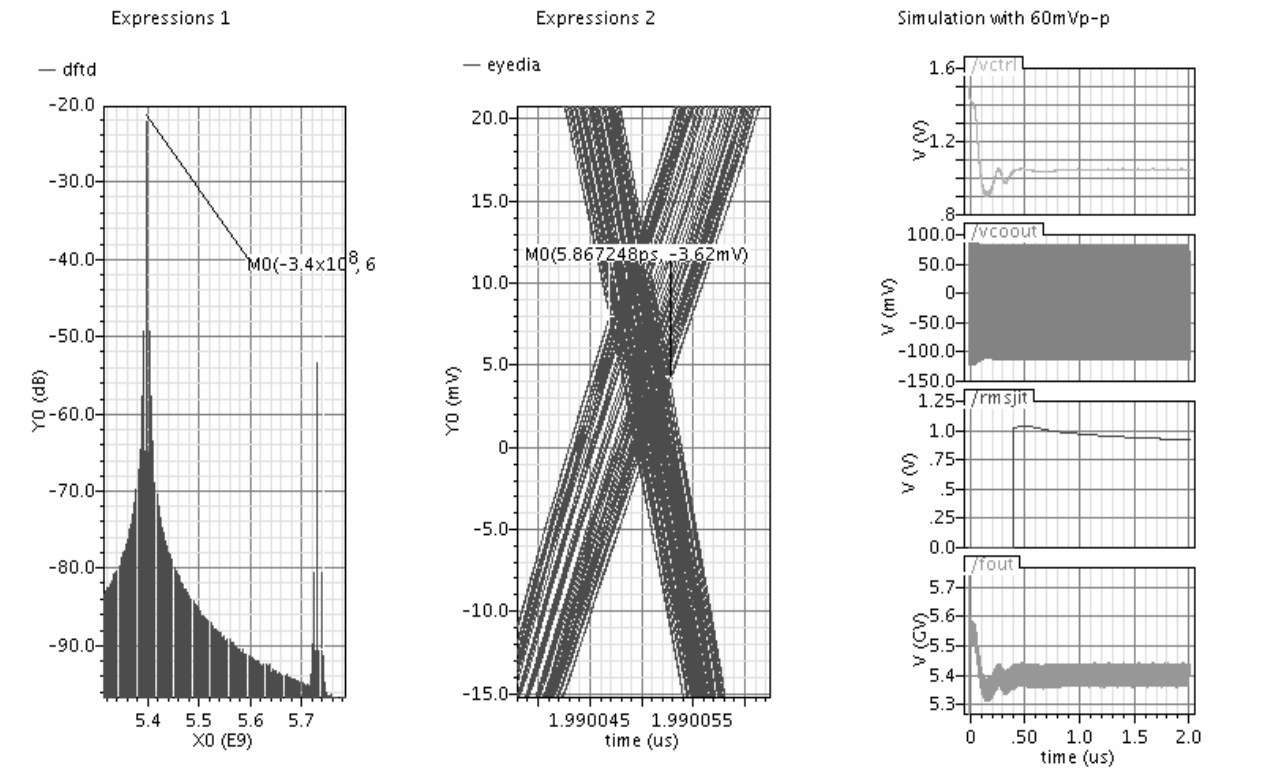


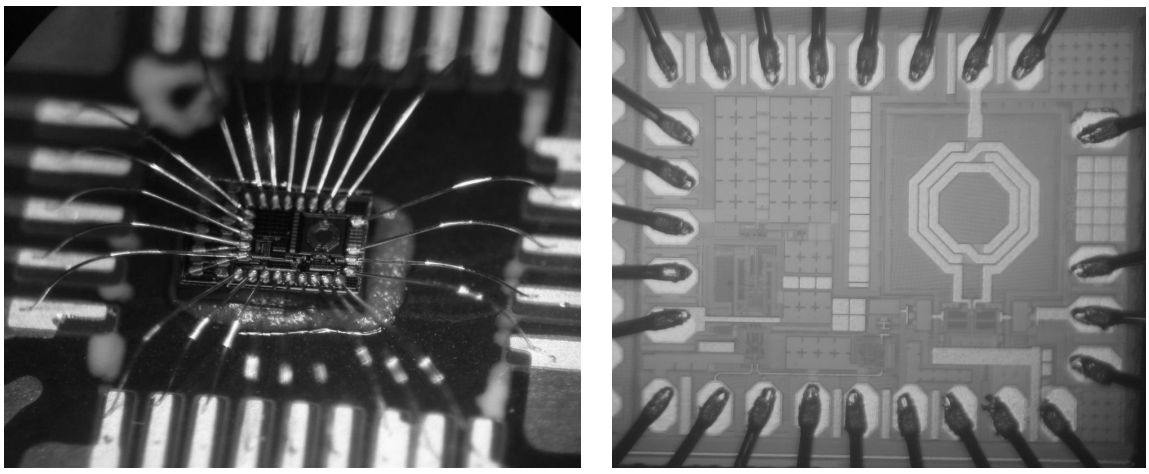
Figure 6-15. Post layout simulation with package and 60mVp-p noise in supplies and 5mVp-p noise at noise sensitive nodes at reference frequency. The PLL still shows robust 64 dB spur suppression, <6 ps pk-pk DJ and <1 ps RMS jitter with PLL tuned to 5.4 GHz carrier.

Normally BSIM4 models do not always have good models for all the devices used in the PLL so the data presented in the Table 6-II has added margins to help account for some excess noise not present in the simulation. Performance results meet our targeted specifications and our objective of developing state-of-the-art low power, fast settling and low jitter PLL architecture.

6.5. Low Power Fast Settling and Low Jitter PLL Measured Results

Measurement of the fabricated prototypical low power, fast settling and low jitter PLL is presented in this section. Due to significant delayed in fabrication time, which led to 2 months delay, this dissertation does not include complete characterization of the proposed PLL. Only a functional test and initial measurements are presented to demonstrate proper operation. Complete measured data for the proposed PLL, which shows great value in academia for advancing the state-of-the-art and to the industry, will be published in peer review journal or conference at opportune time.

Figure 6-16 (a) and (b) show the proposed PLL wire-bonded directly to PCB. Figure 6-17



(a) **(b)**

Figure 6-16. (a) Wire-bonded die attached to PCB with adhesive (b) Micrograph of wire-bonded PLL with less than 1.5mm of bond-wire

shows the characterization PCB board with wire-bonded PLL. The PCB board is made for re-configurability with option for external loop filter if such need arrives. The PCB board has three different ground planes, one for digital, one for analog and one for RF to improve noise isolation as shown in Figure 18. All grounds are tied to the voltage source ground during testing. All RF lines are 50 transmission lines. The DC bias lines are kept wide for low IR drop and are shielded with ground line for isolation. The 1.5V DC supply can be regulated with ADP1710AUJZ-1.5 regulator and 1.2V supply with AD01710AUZ-1.2 regulator but for initial test direct biasing using DC supplies is used. For more thorough and better measurement all supplies will be regulated for improved PSRR performance. The lab test environment is shown in Figure 6-19.

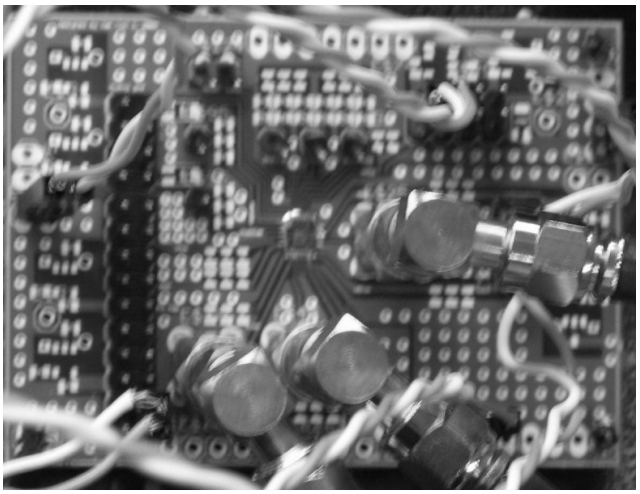


Figure 6-17. (a) Characterization PCB board for the PLL with option for external loop filter

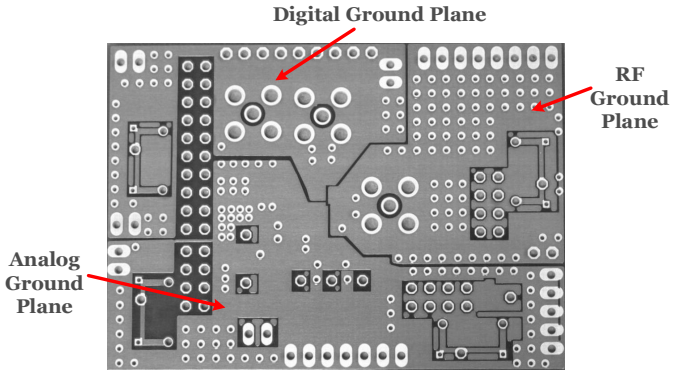


Figure 6-18. PCB Ground plane scheme for low noise environment.

Instruments includes Rhode and Schwarz FSP 40 GHz spectrum analyzer, Tektronix TDS 8000B digital sampling oscilloscope, TDS 2014B digital oscilloscope, HP 8664A 3GHz signal source, and HP6629A DC power supply. For initial testing, HP 8664A signal source is used as a reference signal source. The phase noise at 300 MHz frequency range is about -118 dBc/Hz at 10 KHz offset as shown in Figure 6-20 [24]. For PLL multiplying ratio of 16, the reference noise should shift the in-band phase noise level to -94 dBc/Hz at 10 KHz which is pretty decent reference for PLLs. At 1 KHz frequency offset the noise level is -85 dBc/Hz which is little poor but for initial measurement it will suffice.

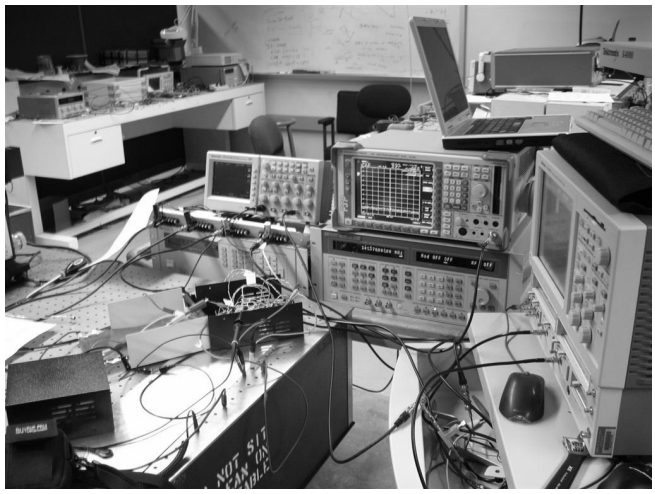


Figure 6-19. (a) PLL Characterization setup with RF spectrum analyzer, digital sampling scope, oscilloscope and HP signal generator which is initially used as a reference frequency source.

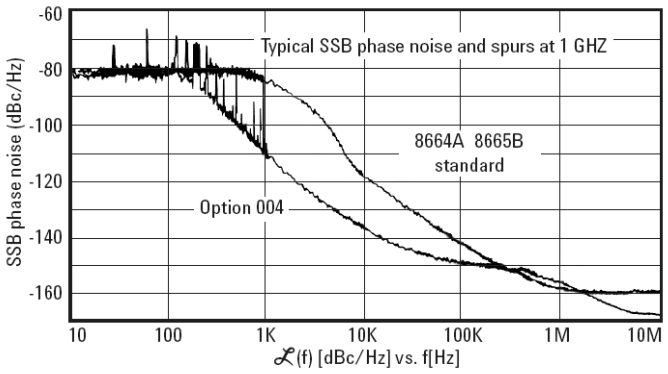


Figure 6-20. (a) Phase noise of 8664A HP signal generator at 10 KHz offset is -118 dBc/Hz

Figure 6-21 shows the measurement result for the proposed PLL tuned to output frequency of 5.5315 GHz. The measured output power level is -10.76 dBm including cable loss.

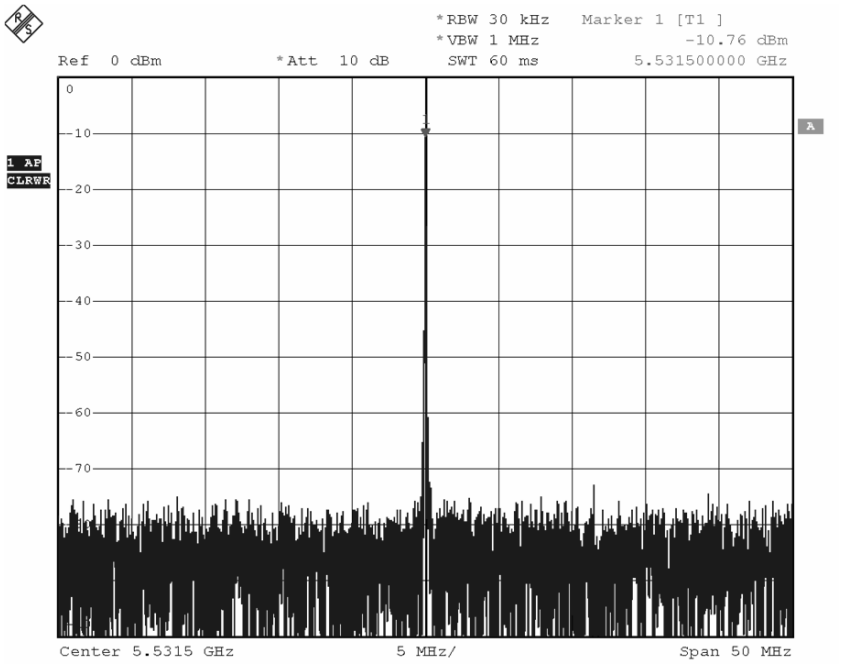


Figure 6-21. PLL output tuned to frequency 5.646 GHz shows the reference spurs at 353MHz offset from the carrier are below 57.6 dB.

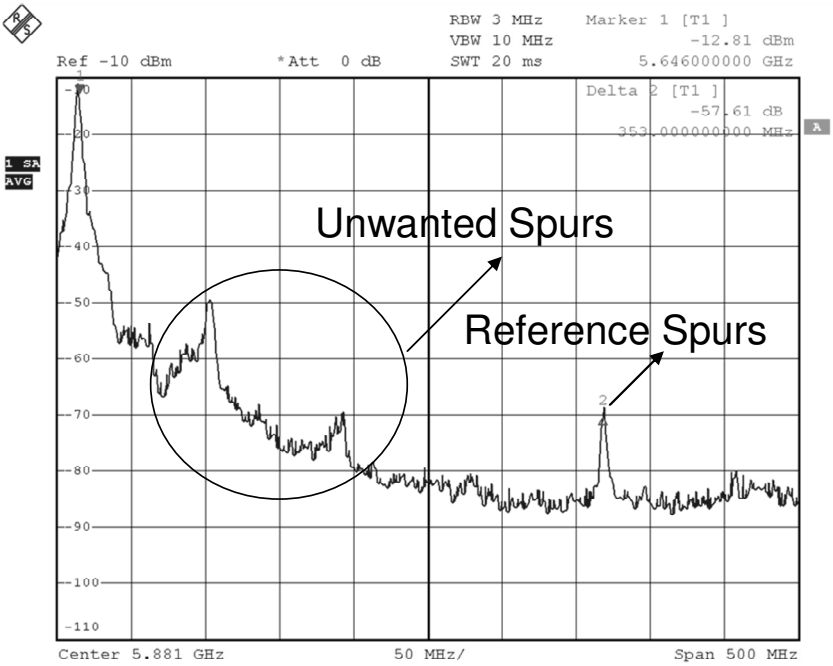


Figure 6-22. PLL output tuned to frequency 5.646 GHz shows the reference spurs at 353MHz offset from the carrier are below 57.6 dB.

Figure 6.-22 shows the PLL tuned to 5.646G Hz has reference spur below 57.6 dB for control loop voltage of 1.2 V. This is robust reference spur suppression figure at outer edge of charge-pump current matching range. The unwanted spurs in the spectrum due to noise coupling can be removed with regulated supplies and filter capacitances on bias lines in final measurement. This is the worst case suppression and for lower control voltages the reference spurs suppression is better than 66 dB.

Figure 6-23 shows the measured output of frequency divider for the proposed PLL tuned to output frequency of 5.48167 GHz which corresponds to divided frequency of 342.61 MHz. The measured output power level is -12.4 dBm including cable loss. The output spectrum shows the phase noise at 5 MHz offset from carrier of -133.60 dBc/Hz at resolution bandwidth of 300 KHz.

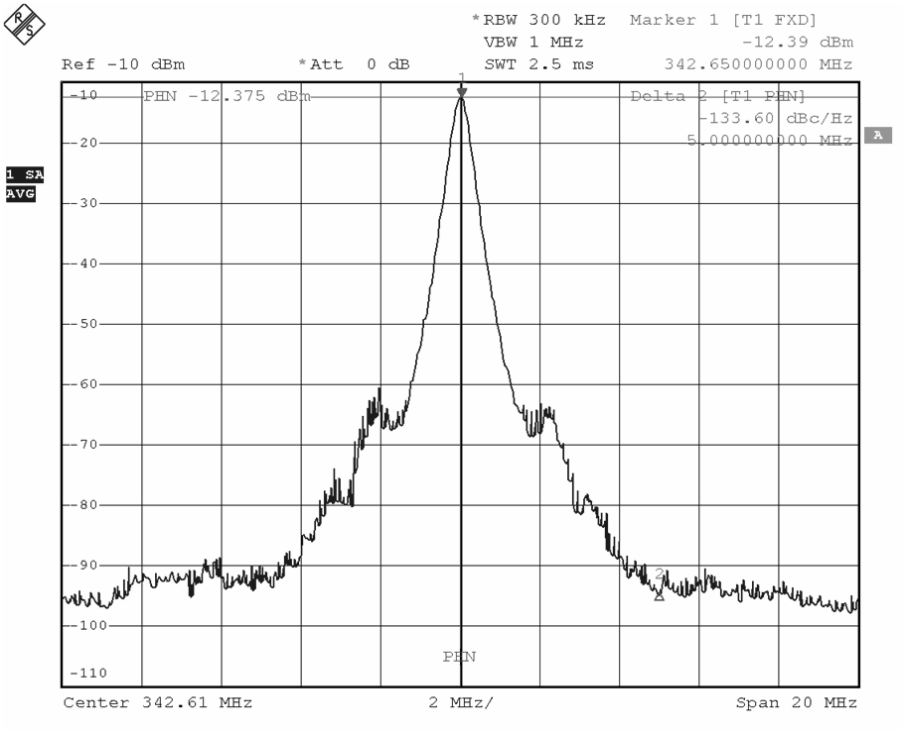


Figure 6-23. Divider output spectrum when PLL tuned to 5.48176 GHz. The phase noise at 300 KHz resolution band is -133.60 dBc/Hz at 5 MHz offset.

Figure 6-24 shows the measured tuning characteristic of the PLL. Over the control voltage range from 0 to 1.5V, the VCO output frequency varies over 206 MHz. The measure VCO gain, K_V, for the proposed PLL is 190 MHz/V which pretty close to the simulated value of 200 MHz/V. The output frequency, however, is shifted up from the post layout simulation result by 300 MHz. Possibility of frequency shift was anticipated due to large variation in simulation results between schematic, capacitive extracted post layout simulation and RC extracted simulation. The data presented in Figure 5-34 is capacitive extracted simulation since it was the worst case simulation result. The schematic simulation showed 250 MHz shift in frequency over the capacitive extracted simulation, as shown in Figure 5-35, with VCO gain of about 225MHz which is close to the measured results.

Figure 6-25 shows a single shot the phase noise measurement of the PLL tuned to 5.5309 GHz. At 1 MHz frequency offset, the measured averaged phase noise is about -120 dBc/Hz which matches well with the simulated results.

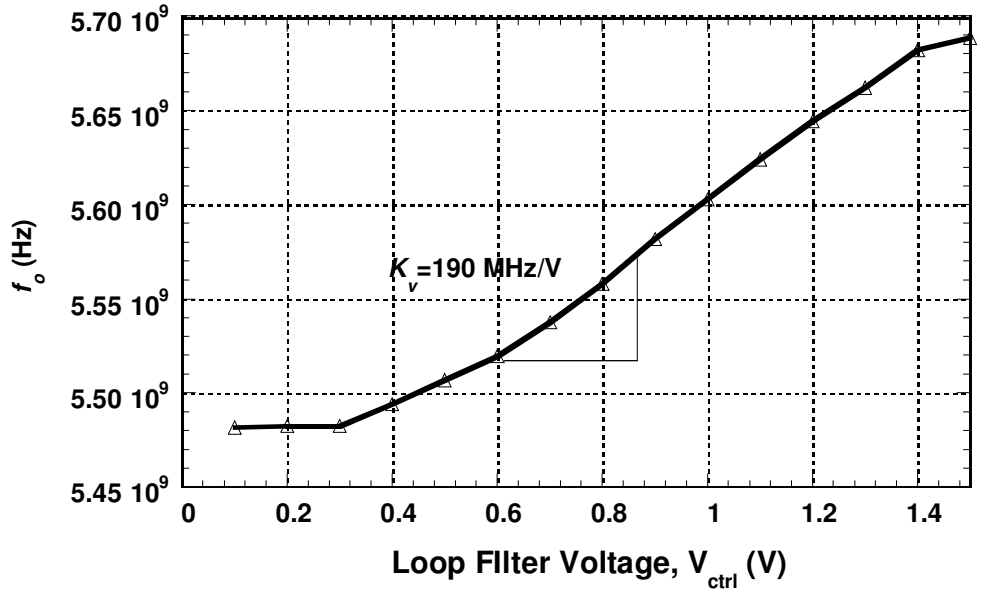


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Figure 6-24. Measured tuned PLL output frequency (f_o) vs. loop filter voltage (V_{ctrl}).

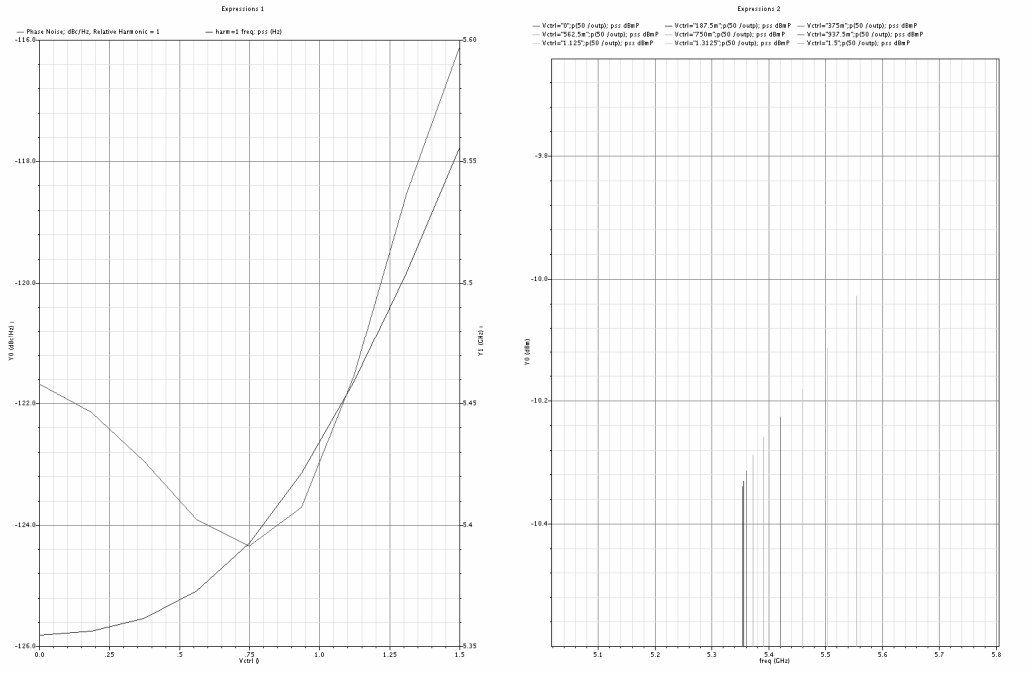

Figure 6-25. Simulated tuning characteristic shows VCO operating from 5.35 GHz to 5.56 GHz.

The PLL phase noise measured with Agilent phase noise interface, which has lower noise floor, is expected to be better than the spectrum analyzer measurement which has poorer noise floor.

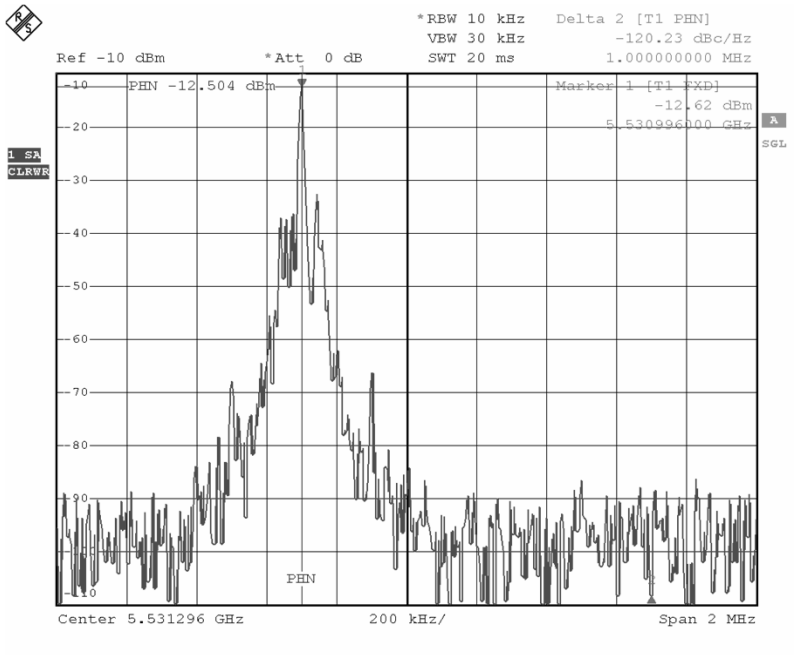

Figure 6-26. Single shot phase noise measurement of PLL tuned to 55.30996 GHz.

Table 6-III summarizes the initial measurements in comparison with simulated performance. Initial data suggest pretty good performance match for the proposed PLL.

TABLE 6-III
LOW POWER, FAST SETTLING AND LOW JITTER PLL PERFORMANCE COMPARISON

Parameter	Description		Simulated	Measured
Power	DC power consumption		11mW	11.5 mW
Rs	Reference Spurs		< -64 dB	< –57.6 dB
P_{noise}	VCO Phase Noise@ 1MHz off.		–121.8 dBc/Hz	–120 dBc/Hz
f_o	PLL output frequency	Schematic Post Layout	5.35– 5.48 GHz 5.1– 5.3 GHz	5.48-5.64 GHz
K_V	VCO gain		200 MHz/V	190 MHz/V

Complete measured data for the proposed PLL, with regulated supplies and filtered bias lines, will be published in peer review journal or conference at appropriate time.

CHAPTER SEVEN

7.0. Conclusion and Future Direction

This dissertation presents a low power adaptive fast settling phase locked loop architecture with novel load independent switched LC VCO, low offset and low glitch dynamic replica-based current steering charge pump and optimized very low power divider to achieve sub-*ps* jitter performance in a 0.18-μm process CMOS technology. Consuming 11mW of total power from 1.5V supply, the PLL achieve sub-μs settling time, worst case reference spurs below 64 dB with integrated RMS jitter of less than 2 ps and deterministic jitter of less than 7ps in a packaged environment. The PLL phase noise is lower than –120 dBc/Hz over the tuning range and is designed with loop bandwidth of 1 MHz.

Initial measured data matches well the simulated performance except for higher output frequencies which is attributed to modeling inaccuracies**.** The proposed work which shows great value in academia for advancing the state-of-the-art and to the industry will be published in peer review journal or conference at appropriate time once characterization is complete. Initial data and rigorous simulation presented in this dissertation motivates full characterization of the PLL which can be leveraged for design of even high FOM factor PLLs.

The dissertation consists of theoretical details of several novel VCO designs, charge-pump architecture and novel adaptive bandwidth mechanism for the PLL. The dissertation includes culmination of works from published or to be published peer reviewed journals and conferences.

Several opportunities exists for advancement of PLL performance for both wireline and wireless transceiver application. Body-enabled low voltage LC VCOs has great potential to

achieve low phase noise and high FOM factor in a triple-well process. Researchers [25] and [26] have used body terminals to achieve high FOM factor VCOs at low supply voltage. Forward body biasing reduces transistor threshold voltage that results in increased bias current, higher transconductance and low flicker noise. Study have shown forward biasing the substrate can reduce flicker noise [27]. This is very significant for VCO design for several reasons. First, lower flicker noise translates to lower phase noise. Second, higher g_m and higher bias current for the same geometry means higher voltage swings and higher transistor F_t. Higher F_t translates to faster switching of the cross-coupled differential pair in the oscillator and lower *1/f* noise up-conversion and therefore, lower phase noise.

Further research, as shown in Appendix, in this line will help advance single or multi-phase LC VCO design to achieve even high FOM performance. Body-biasing can also be applied to frequency divider to increase speed while consuming less DC power. Each individual circuit can be improved. I envision great future for ultra-low power PLL with effective use of the body terminal.

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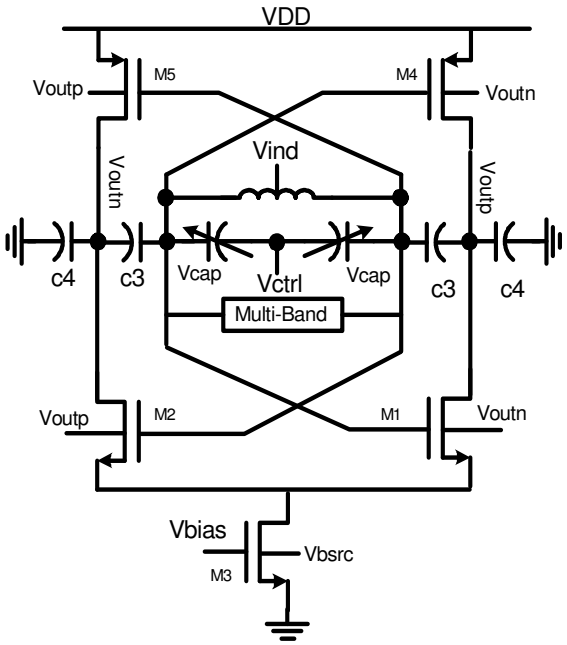
AUTHOR'S BIOGRAPHICAL SKETCH

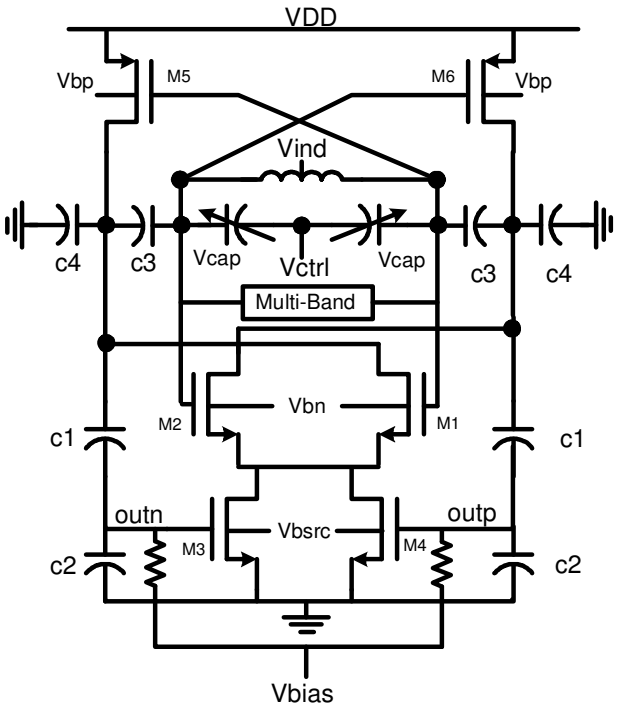
Parag Upadhyaya was born in Kathmandu, Nepal. He received the BSEE and MSEE degree from Washington State University (WSU) in 2000 and 2005 with honors, respectively. He was with Cypress Semiconductor data communication division between 2001 and 2003 as a design engineer, where, he specialized in high speed wireline transceivers. Since 2005, he has been a Ph.D. student in the Advanced RF and Mixed-Signal Application Group (ARMAG) at WSU. He is a recipient of best paper award in 1998 for his wok in tribology, best poster award in 2004 for works related to sub-harmonic mixer, and best poster award in 2006 for novel mixed-signal circuits for wireline and wireless transceiver. He is also a recipient of outstanding Ph.D. student award for the year 2007-2008 from the school of Electrical Engineering and Computer Science at WSU. He has authored or co-authored over 24 journal, conference, and book chapter publications. His current research interest includes wireline/wireless transceivers and MMICs for high-speed data communications.

APPENDIX

A. Proposed Novel body-biased LC VCO with very high FOM factor



B. Proposed Novel complementary body-bias LC VCO with switched current source



C. Proposed Novel Quadrature body-coupled LC VCO with dynamic current source