HIGH SPEED SIGE MMICS FOR PHASED ARRAY COMMUNICATIONS

By

PINPING SUN

A dissertation submitted in partial fulfillment of
the requirements for the degree of

Doctor of Philosophy

WASHINGTON STATE UNIVERSITY
School of Electrical Engineering and Computer Science

August 2008

To the Faculty of Washington State University:

The members of the Committee appointed to examine the dissertation of Pinping Sun find it satisfactory and recommend that it be accepted.

_____
Chair

_____

_____

ACKNOWLEDGMENT

I would first like to thank my parents, for all the love, support and understanding over my study over my life. I wish to express sincere appreciation to my advisor, Professor Deuk Heo, for his guidance and helpful suggestions in the project. I would like also to thank the rest of my committee, Professor George La Rue and John Ringo for their experience and support.

Finally, I would like to thank my group members, Parag Upadhyaya, Peng Liu, Lan Chuan Zhou, Jaeyoung Jung, You Yu, Yang Zhang, I have got many helps from them during the projects.

This work was supported by Air Force Research Laboratory, Boeing Phantom and Jazz Semiconductor.

HIGH SPEED SIGE MMICS FOR PHASED ARRAY COMMUNICATIONS

ABSTRACT

by Pinping Sun, Ph.D.
Washington State University
August 2008

Chair:

High speed SiGe MMICS for phased array communications has been widely used in satellite communications. This dissertation presents the development of reconfigurable SiGe MMICs for upper X-band or lower Ku band satellite phased array communications. Novel high-isolation, low-insertion-loss and highly linear octagonal PIN diode has been designed on SiGe substrate to improve on the current state of the art performance. Fabricated in a standard 0.18-μm SiGe BiCMOS technology, the 50 μm^2 PIN SPST switch can achieve an insertion loss of less than 0.65 dB from 2 to 18 GHz with the measured P_{1dB} of 16 dBm. The radiation tolerance of the developed PIN diodes has been verified with TID test up to 1000 krad.

Based on the novel PIN diode implementation, the new SPDT architecture which alleviates the leakage caused by the *Psub-Nwell* parasitic diodes has been presented. The measurement results shows that the SPDT switch can achieve a through-path loss of 1.2 to 1.8 dB and an isolation path loss of 51 to 36 dB over a wide frequency range (2 to 18 GHz). A 4-bit Ku-band bridged-T filter type PIN diode phase shifter is used to realize 0^0 to 360^0 phases with a resolution of 22.5^0. The average power consumption of this phase shifter is only 2.5 mA with a 3.3 V voltage supply. This phase shifter achieves compact chip area, flat phase response, low delta insertion loss, high return loss and low power consumption. The low power active combiner is used to combine the multiple phase shifters into a phased array.

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

PUBLICATIONS

Journal Papers

- **P. Sun,** P. Upadhyaya, D.Heo, "Silicon-Based PIN SPST RF Switches for Improved Linearity and Insertion Loss", submitted to *IEEE Trans. Microwave Theory Tech.*

- Y.S. Suh, **P. Sun**, I. S. Kim, J. S, Song, and D. Heo, "A Fast Computation Method in Frequency Domain for Power Ground Plane Impedance Calculation Using the Mobius Transform," *IEEE Tran. Adv. Packag*, vol.31, No.2, pp.320-325, May 2008

- **P. Sun,** P. Upadhyaya, D.Jeong, D.Heo, G.. La Rue**, "**A Novel SiGe PIN Diode SPST Switch for Broadband T/R Module," *IEEE Microw. Wireless Compon. Lett*., pp.352-354 , May 2007

Conference Papers

- **P. Sun**, Y. Kim, D. Heo, "An Ultra Low Power Analog Frequency Divider", accepted by the proceeding of *IEEE MTT-S International Microwave Symposium,*2008

- **P. Sun,** P. Upadhyaya, D.Heo, "A High Performance Double Bias Tuning Complementary VCO," Technology and Talent for the 21st Century, 2007

- **P. Sun**, P. Upadhyaya, L. Wang, D. Jeong, D. Heo, " High Performance PIN diode in 0.18 μm SiGe Process for Broadband Monolithic Control Circuits", in *Proc. European Microwave Integrated Circuit Conf.*, pp. 149-152, Sept. 2006.

- L. Wang, P. Upadhyaya**, P. Sun**, D. Heo, "A 5.3GHz Low-Phase-Noise LC VCO With Harmonic Filtering Resistor", in *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 3237-3240, May 2006.

- **P. Sun**, L. Wang, P. Upadhyaya, and D. Heo, "High Isolation 10GHz to 20 GHz SPDT Switch Design Using Novel Octagonal PIN diode structure," in *Proc. IEEE Workshop on Mcroelectronics and Electron Devices*, Apr. 2005, pp. 38-41.

- L. Wang, **P. Sun**, D.Heo., "A 15-GHz Single-Pole Double-Throw Annular MOSFET Switch for space application", in *Proc. IEEE Workshop on Microelectronics and Electron Devices*, Apr. 2005, pp. 103-106.

- **P. Sun,** Y. Lian and A. B. Ajjikuttira. "A 10-Gb/s, 1.5-volt low-power 1:4 demultiplexer for optical fiber communication", *ASIC, 2003. Proceedings. 5th International Conference,* vol. 2, Oct. 2003，pp.1082 – 1085.

- **P. Sun***,* Y. Lian and A. B. Ajjikuttira., **"**A 2.4-Gb/s Low-Power 1:4 Demultiplexer for Optical Fiber Communication", *Inaugural Symposium on Microelectronics*, the Institute of Microelectronics, Singapore, 2003

CHAPTER ONE

INTRODUCTION

In satellite space communications, phased-array antenna systems offer many significant advantages over those that utilize a conventional antenna. The advantages include the ability to make multiple steered antenna beams from the same aperture, the ability to make antennas conformal with their mounting structure, and the ability to generate directive beams that can be electronically repositioned. Solid-state device technology has motivated phased arrays to overcome the low reliability inherent with tube-type transmitters and their associated high voltage power supplies and also improves system efficiency. The transmit/receive (T/R) module forms the final stage of the module for transmitted signals and the first stage of the module for received signals. Apart from amplification, it controls the amplitudes and phase of the signals to steer the antenna beam. Low module cost is desirable due to the number of modules required in a general phased array application. For these reasons, T/R modules significantly affect the entire phased array antenna architecture and play a critical role in determining the overall system cost and performance for phased array based applications [1].

Most high performance transmitter/receiver (T/R) modules in the phased array communication systems have been commonly implemented in III-V compound semiconductor technologies, such as GaAs or InP [2]-[3]. However, high cost and low integrative capacity of these materials are prohibitive to the commercialization of fully integrated SoC solutions. Recently, silicon based technologies became a low cost alternative solution [4]-[6]. For space applications, radiation-tolerant and low cost SiGe BiCMOS technology becomes one of the technologies of choice for the fast-growing phased array communication systems [7]-[14].

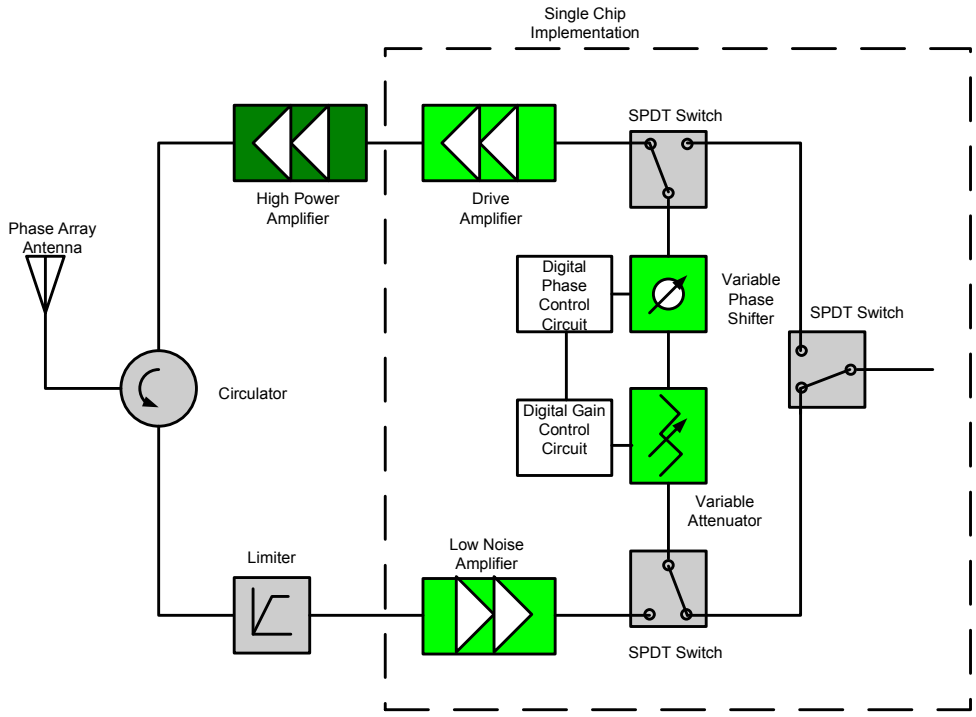


Fig. 1 Next Generation T/R module with single chip front-end

This dissertation is focused on the investigation of radiation-tolerant SiGe MMICs for upper X-band or lower Ku band satellite phased array communication systems. It includes the development of low cost and high performance SiGe MMIC blocks such as SPDT T/R switch and phase shifter based on novel PIN diodes. Innovative circuit design and layout methodologies have been developed to improve on standard SiGe circuit performance for radiation-tolerant space communication applications. The radiation tolerance of developed PIN diodes and RF SiGe MMICs has been verified with TID test up to 1000 krad.

1.1 Organization

The basic operations of phased array will be introduced in Chapter 2. Chapter 3 will present our first step in the research, a 2GHz to 18 GHz high isolation, low insertion loss, highly linear and high radiation tolerant PIN diode SPST switch. The advantages of using

an octagonal PIN diode will be explained through the theoretical analysis and measurement verification.

High performance SPDT design will be presented in chapter 4. We will extensively address many design aspects of SPDT switch, such as series, series-shunt, *Psub-Nwell* parasitic diode and the selection of anode size for series and shunt arm. A through-path loss of 1.2 to 1.8 dB and an isolation path loss of 51 to 36 dB over a wide frequency range (2 to 18 GHz) have been measured.

In Chapter 5, we will describe a 4 bit Ku band compact phase shifter and active power combiner design for phased array. Finally, the conclusion will be given in Chapter 6.

CHAPTER TWO

BACKGROUND

The demand for high data rate wired and wireless communications drives the increase of the channel capacity. According to Shannon's theorem, the channel capacity (*C*) characterized by the highest data rate of reliable transmission in bits per second (bps) is given by[15]:

$$C = B \times \log_2(1 + S / N) \tag{1}$$

where *B* is the channel bandwidth and the *S/N* is the signal-to-noise ratio. This equation indicates that by increasing the channel bandwidth and the *S/N*, the channel capacity can be improved.

Usually the maximum bandwidth is decided by the Federal Communications Commission (FCC). For a given operating frequency, the bandwidth is limited by the FCC regulation, and the directly increasing the bandwidth to increase the data rate is often impossible. Thus, the method which can improve the system's *S/N* becomes more practical and important.

Phased array communications system is one architecture level solution to increase the system's *SNR*. The phased array is a group of antennas in which the relative phases and the respective signals feeding the antennas are varied in such a way that the effective radiation pattern of the array is reinforced in a desired direction and suppressed in undesired directions[16]. Usually, for the beam forming in the phased array, the same signal is transmitted or received on each antenna with a time delay and a variable gain. By doing this, the directional radiation pattern is shaped and focused on one particular direction. Compared with mechanical reorientation of antenna to generate beam steering, the electronic methods is much faster and can avoid the strong interfere with the undesired signal. Thus, the electrically scanned phased array systems are widely used in

recent years [17].

2.1 The SNR at phased array antennas

The phased array system can genetically improve the system's *SNR*. When the antennas are spaced at sufficient distance, the radiation noise of each antenna is uncorrelated. However, the signals in the antenna are correlated, and lead to the *SNR* improvement in phased array systems because it can focus the transmitted or received signals into a certain direction and suppress the noise.

Since the received signals are coherent, the n channel output signal can be

$$S_n = n^2 S_1 \tag{2}$$

Since the noise source at each of the antenna is white and uncorrelated, it can be described as:

$$N_n = \sum_{i=1}^{n} N_1 = n N_1 \tag{3}$$

where N_1 is the noise from one antenna and N_n is noise from N element phased array. By putting the (2) and (3) into (1), the signal from antennas add in amplitude (coherently) while the noise adds in power, creating a $10\log(N)$ dB in the *SNR* for an N element phased array receiver. Thus, the channel capacity is increased.

2.2 The non-linearity at phased array antennas

An ideal phased array communication system would be a linear system. However, the harmonic distortion from the system itself, the gain compression, cross modulation and interference can become comparable with the desired signals, corrupting the signals.

The gain compression point is one important figure of merit. The small-signal gain of a circuit is usually obtained with the assumption that the harmonics are negligible.

However, as the signal amplitude increases, the gain begins to vary. The output is a compressive or saturating function of the input. The 1 dB compression point is the input signal level that causes the small signal gain to drop by 1dB [18] (shown in Fig.2). It indicates where the circuits start to leave the linear region and the harmonics become serious problems.

Another important specification that is used to measure the system's linearity is the third order intercept point. A weak signal accompanied by two strong interferers experiences third order non-linearity. When one of the IM products falls in the band of interest, the desired component is corrupted. The third intercept point (IP3), this parameter is measured by a two toned test. It is obtained by extrapolating the fundamentals output and the third-order inter-modulation products which increase at three times that of the fundamentals. The third-order intercept point is defined to be at the intersection of the two lines [18] (shown in Fig.3). The horizontal coordinate of this point is called the input *IP3*(*IIP3*), and the vertical coordinate is called the output *IP3*(*OIP3*).

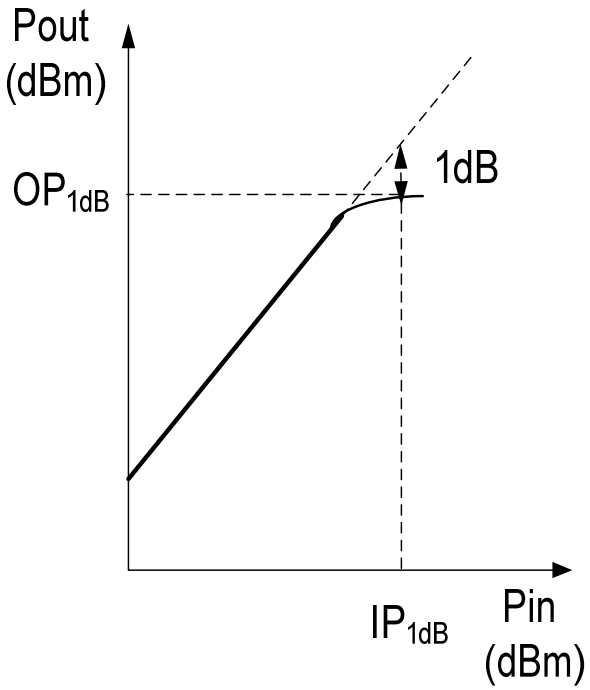


Fig.2 Definition of the 1-dB compression point

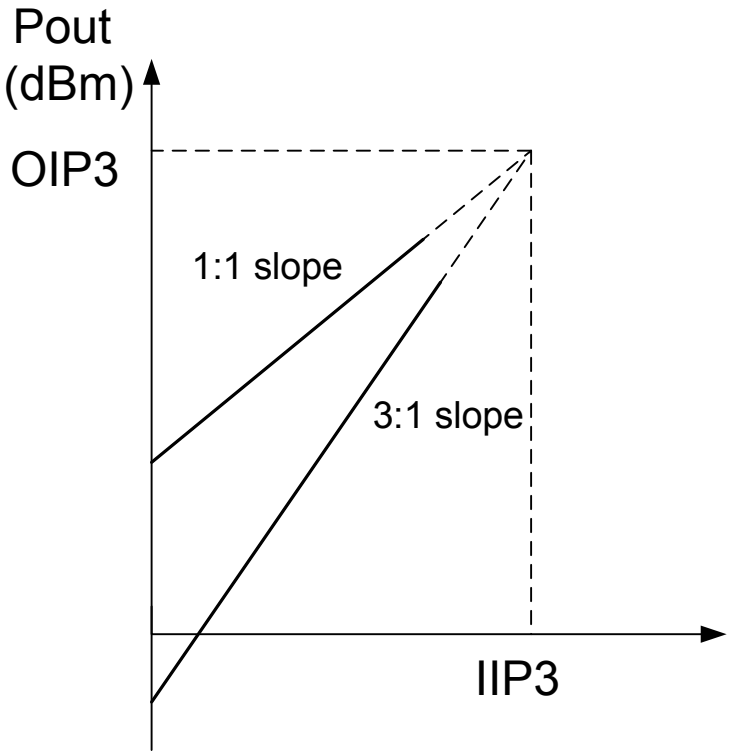


Fig.3 Definition of the third order interception point

2.3 Phased array architectures

There are two types of phased array architecture which are widely used these days: IF phase shifting and RF phase shifting architectures. Fig. 4 shows the IF phase shifting architecture. After the LNA, the LO signals are mixed with the input RF signals and convert them to IF band. Since the phase shifting and the power combining functions are operated at low frequency, the IF phase shifter exhibits lower loss and lower power consumption than the RF phase shifter. However, at low frequencies, the passive devices, such as inductors and capacitors consume larger chip area than RF phase shifting. Also, the mixers are connected to a low directional antenna and are subjected to interference from all directions and the inter modulation products generated can propagate throughout the array, causing more interference [16].

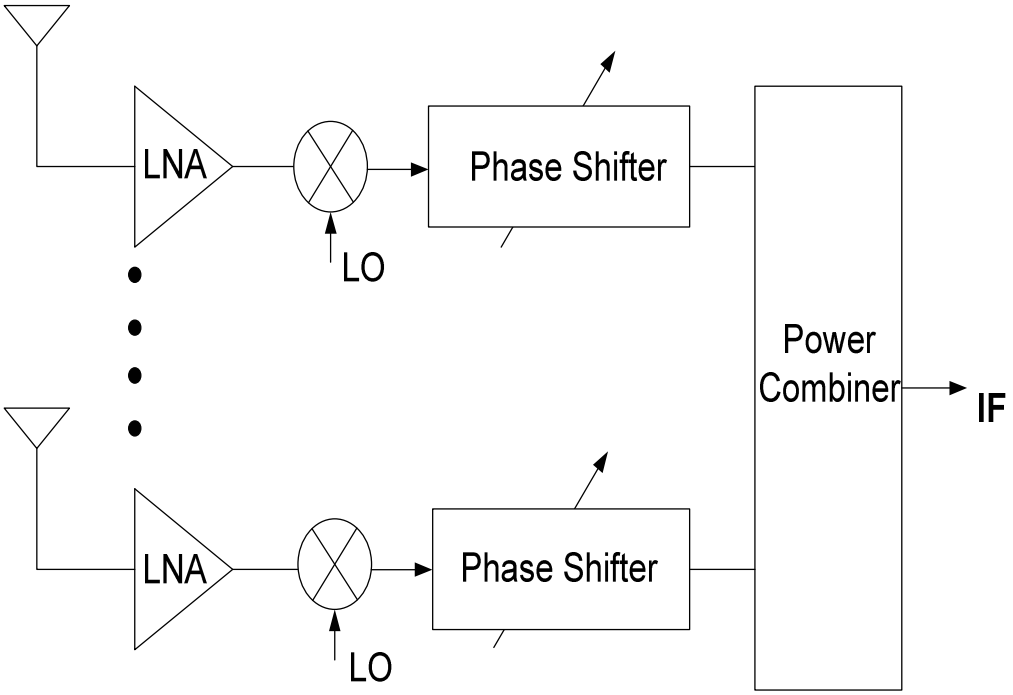


Fig.4 IF phase shifting architecture

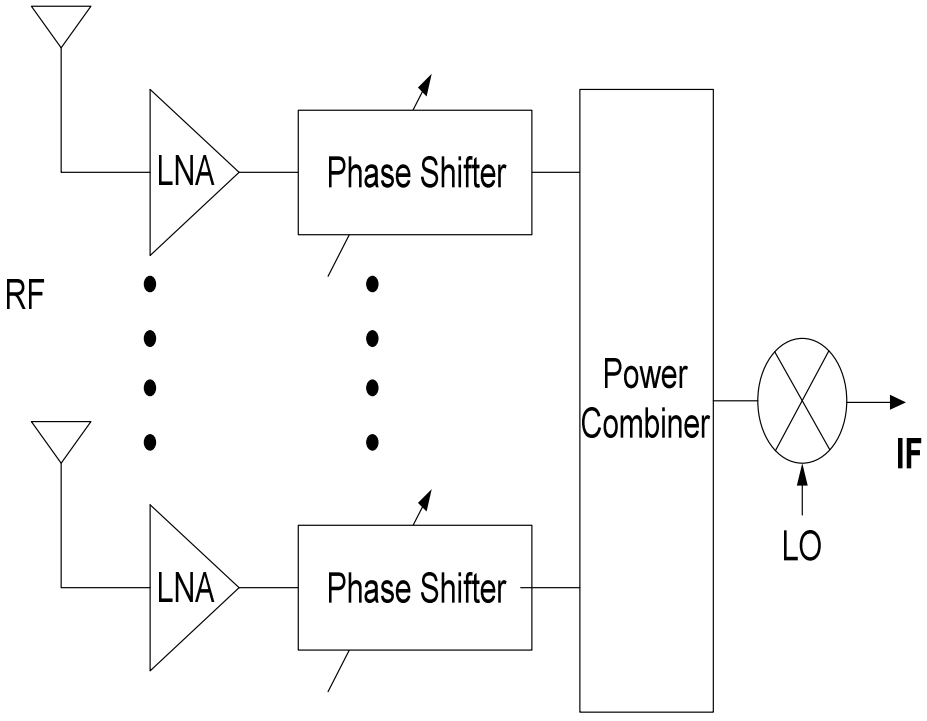


Fig.5 RF phase shifting architecture

Phase shifting in the RF domain for each array element has been very popular (shown in Fig.5). The output signal after the RF combiner has high pattern directivity and can substantially reject an interferer before the mixer, which can maximize the system's signal to noise ratio. Also, the LO distribution network is removed in system resulting a simple system. This project uses the RF phase shifting architecture [16]–[17].

The exploration of a SiGe phased array receiver will be presented in subsequent chapters.

CHAPTER THREE

HIGH ISOLATION, LOW INSERTION LOSS AND HIGH LINEARITY PIN DIODE DESIGN

A low insertion loss, high isolation and highly linear PIN Diode SPST in Jazz 0.18-um BiCMOS process is presented in this dissertation to achieve state of the art performance.

3.1 The return loss, insertion loss and isolation in switch design

The T/R modules in phased array systems need a high performance switch. There are three important criteria to evaluate switch performance. They are the return loss, the insertion loss in the "on' state and the isolation in the "off" state.

At high frequencies electric circuits can be viewed as a collection of finite transmission line sections connected to various discrete active and passive devices. When an incident voltage wave propagating along the positive z-axis interacts with a load impedance termination, the traveling waveform can be defined as;

$$V(z) = V^{+}e^{-kz} - V^{-}e^{+kz} \tag{4}$$

$$I(z) = I^{+}e^{-kz} + I^{-}e^{+kz} \tag{5}$$

where k is the propagation constant, the V^{+}, I^{+} represent wavefronts propagating in the +z direction, whereas the V^{-}, I^{-} donate the wave propagation in the –z direction[19].

If the source impedance is not match with the load impedance, there is a reflection from the load to the source which is defined by the reflection coefficient Γ:

$$\Gamma_0 = \frac{V^{-}}{V^{+}} \tag{6}$$

The return loss (RL) is defined by the mismatch between the available source power and

the power delivered to the transmission line in the case when the input reflection coefficient is not zero, which is the ratio of reflected power, $P_r = P_{in}^-$, to the incident power, $P_i = P_{in}^+$. It can be described as:

$$RL = -10\log\left(\frac{P_r}{P_i}\right) = -10\log|\Gamma|^2 = -20\log|\Gamma_{in}| \tag{7}$$

Insertion loss (*IL*) defined a ratio of transmitted power P_t to incident power P_i. If an unmatched circuit is connected to an RF source, reflection occurs that result in a loss of power delivered to the circuit. The insertion loss reaches the maximum when the circuits represent open conditions. In switch applications, the turn on resistance is expected to be very small and when the circuits are matched to the source, most of the power is transmitted to the circuits, and the insertion loss becomes small [19].

$$IL = -10\log\frac{P_t}{P_i} = -10\log\frac{P_i - P_r}{P_i} = -10\log\left(1 - |\Gamma_{in}|^2\right) \tag{8}$$

When the switch is turned off, isolation is used to define the transmitted power to incident power. The circuits have good isolation when the leakage from the source to the load is very small.

3.2 The PIN diode and PN diode

A PN diode is formed by placing the P^+ and N^+ type semiconductor closely together. For a PIN diode, an extra low doping intrinsic layer is placed between the P^+ anode and N^+ cathode. In microwave applications, PIN diode is widely used for switching, amplitude attenuation and phase shifting [20]. Compared with PN diodes, PIN diodes have better isolation and linearity.

In the diode reverse bias condition, the intrinsic region between the P^+ anode and N^+ anode increase the depletion region width, reduce the junction capacitance and increase

the isolation. Since the thicker depletion region exhibited flatter C-V profiles than the thinner ones, the reverse bias capacitance modulation of PIN diode is smaller than PN diode [21].

For a PN diode, the I-V curve shows an exponential equation as:

$$I = I_s(e^{qV/nkT} - 1) \tag{9}$$

where the I is the diode current, I_s is the saturation current, V is the voltage across the diode, n is the ideal factor, k is boltzmann's constant, q is the magnitude of the charge on an electron. The exponential function of voltage-current is obviously non-linear.

PIN diodes are designed to enhance the linearity of the forward biased resistance of the PN diode. In the forward bias condition, when the it satisfy $Q_s >> I_{rf} / 2\pi f$, where the I_{rf} is the RF current, f is the operating frequency and Q_s is stored charge in intrinsic region, the stored charge is much larger than the RF induced charge that is added or removed from I-region by the RF current. The intrinsic resistance is:

$$R_I = \frac{l_i^2}{2\overline{\mu}\tau I_{dc}} \tag{10}$$

where, l_i , the thickness of intrinsic region, μ, the average electron and hole mobility, are predefined by the process. The forward biased PIN diode behaves as a current controlled resistor that presents a linear resistance to the flow of RF current through the diode. This is the property of a PIN diode that enables the device to be used as the RF power control element in linear attenuators and modulators [20].

3.3 The PIN diode and the MOSFET switch

A MOSFET can also be used as a switch. When it turns on, the turn on resistance is[22]:

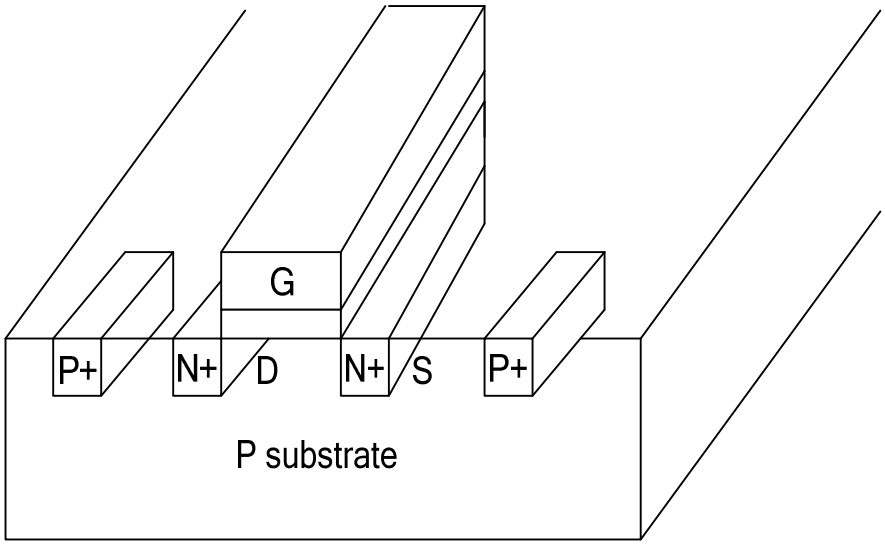


Fig.6 The physical cross-section view of MOSFET

$$R_s = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_T)} \tag{11}$$

At the turn off state, the capacitance is:

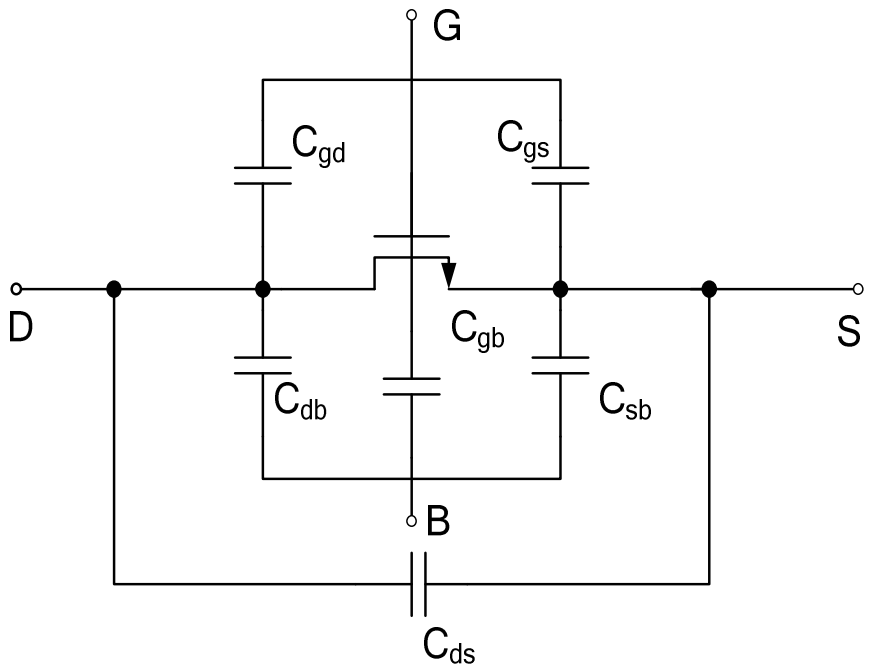


Fig. 7 Parasitic capacitances of a MOS transistor that is used as switch in “off “state [6]

$$C_{off} = C_{ds} + \frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}} + \frac{C_{sb}C_{db}}{C_{sb}+C_{db}} \tag{12}$$

which can also be written as:

$$C_{off} = F(W, L, V_{db}, V_{sb}) \tag{13}$$

Both the forward bias resistance and reverse bias capacitance are related to input RF signal amplitude, which will cause the non-linearity in the application.

3.4 PIN diode implementation in standard SiGe BiCMOS process:

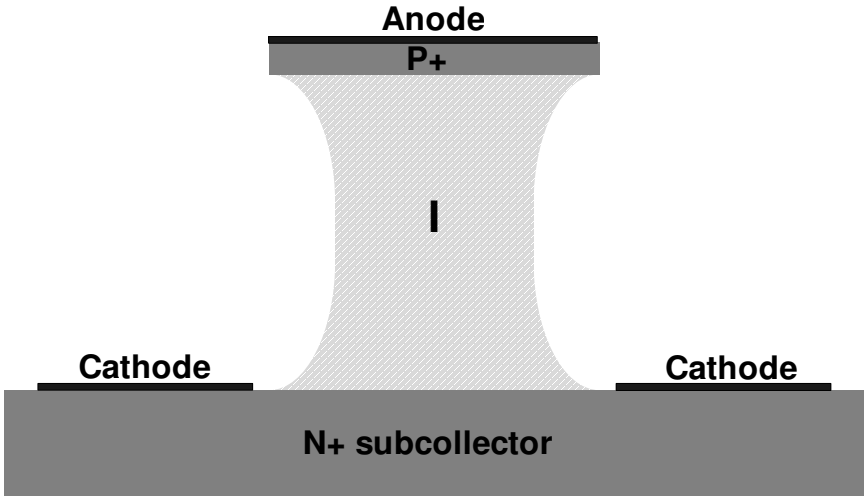


Fig. 8 Ideal vertical PIN diode cross-sectional view

A vertical PIN diode is formed by heavily doped *P* and *N* regions with a lightly doped intrinsic region (*I*), as shown in Fig. 8. The intrinsic region between the anode and cathode is removed by mesa etching to achieve high isolation. In a standard Jazz 0.18-µm SiGe BiCMOS process, the PIN diode is realized with HBT material layers: the P^+ base layer, the *N*-epi collector layer and the buried N^+ subcollector layer, as shown in Fig. 9. The intrinsic region between the anode and cathode can't be etched in this process.

The relationships of the equivalent-circuit model to the physical parameters of the PIN diode are also described in Fig.9. C_I and C_O are the anode-to-substrate and the cathode-to-substrate capacitance, respectively. C_P is the parasitic capacitance between the anode and cathode port. R_C is the contact resistance, which consists of the anode contact resistance R_{CA} and the cathode contact resistance R_{CC}. R_N is the resistance from *N-epi* layer. R_I is the current based resistance, C_J is the junction capacitance in the intrinsic region and R_S is the parasitic resistance in the p-substrate. C_{PD} is the capacitance of the parasitic *Psub-Nwell* diode that varies with bias voltage.

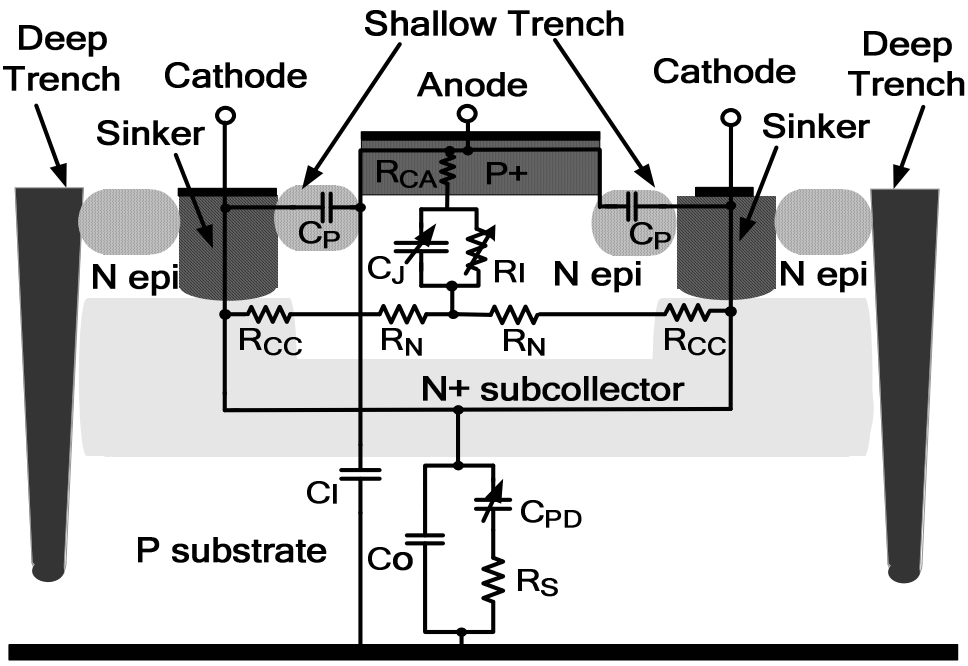
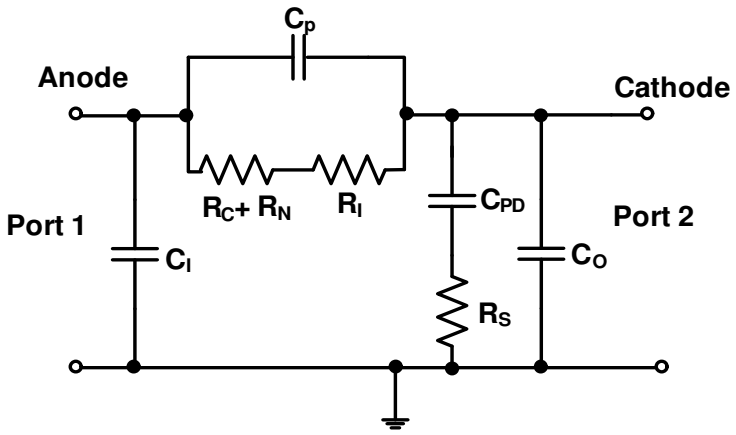
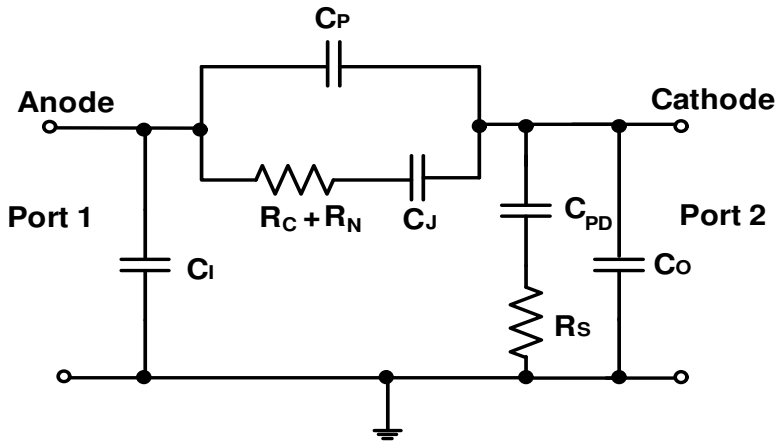


Fig. 9 PIN diode cross-sectional view in a standard SiGe process.

For the microwave PIN diode switch, the crucial criteria are the forward bias insertion loss and the reverse bias isolation. Fig. 10 (a) and (b) show the PIN diode small signal equivalent circuit model for determining the S-parameters.



(a)



(b)

Fig.10. Small signal equivalent circuit models for PIN RF switch (a) Equivalent circuits for "on" state (b) for "off" state

computation. The insertion loss S_{21} and the isolation S_{12} of the PIN diode can be expressed as:

$$S_{21} = \frac{Z_0 \,||\, \frac{1}{sC_o} \,||\left(\frac{1}{sC_{PD}} + R_S\right)}{\frac{1}{sC_P} \,||\, (R_C + R_N + R_I) + Z_0 \,||\, \frac{1}{sC_o} \,||\left(\frac{1}{sC_{PD}} + R_S\right)} \approx \frac{Z_0 \,||\, \frac{1}{sC_o} \,||\left(\frac{1}{sC_{PD}} + R_S\right)}{(R_C + R_N + R_I) + Z_0 \,||\, \frac{1}{sC_o} \,||\left(\frac{1}{sC_{PD}} + R_S\right)} \tag{14}$$

$$S_{12} = \frac{Z_0 \| \frac{1}{sC_I}}{Z_0 \| \frac{1}{sC_I} + \left(\left(R_C + R_N \right) + \frac{1}{sC_J} \right) \| \frac{1}{sC_P}} \approx \frac{Z_0 \| \frac{1}{sC_I}}{Z_0 \| \frac{1}{sC_I} + \frac{1}{sC_J} \| \frac{1}{sC_P}} \quad (15)$$

where, Z_0 =50 Ω is the terminated characteristic impedance. We can safely assume that $|1/sC_P| \geq |R_C + R_N + R_I|$ and $|1/sC_J| \geq |R_C + R_N|$.

Three geometric and layout parameters are used to enhance the performance of the PIN RF switch. They are the anode-to-cathode distance (*ACD*) of the PIN diode, the periphery-to-area (*P/A*) ratio of the anode and the cathode contact resistance.

3.4.1 Insertion Loss enhancement by optimizing anode to cathode distance

In a standard SiGe 0.18-μm BiCMOS process, the *N*-epi layer between the anode and cathode is not completely etched out by the shallow trench isolation. The epi-layer resistance R_N is reduced by the residual un-etched *N*-epi layer since extra current path has been generated. Thus, the total cathode contact resistance is the series connection of R_N and R_{CC}. Since R_N *is* decreased with the reduction of *ACD*, the best insertion loss can be achieved with the minimum *ACD*, as defined by the design rule of the technology.

In the reverse bias condition, the capacitance C_P between the anode and the cathode reduces the denominator of S_{12} and degrades the isolation. With the reduction of *ACD*, the C_P is increased and the isolation becomes worse.

The isolation of PIN diodes with different *ACD*s shows negligible difference because the parasitic capacitance C_P between the anode and the cathode does not crucially affect the reverse bias capacitance. The C_P can be represented as:

$$C_P = \varepsilon A / S \tag{16}$$

where, A is the PIN diode's lateral area and S is the distance between the anode and the cathode terminal. As shown in Fig. 10(b), the reverse bias capacitance can be simply represented as C_P+C_J. The effect of C_P can be analyzed based on the modeling data from Table II (the Circuit model parameters of 25 μm^2 PIN diode with the ACD of 0.9 μm). According to Table II, C_J is 0.018 pF and C_P is 0.0001 pF for this particular size device. When PIN diode's ACD increases from 0.9 μm to 1.8 μm, based on equation (8), CP becomes 0.0002 pF while increasing C_P+C_J by 0.5 %, which is insignificant. This explains that the *ACD* doesn't have a crucial effect on device isolation. Therefore, there is a trade-off between the insertion loss and isolation when optimizing the *ACD*.

3.4.2 Insertion loss enhancement by optimizing *P/A* ratio

In the forward bias condition, the total resistance is the contact resistance R_C plus the current dependent resistance R_I from the intrinsic region which is represented by (17) [23]:

$$R_I = \frac{w_0 w}{2\mu\tau_0 J_0^{1/3} A^{1/3} I_{dc}^{2/3}} \tag{17}$$

where τ_0 is the effective minority carrier lifetime for a given intrinsic layer width w_0 and current density J_0, w is the width of the intrinsic layer, A is the device's anode area, μ is the average electron and hole mobility and I_{dc} is the forward bias current.

The relationship between τ_0, the bulk lifetime τ_{bulk} and the effective surface recombination velocity v_{perim} is given by (18)-(20) [13]. The contributions from τ_{bulk} can be neglected because there are more dislocations at the interface and the periphery than in the bulk region. As (18)-(20) describe the minority carrier recombination from the P^+/I

interface, the periphery is the main factor affecting τ because there are more dislocations located at the interface and the periphery than in the bulk region [24].

$$R_{eff} = R_{bulk} + R_{perim} + R_{interface} \tag{18}$$

$$\frac{p - p_0}{\tau} A \approx \frac{p - p_0}{\tau_{interface}} A + \nu_{perim}(p - p_0)P \tag{19}$$

$$\frac{1}{\tau} \approx \frac{1}{\tau_{interface}} + \nu_{perim}(\frac{P}{A}) \tag{20}$$

where, R_{eff} is the effective recombination rate of the device, R_{bulk} is the bulk minority carrier recombination rate, R_{perim} is the periphery normalized minority carrier recombination rate, $R_{interface}$ is the recombination rate at the SiGe/Si interface, p - p_0 is the excess minority carrier concentration on the n-side of the junction, $\tau_{interface}$ is the P^+/I interface minority carrier lifetime and v_{perim} is the effective hole surface recombination velocity. The interface recombination is determined by the process, but the PIN diode geometry is custom-tailored in this design to achieve a small periphery-to-area ratio, and longer minority carrier lifetime.

The forward bias current I_{dc} consists of recombination, I_{rec}, and diffusion, I_{diff}, currents as shown in equations (21)-(22) [24]. I_{diff} is 10^{19} times smaller than the I_{rec}, and thus, is neglected in the calculation. I_{rec} is the sum of bulk recombination current which is proportional to the diode area, A, and the surface recombination current which is proportional to the perimeter length, P. Since the major recombination occurs at the perimeter and not the bulk, the bulk recombination current is omitted in (22).

$$I_{dc} = I_{rec} + I_{diff} \approx I_{rec} \tag{21}$$

$$\begin{aligned} I_{rec} &= (\frac{qWv_{th}\sigma N_t n_i}{2} A + q\, s_p L_s n_i P) \exp\left(\frac{qV}{2KT}\right) \\ &\approx \left(q\, s_p L_s n_i P\right) \exp\left(\frac{qV}{2KT}\right) \end{aligned} \tag{22}$$

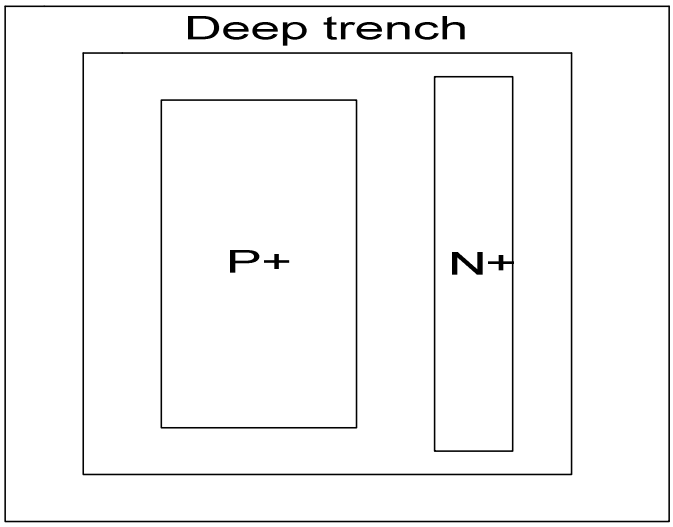
where, v_{th} is the thermal velocity of the carriers, N_t is the trap concentration, σ is the capture cross section of the deep trap, W is the effective depletion width where the carrier recombination is significant, n_i is the intrinsic carrier concentration, s_p is the surface (perimeter) recombination velocity and L_s is the surface diffusion length.

By employing equations (20)-(22) in (17), we can obtain:

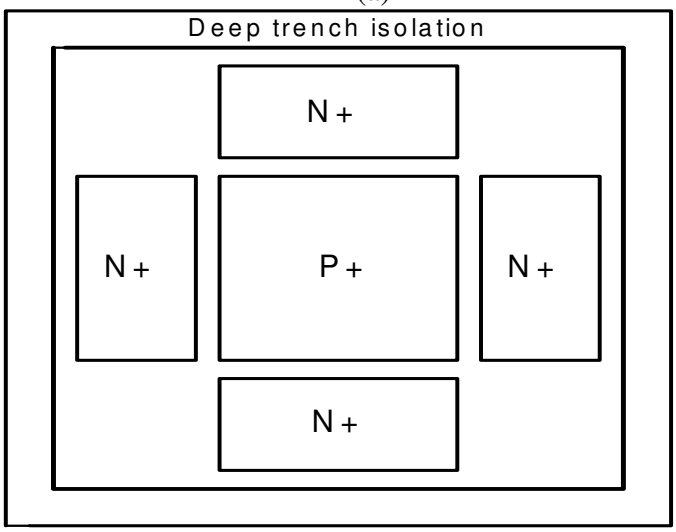
$$R_I = \frac{w_0' \, w \, v_{perim}}{2\mu J_0^{1/3}\left[q \, s_p \, L_s \, n_i \exp\left(\frac{qV}{2KT}\right)\right]^{2/3}} * \frac{1}{A}\left(\frac{P}{A}\right)^{1/3} \tag{23}$$

Equation (23) shows that R_I is proportional to P/A for a given anode size. By minimizing the anode's P/A ratio, the current dependent resistance can be reduced and forward bias insertion loss is improved. The optimization method is based on the reverse proportional relationship between the τ and PIN diode's periphery-to-area ratio (P/A).

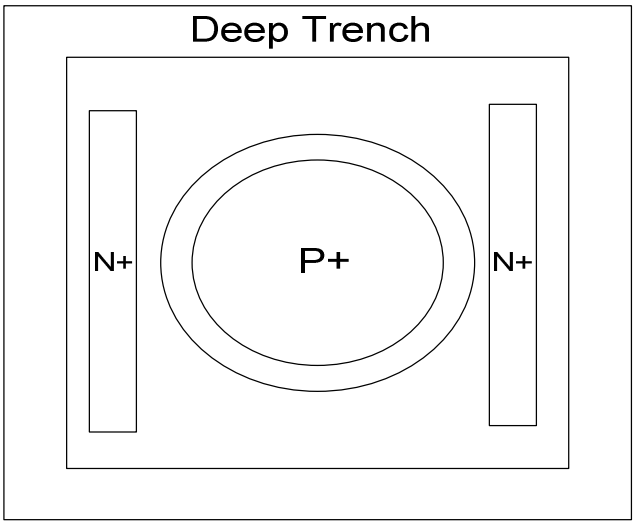
The improvement of the P/A ratio of a PIN diode can be achieved by changing the anode's geometry. Compared with rectangular (25 µm * 2 µm with P/A = 1.08 x 10^4 cm^{-1}), square (7 µm * 7 µm with P/A = 0.56 x 10^4 cm^{-1}), dodecagon (50 μm^2 with P/A = 0.508x10^4 cm^{-1}) and circular (50 μm^2 with P/A = 0.501x10^4 cm^{-1}) PIN diode geometry, the octagonal (50 μm^2 with P/A = 0.51x10^4 cm^{-1}) PIN diode becomes a simple and effective choice for PIN diode design in a standard SiGe process without the mesa etching step. For the 50 μm^2 anode size, the octagonal geometry reduces the P/A ratio by 52.9% and 9.28 %, compared with the rectangular and square geometry, respectively.



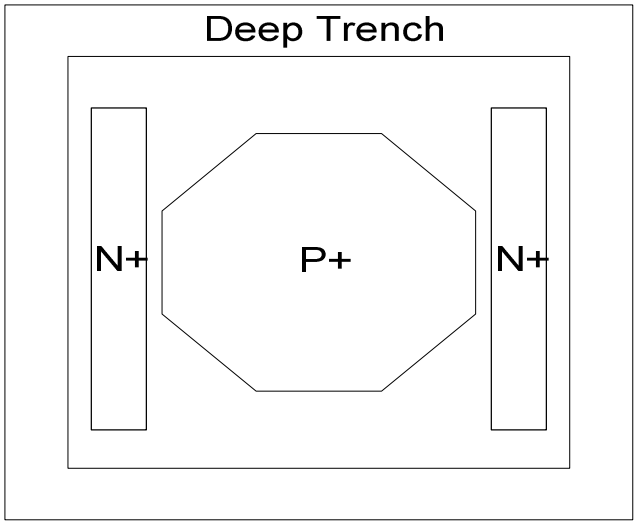
(a)



(b)



(c)



(d)

Fig.11. PIN diode with (a) rectangular (b) square (c) circular (d) octagonal anode shape

3.4.3 Insertion loss enhancement by optimizing the cathode contact resistance

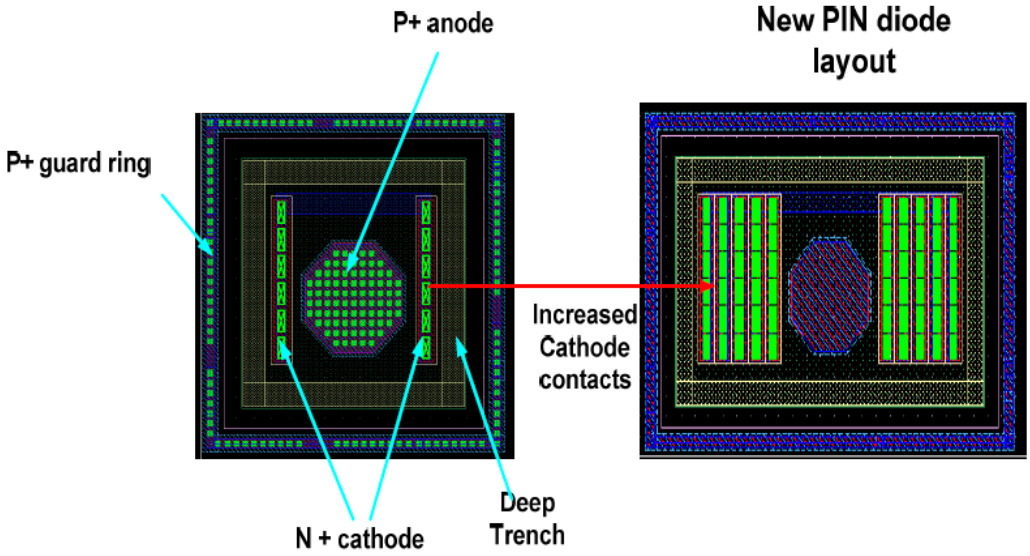


Fig.12 The optimization of PIN diode cathode contact resistance

Because the forward bias resistance also consists of the cathode contact resistance, by reducing the cathode contact resistance, the insertion loss can be improved. In the new

design, the number of cathode contacts has increased 10 times; the cathode contact resistance has reduced from 0.2 ohm to 0.02 ohm, which improves the insertion loss.

3.5 Analysis of geometric effects on linearity and power handling capability

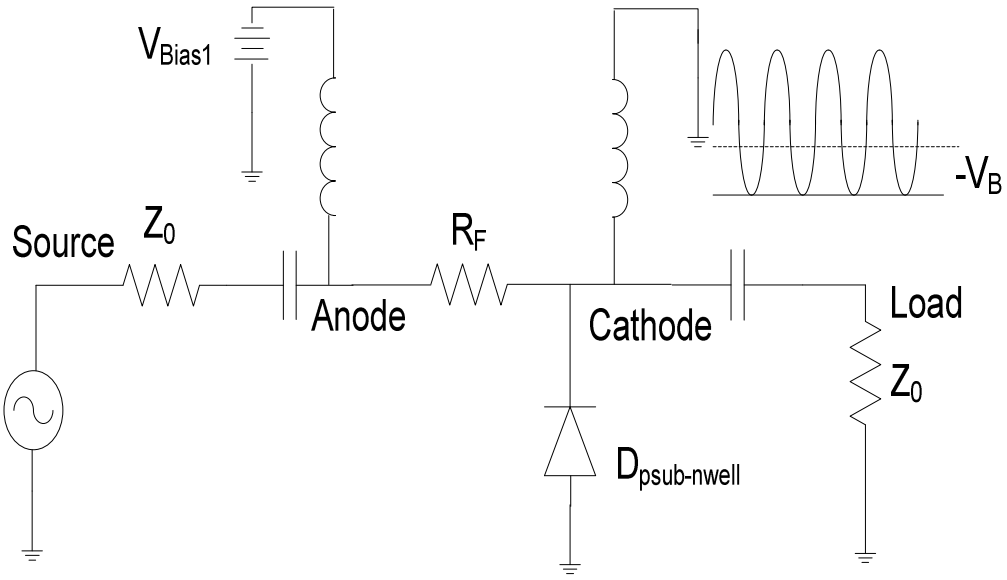
In a standard *SiGe* BiCMOS process, the nonlinearity in a series connected PIN RF switch exists due to the current-dependent resistance (R_f) modulation [25], and the leakage of the un-wanted forward biased *Psub-Nwell* parasitic diode under large RF signal swings.

In the forward bias condition, the modulation of the current-based resistance, R_f, in the intrinsic region can severely degrade the linearity of the PIN RF switch. The modulation occurs either at very low input frequencies or at high power levels.

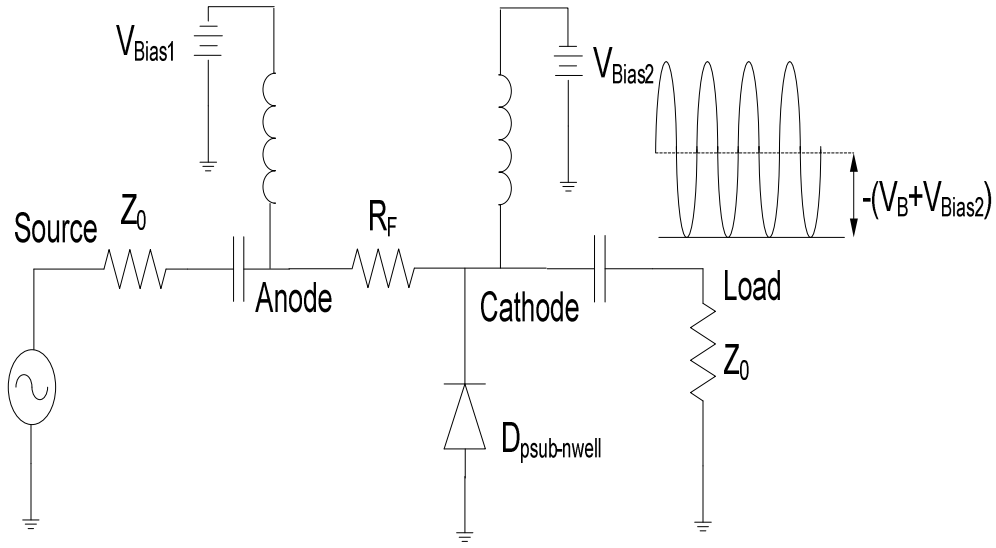
When $f < 1/(2\pi\tau)$, where f is the PIN RF switch's operating frequency and τ is the effective carrier lifetime in the intrinsic region, the injected carriers in the intrinsic region recombine before responding to the input frequency. For an average τ of 10 ns [26], the PIN RF switch's low frequency modulation is below 159 MHz, which is significantly lower than the required application frequencies. Thus, distortion in the PIN RF switch is primarily dominated by large RF input power. At a high RF signal power, the stored carriers are insufficient to track large injected RF currents, and thus, linearity is degraded. The compression point of the PIN RF switch P_{1dB} can be expressed as [25]:

$$P_{1dB} = 14.4 + 15 \log (Q_{nC} f_{MHz} / R_I) \tag{24}$$

where Q_{nc} is the stored charge in nano-coulombs and f_{MHz} is the operating frequency in mega-hertz. The employment of smaller *P/A* ratio octagonal anode shape also improves the PIN RF switch's linearity. Since $Q=I\ \tau_0$, by employing I and R_I from (20)-(22) in (24), we can obtain:



(a)



(b)

Fig.13 Simplified large-signal models for a forward biased series PIN diode with cathode (a) grounded and (b) positively biased

$$P_{1dB} = 14.4 + 15 \times \log \left\{ \frac{2 f_{MHz} \mu \, J_0^{\frac{1}{3}} \left[q s_P L_S n_i \exp\left(\frac{qV}{2KT} \right) \right]^{\frac{5}{3}}}{w \, w_0 \, v_{perim}^{\,2}} \times \frac{A^2}{\left(\frac{P}{A} \right)^{\frac{1}{3}}} \right\} \tag{25}$$

For a given size of PIN switch in the predefined process, the magnitude of distortion signal is directly related to the operating frequency and *P/A*. By reducing the *P/A*, the device's carrier lifetime is increased, and more charges are stored in the intrinsic region to handle large RF power. Thus, the octagonal anode geometry with small *P/A* ratio enhances the PIN RF switch's power handling capabilities.

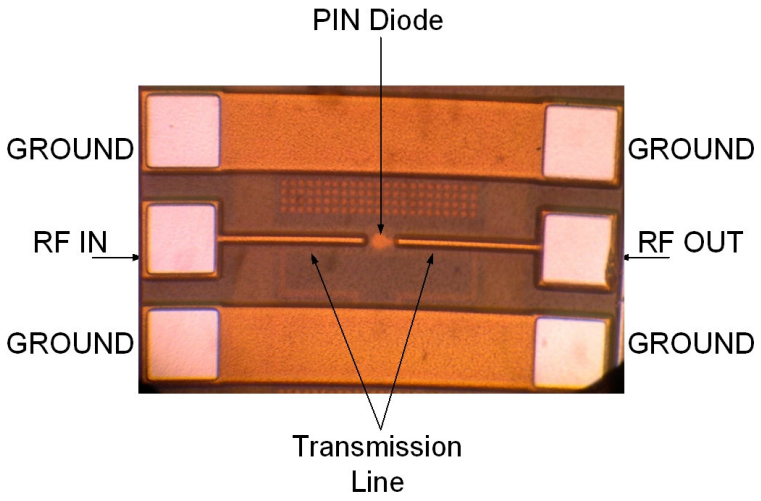
The undesirable forward bias *Psub-Nwell* parasitic diode can also degrade the power handling capability of the switch. Since the *P* substrate is always grounded, a large negative swing on the *N-well* subcollector, which is the cathode of PIN diode switch, can push the *Psub-Nwell* parasitic diode into a forward-bias region. In order to overcome this limitation, the PIN diode switch's cathode can be positively biased [5]. This simple implementation increases the power handling capability of the PIN diode switch over a wide-band frequency range.

Fig. 13 illustrates two bias conditions for the parasitic *Psub-Nwell* diode, which result in different linearity and power handling capabilities. The resistance R_F represents the PIN diode's forward bias resistance, V_{bias1} is the anode bias voltage, and V_{bias2} is the cathode bias voltage. In Fig. 13 (a), the PIN diode's cathode is shorted to ground through an inductor. When the RF swing at the cathode is lower than $-V_B$, where the V_B is the forward pinch-on voltage of the parasitic diodes, the parasitic diode $D_{psub\text{-}nwell}$ is forward biased, and it functions as a small forward-biased resistor. The cathode output voltage is then approximately clamped to $-V_B$. Fig. 13(b) demonstrates a technique for improving the linearity and power handling capability of PIN SPST switches. This improvement is achieved by applying a positive bias to the cathode of the series PIN diode. The positive bias at the PIN diode switch's cathode does not affect the normal operation of the switch as long as $(V_{bias1}\text{-}V_{bias2}) = V_{FB}$, where the V_{FB} is the forward bias voltage of the PIN diode

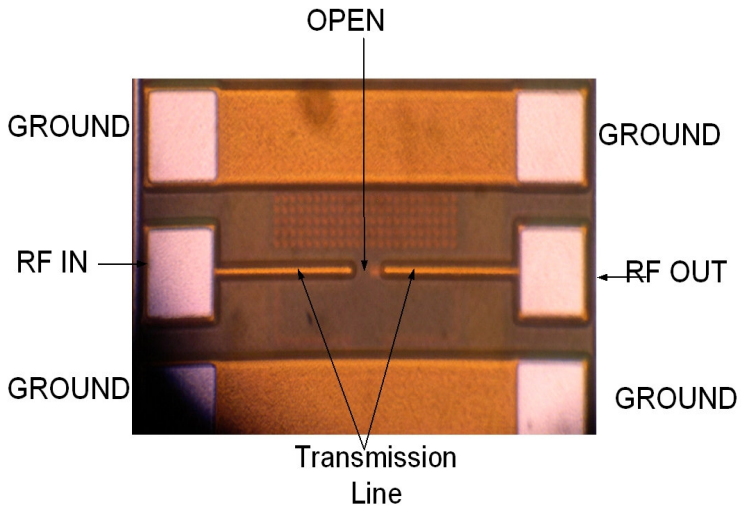
switch to achieve a given amount of forward bias current. By using this technique, applying positive DC bias to the cathode, the parasitic diode is always in reverse bias and can withstand a strong negative swing to $-(V_B+V_{bias2})$. This positive cathode bias technique, therefore, leads to larger power handling capability and higher linearity.

3.6 De-embedding test structure for an extracting accurate PIN diode model

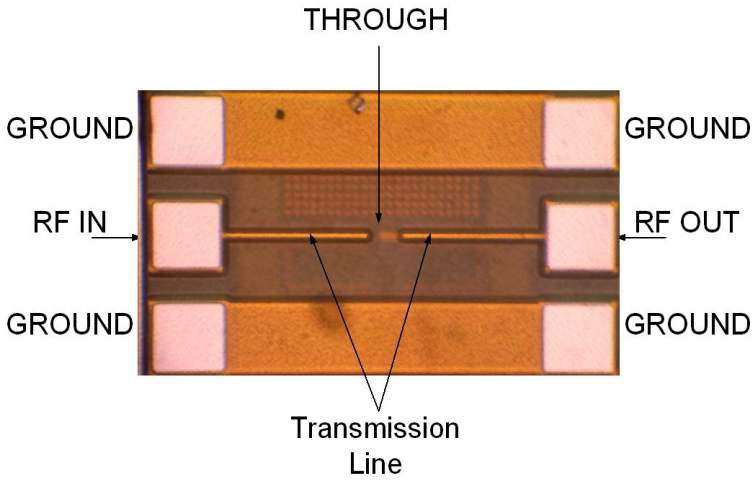
In order to get accurate model information oft PIN diodes, de-embedding test structures were designed for the measurement. Three-step de-embedding method is used to build the test structure [27]. By using this technique, the parasitic components'



(a)



(b)



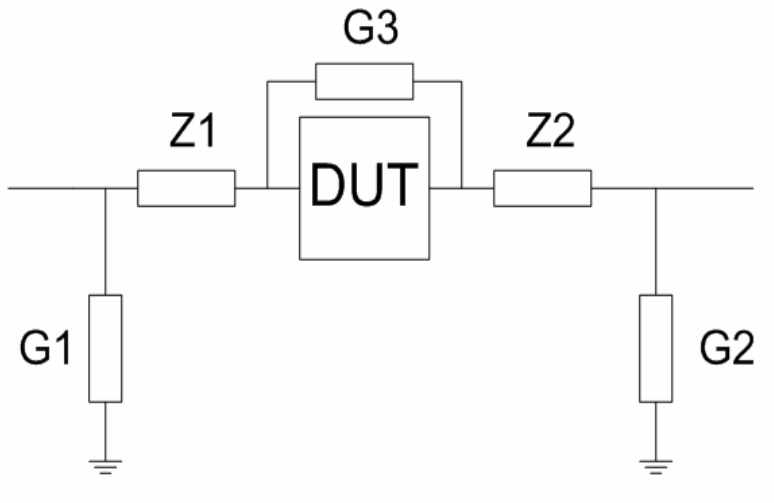
(c)

Fig.14. Chip diagram of (a) the PIN diode test structure, (b) open, and (c) through layout of the de-embedding structure.

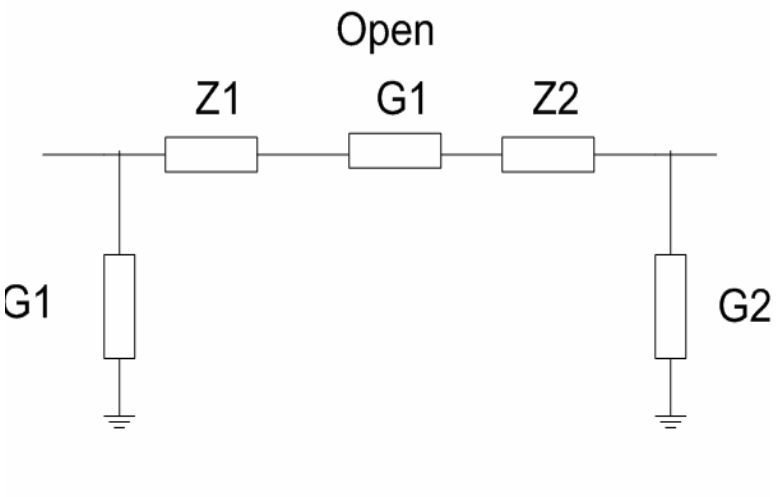
influence on the test structure stemming from the contact pads, the metal interconnection and coupling effects from the silicon substrate is subtracted from the RF behavior of the actual device under test (DUT).

For the PIN diode, bias voltages for anode and cathode are provided from the bias tee and only two ports are used in the test structure. The layout of the RF test-structure and the corresponding on-wafer de-embedding structure, i.e., open and through structures which are needed for the de-embedding procedure, are shown in Fig. 14. The chip diagram of the pads and the metal interconnections is identical for the test structure and the de-embedding structure.

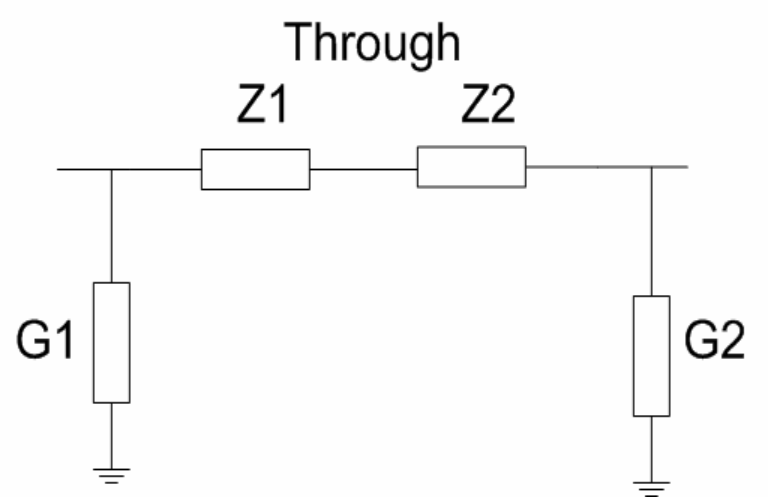
The basic assumption in the de-embedding procedure comes from the theory that the effect of parasitics in the de-embedding layout structure can be represented as equivalent admittances and impedances shown in Fig. 15. Thus, the electrical behavior of the DUT is influenced by the parasitic admittance G_1, G_2 and G_3 and the parasitic impedances Z_1 and Z_2 .The admittance G_1 G_2 and G_3 represents the coupling via the metal interconnections and the silicon substrate between the pads of anode (port 1) and ground,



(a)



(b)



(c)

Fig.15. Equivalent schematic circuit of (a) RF test-structure, (b) open de-embedding structure, and (c) through de-embedding structure

cathode (port 2) and ground, and anode (port 1) and cathode (port 2), respectively. The impedances Z_1 and Z_2 originate from the metal interconnection's series impedance between port 1 and port 2, and the actual DUT.

By measuring the S-parameters of the on-wafer de-embedding structure and converting them to y-parameters, all parasitic admittance and impedance values can be calculated according to the following equations:

$$G_1 = y_{11op} + y_{12op} \tag{26}$$

$$G_2 = y_{22op} + y_{12op} \tag{27}$$

$$G_3 = (-1/y_{12op} + 1/y_{12th})^{-1} \tag{28}$$

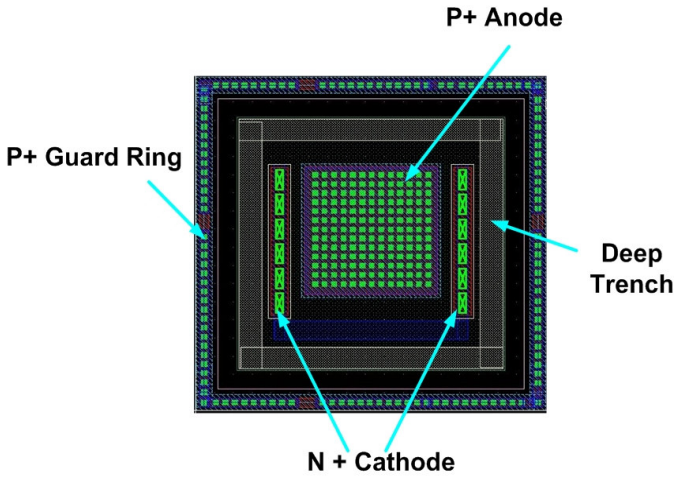
$$Z_1 = Z_2 = -1/(2y_{12th}) \tag{29}$$

where the y_{11op}, y_{12op} and y_{22op} is the measured y-parameter of the open structure and y_{12thr} is measured y-parameter of the through structure. After excluding the calculated parasitic admittance and impedance, an accurate DUT model is achieved.

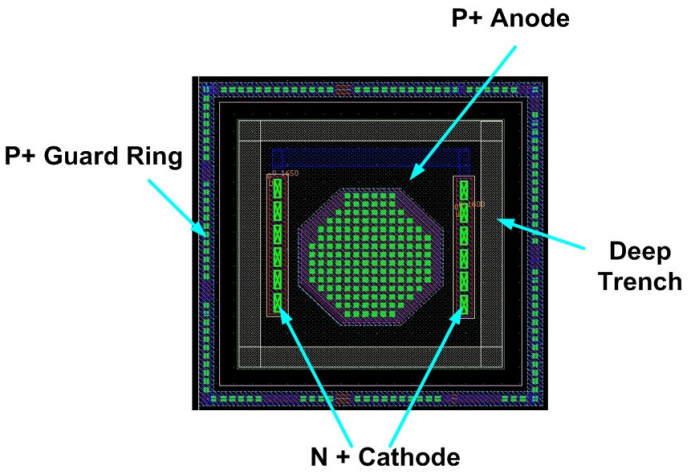
3.7 Measurement results for PIN Diode SPST switch

Various *SiGe* PIN RF switches with different geometries have been implemented in a standard 0.18-*μm* SiGe BiCMOS process to achieve low insertion loss, high linearity, and high power handling capability.

Six square and six octagonal PIN RF switches were implemented in a standard 0.18-*μm SiGe* BiCMOS process. Each geometry has two anode sizes, i.e., 25 μm^2 and 50 μm^2, and each size has three *ACDs*, i.e., 0.9 μm, 1.35 μm, and 1.8 μm, where the minimum ACD defined by the design rule is 0.9 μm. Fig. 16 shows the layout of the 50 μm^2 square and octagonal PIN diode with an ACD of 0.9 μm. The deep trench, double body-tie guard



(a)



(b)

Fig.16 50 μm^2 (a) square and (b) octagonal PIN diode layout in a standard SiG process.

rings are used to further improve isolation.

3.7.1 The DC measurement results of PIN diodes

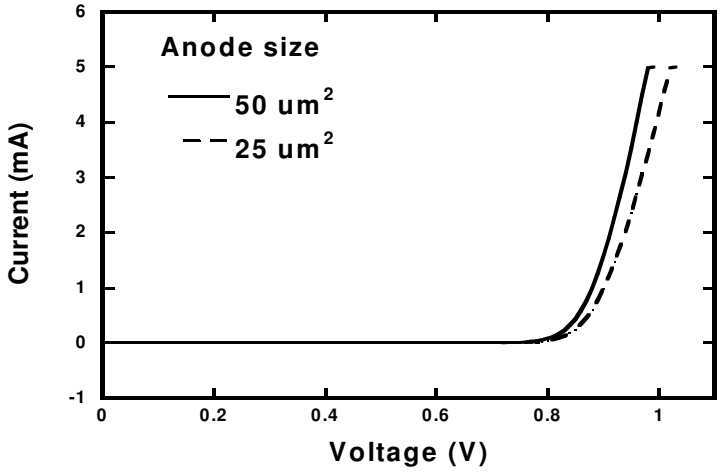
The DC measurements of the 25 μm^2 and 50 μm^2 octagonal PIN diodes with an ACD of 0.9 µm are shown in Fig. 17. For all diodes, the measured saturation current is around 10^{-18} A, and the junction reverse breakdown voltage V_b is -11 V at 300 K, respectively. The reverse saturation current is only around 10^{-10} A. Table I lists the I_S (saturation current), n (ideality factor) and I_R (reverse saturation current) for different sizes of

TABLE I
DC CHARACTERISTIC OF OCTAGONAL PIN DIODE SWITCHES
WITH THE ACD OF 0.9 μM

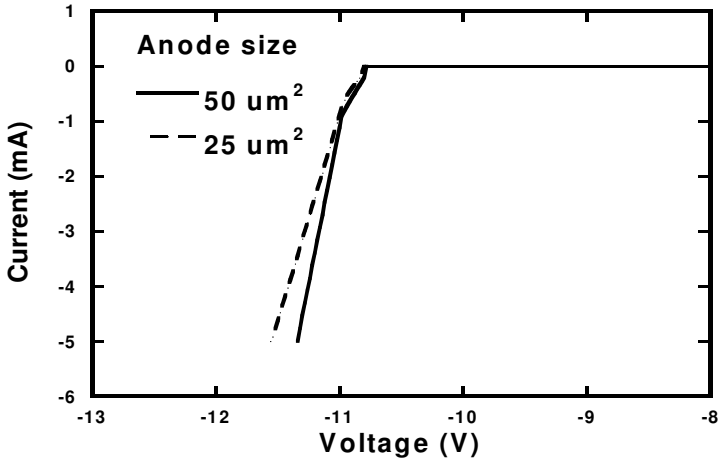
Anode size (μm^2)	Is (A)	n	I_R (A)	V_b (V)
50	$7.46x10^{-18}$	1.18	$3.27x10^{-10}$	-11
25	$2.49x10^{-18}$	1.02	$3.05x10^{-10}$	-11

octagonal PIN diode switches with the ACD of 0.9 μm. The square PIN diode switches show similar DC performance to octagonal PIN diode switches.

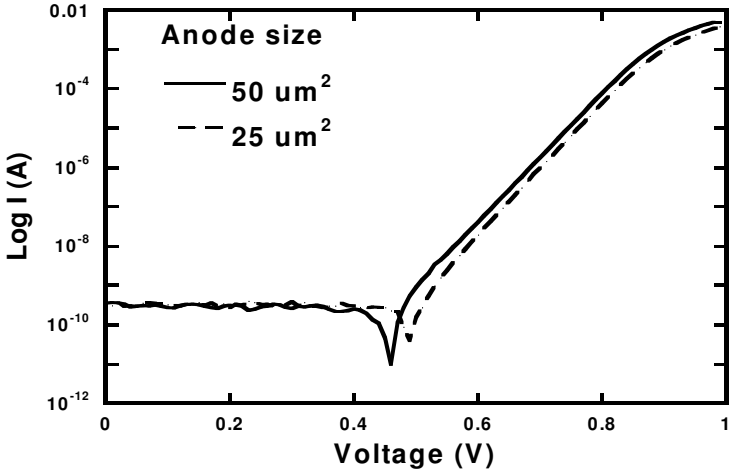
3.7.2 The RF measurement results of PIN diodes



(a)

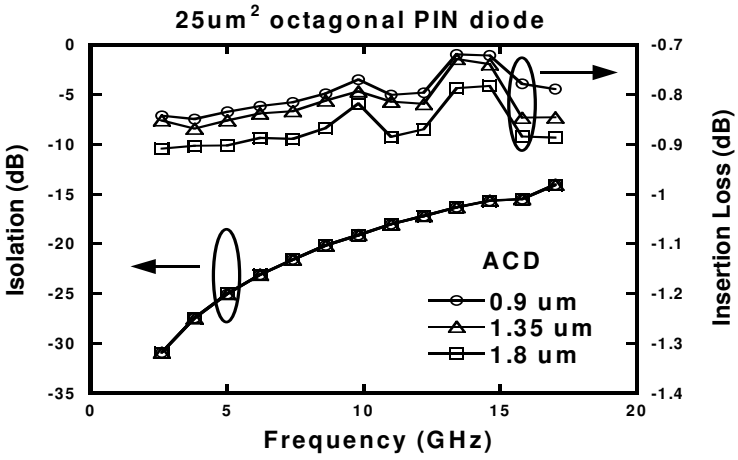


(b)

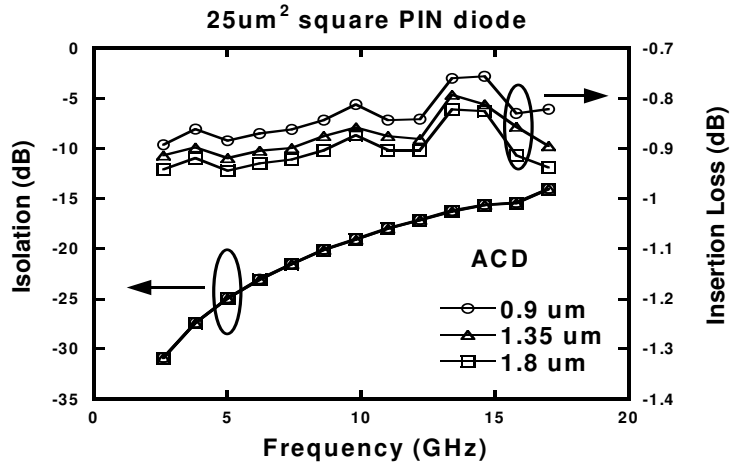


(c)

Fig. 17 Measured IV curves: (a) at the forward bias; (b) at the reverse bias; and (c) log current verse voltage of 25 μm^2 and 50 μm^2 octagonal PIN diode with ACD of 0.9 μm

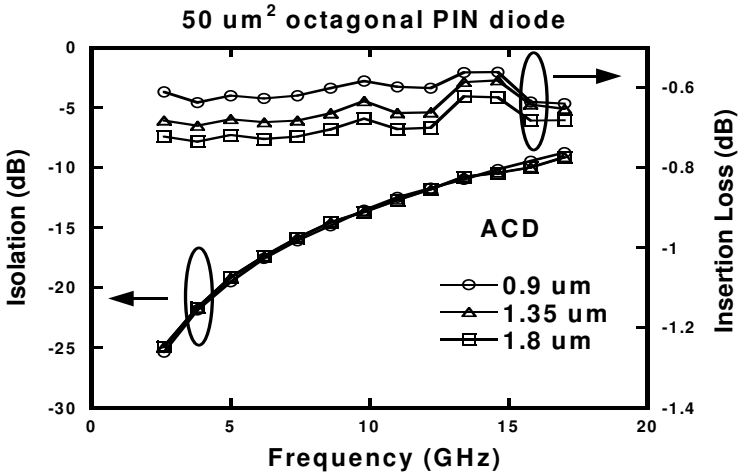


(a)

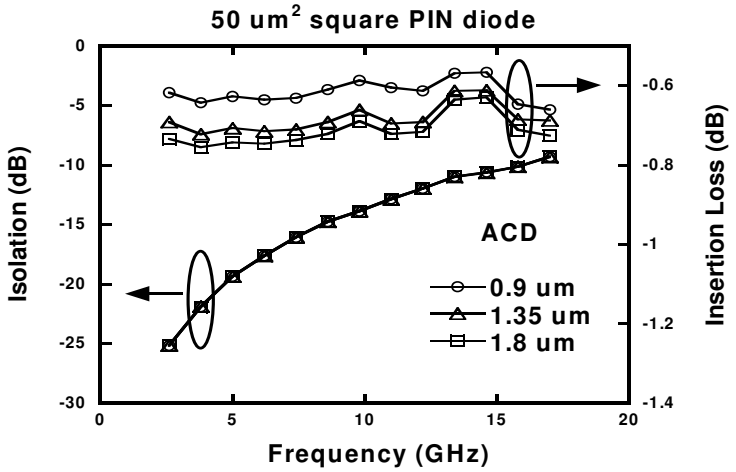


(b)

Fig. 18 Measured insertion loss and isolation of 25 μm^2: (a) octagonal PIN diode switch; and (b) square PIN diode switch (I_{FB} = 2 mA, V_{RB} = -1V)



(a)



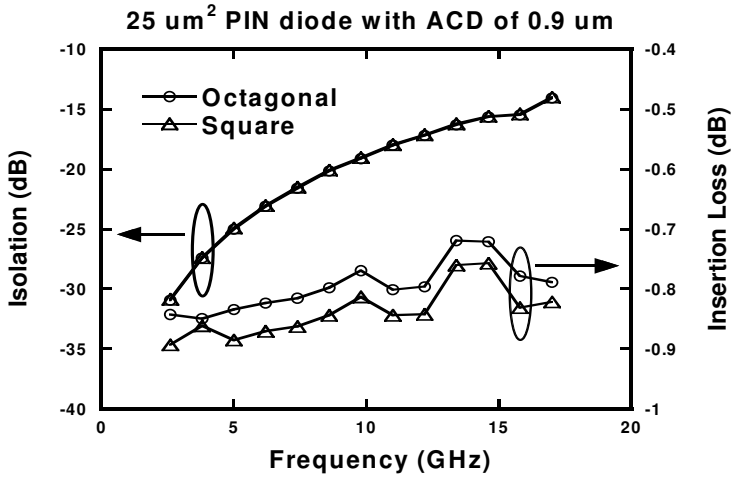
(b)

Fig. 19 Measured insertion loss and isolation of 50 μm^2: (a) octagonal PIN diode switch; and (b) square PIN diode switch (I_{FB} = 2 mA, V_{RB} = -1V)

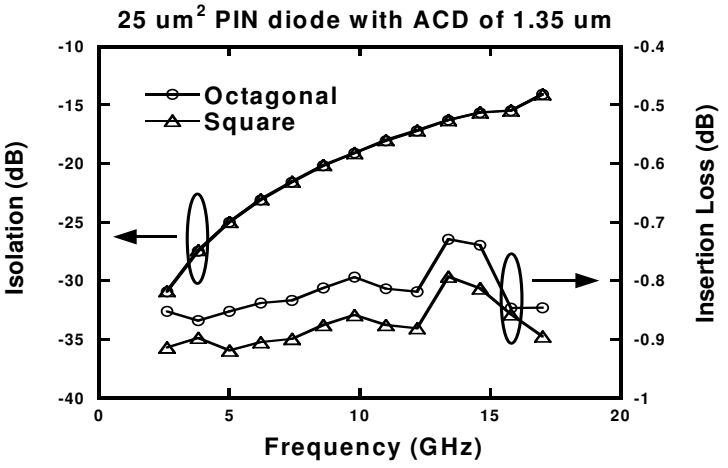
Dedicated two-port de-embedding structures are used for the RF performance of the switches. Measured insertion loss and isolation of the 25 μm^2 and 50 μm^2 PIN diode switches with ACD of 0.9 μm, 1.35 μm and 1.8 μm are shown in Fig. 18 and Fig. 19. When the ACD is reduced from 1.8 μm to 0.9 μm, the insertion loss is improved by 12.5% for 25 μm^2 octagonal PIN diode, 10.2% for 25 μm^2 square PIN diode, 15.3% for 50 μm^2 octagonal PIN diode and 13.3% for 50 μm^2 square PIN diode at 15 GHz. The

isolation shows very little variation with different ACD. By choosing PIN diode ACD as the minimum length defined by the design rule (i.e. 0.9 μm), the device can achieve the best insertion loss as expected from (14).

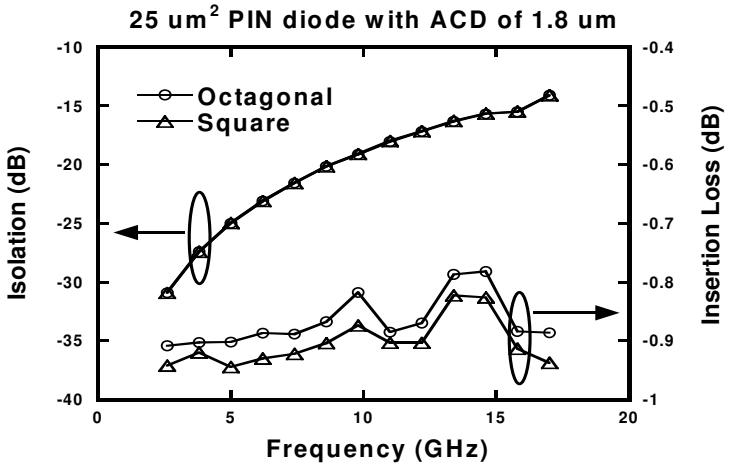
Based on (23), for a given PIN diode size, the octagonal geometry has a larger *P/A* ratio than a square one; therefore, it has smaller forward bias current and better insertion loss. The measurement results in Fig. 20 validate this trend. At 15 GHz, for 25 μm^2 PIN diode switches, the octagonal geometry gives an average of 2.38 % improvement in insertion loss over the square geometry for an ACD of 0.9 μm, 1.35 μm and 1.8 um. For 50 μm^2



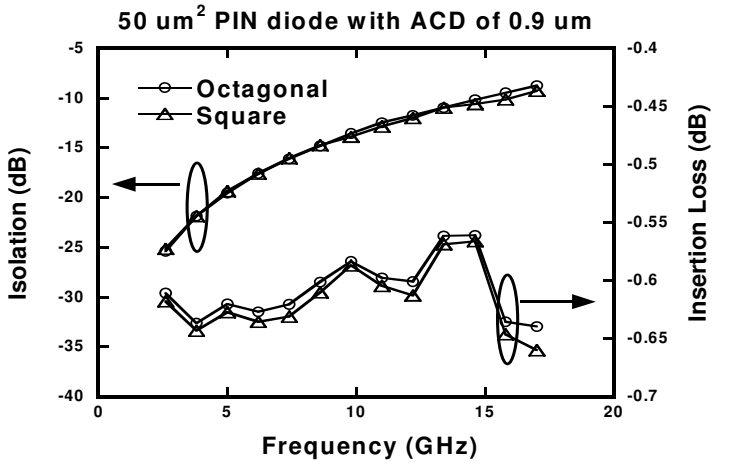
(a)



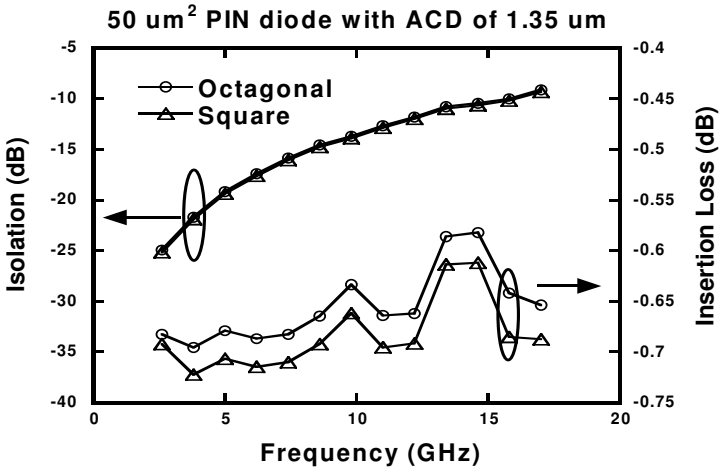
(b)


25 um2 PIN diode with ACD of 1.8 um
Octagonal
Square
Isolation (dB)
Insertion Loss (dB)
Frequency (GHz)
-10
-15
-20
-25
-30
-35
-40
-0.4
-0.5
-0.6
-0.7
-0.8
-0.9
-1
0
5
10
15
20

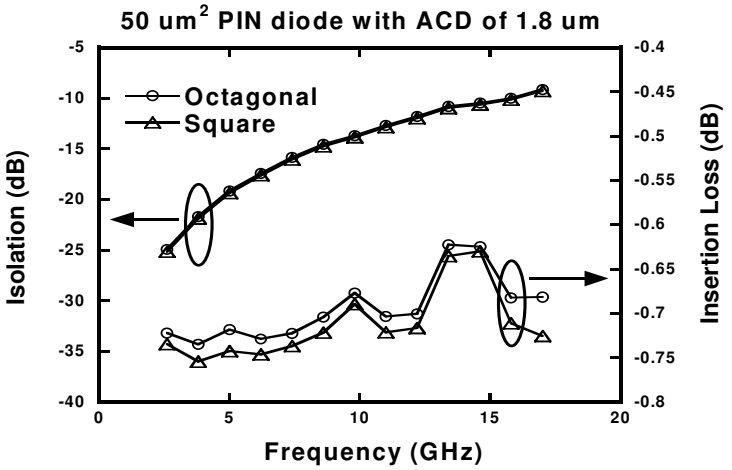
(c)


50 um2 PIN diode with ACD of 0.9 um
Octagonal
Square
Isolation (dB)
Insertion Loss (dB)
Frequency (GHz)
-5
-10
-15
-20
-25
-30
-35
-40
-0.4
-0.45
-0.5
-0.55
-0.6
-0.65
-0.7
0
5
10
15
20

(d)


50 um2 PIN diode with ACD of 1.35 um
Octagonal
Square
Isolation (dB)
Insertion Loss (dB)
Frequency (GHz)
-5
-10
-15
-20
-25
-30
-35
-40
-0.4
-0.45
-0.5
-0.55
-0.6
-0.65
-0.7
-0.75
0
5
10
15
20

(e)



(f)

Fig. 20 Insertion loss and isolation of 25 μm^2 octagonal and square PIN diode switches with ACD of (a) 0.9 µm, (b) 1.35 µm and (c) 1.8 µm; insertion loss and isolation of 50 μm^2 octagonal and square PIN diode switches with ACD of (d) 0.9 µm, (e) 1.35 µm and (f) 1.8 µm. (I_{FB} = 2 mA, V_{RB} = -1V)

PIN diodes, the octagonal geometry devices show an average of 3.57 % improvement in insertion loss over the square geometry at 15GHz.

Measured input P_{1dB} of 50 μm^2 PIN diode switches with an *ACD* of 0.9 um at I_{FB} = 2 mA is shown in Fig. 21. The input P_{1dB} for octagonal geometry is 15 dBm, which is 1 dB improvement over the square geometry. The P_{1dB} of 50 μm^2 PIN diode with different ACD shows similar P_{1dB} performance. Fig. 22 (a) and (b) gives the comparison data of P_{1dB} measurement for 50 μm^2 square and octagonal PIN diode switches at different cathode voltages. The measurement data show that the diode with positive cathode bias of 2 V shows 1dB higher P_{1dB} than the grounded cathode in both octagonal and square anode cases, which supports our theoretical analysis.

From the aforementioned analysis and measured data, octagonal geometry devices with an ACD of 0.9 µm have the best insertion loss, isolation and P_{1dB} performance. The

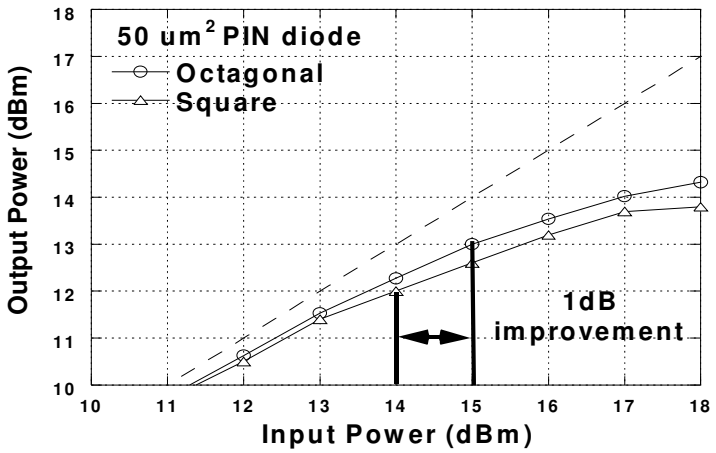
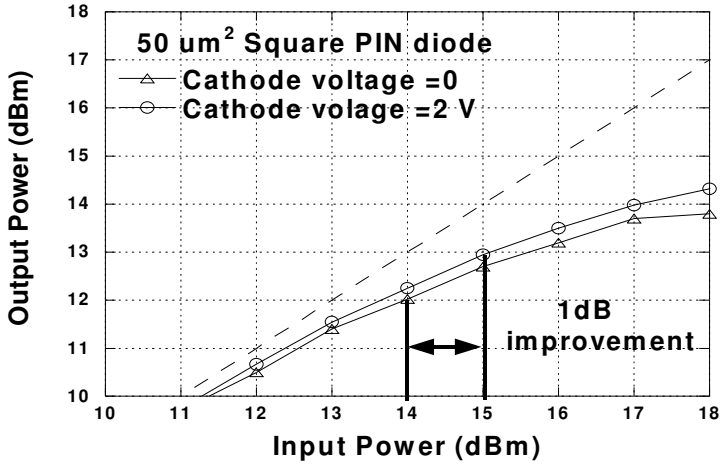
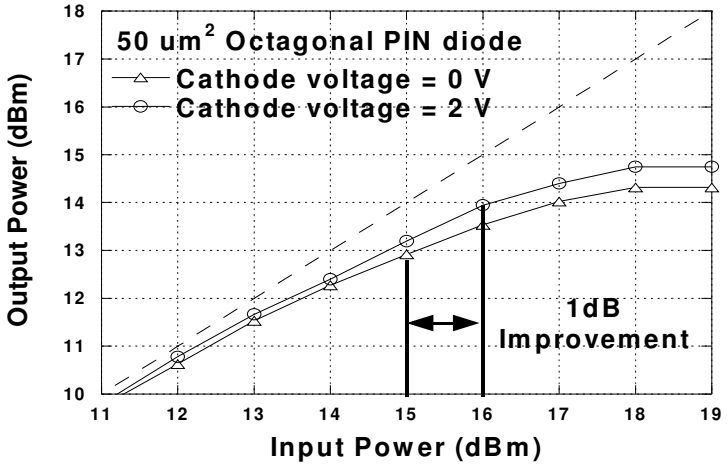


Fig. 21 Measured data of P_{1dB} compression point of 50 μm^2 octagonal and square PIN diode switches (I_{FB} = 2 mA)

models of 25 μm^2 and 50 μm^2 octagonal PIN diode switches with ACD of 0.9 μm are developed from S-parameters measuring an on-wafer RF probe system. These models can be used for high isolation RF switches, variable attenuators and phase shifter design in phased array applications. The forward bias models are developed at the bias current of 2 mA. The reverse bias models are obtained at the reverse bias voltage of 1 V. Tables II and III show the model parameter values for 25 μm^2 and 50 μm^2 PIN diode switches according to the corresponding parameters shown in Fig. 23. For the 25 μm^2 PIN diode, the average return loss is around 22 dB from 2 to 18 GHz. The insertion loss is lower than 0.85 dB, and isolation is between 15 dB and 32 dB. The 50 μm^2 PIN diode switch shows a flat return loss around 25 dB. The insertion loss is lower than 0.65 dB, and the isolation is between 27 dB and 9.7 dB at the given frequency band. This insertion loss at the X and Ku band is the best value reported for a standard 0.18-*μm* SiGe PIN diode switch with the same anode size. The isolation of this PIN diode switch is also comparable to the performance reported in [10]-[14].



(a)



(b)

Fig. 22 Measured data of P_{1dB} compression point with positive cathode voltage for 50 μm^2 (a) square PIN diode switch and (b) octagonal PIN diode switch (I_{FB} = 2 mA)

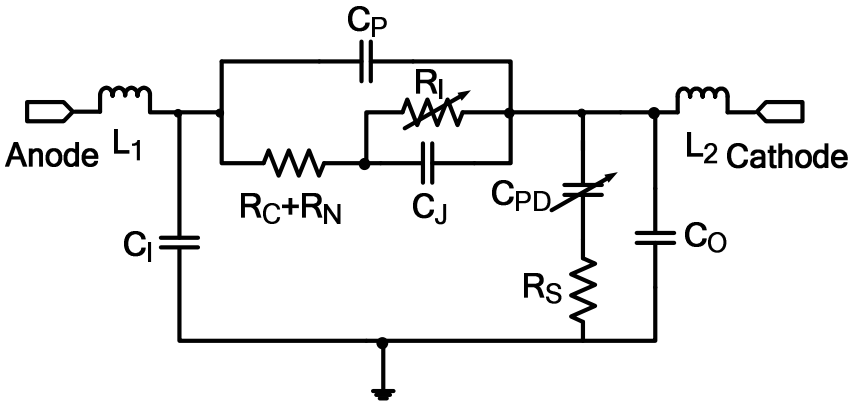
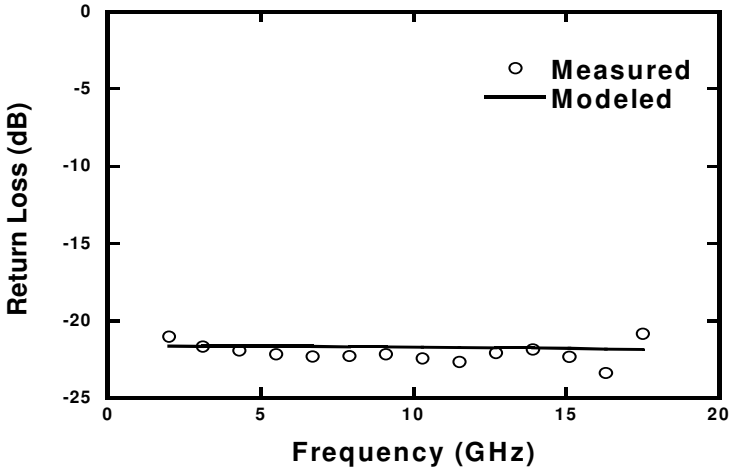
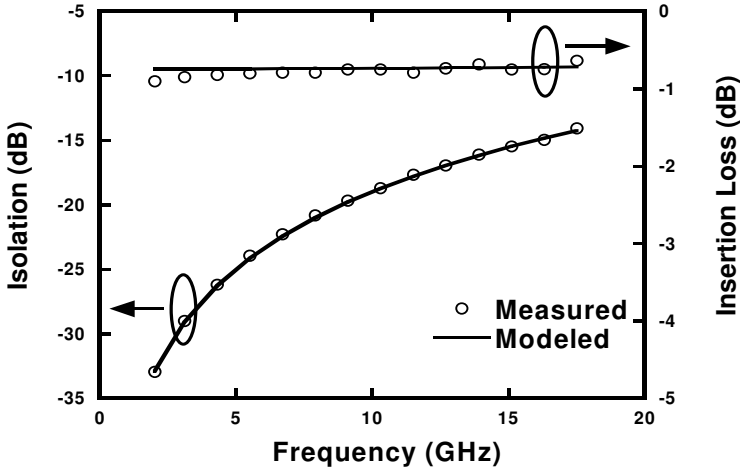


Fig. 23 Equivalent circuit model of the octagonal PIN diode SPST switch



(a)



(b)

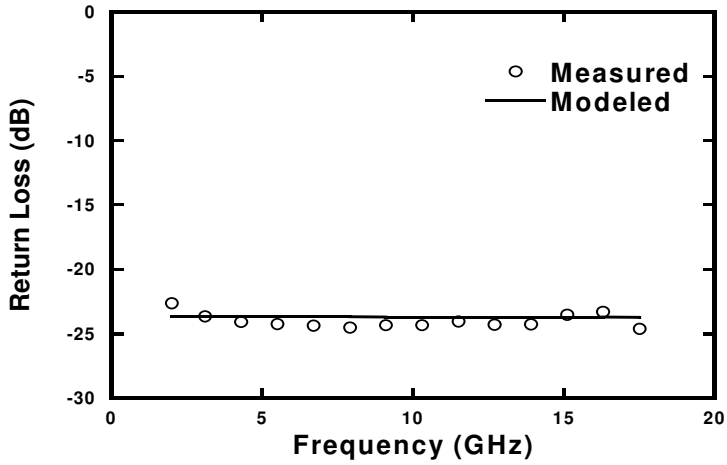
Fig. 24 Measured and modeled results of series 25 μm^2 PIN diode switch (a) return loss and (b) insertion loss and isolation

TABLE II
CIRCUIT MODEL PARAMETERS OF 25- μm^2 PIN DIODE WITH ACD OF 0.9 μm

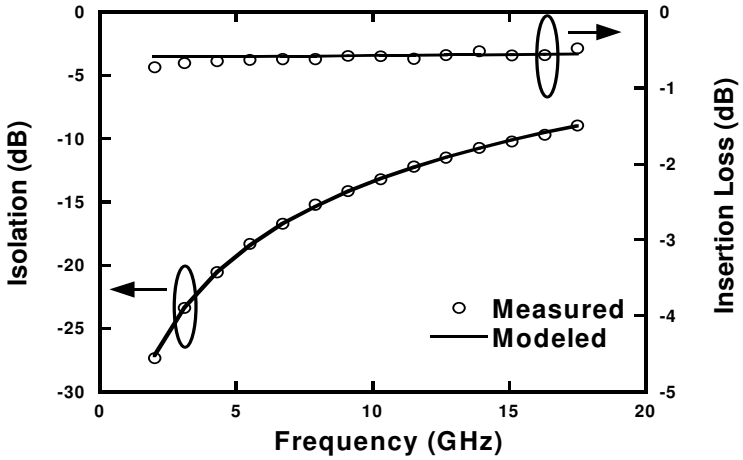
	ON (I_D =2mA)	**OFF(V_{RB}=1V)**
L_1,L_2	Layout determined	Layout determined
R_C+R_N	4.431 Ω	4.431 Ω
R_I	4.362 Ω	100 MΩ
C_J	1.005 pF	0.018 pF
C_P	0.0001 pF	0.0001 pF
C_I	0.002 pF	0.002 pF
Co	0.005 pF	0.005 pF
Rs	203 Ω	203 Ω
C_{PD}	0.004 pF	0.001 pF

TABLE III
CIRCUIT MODEL PARAMETERS OF 50- μm^2 PIN DIODE WITH ACD OF 0.9 μm

	ON (I_D = 2mA)	**OFF(V_{RB} = 1V)**
L_1,L_2	Layout determined	Layout determined
R_C+R_N	3.512 Ω	3.512 Ω
R_I	3.442 Ω	100 MΩ
C_J	1.003 pF	0.032 pF
C_P	0.0001 pF	0.0001 pF
C_I	0.001 pF	0.001 pF
Co	0.003 pF	0.003 pF
Rs	203 Ω	203 Ω
C_{PD}	0.003 pF	0.001 pF



(a)



(b)

Fig. 25 Measured and modeled results of series 50 μm^2 PIN diode switch (a) return loss and (b) insertion loss and isolation

3. 8 The PIN diode TID test:

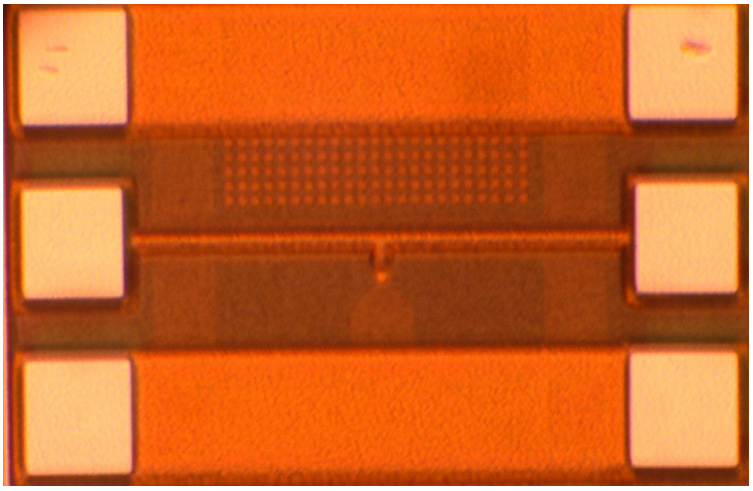
Cressler et al.[28] have demonstrated that IBM's SiGe HBT technology is radiation tolerant to nearly a Megarad(Si), while CMOS is tolerant to nearly 75Krad(Si). However, HBT device has a leakage current under total dose radiation test and this leakage will degrade the performance of MMICs in moderate radiation environment. Marshall et al. [29] evaluated heavy ion and pulsed laser Single Event Upset (SEU) susceptibility of a circuit hardening attempt in IBM's HBT for a potential SEU critical application. This study showed SiGe HBT technology to be sensitive to SEU. However, this SEU causes

only a glitch in the RF and microwave signal of MMICs resulting in a bit error without causing severe communication errors [1].

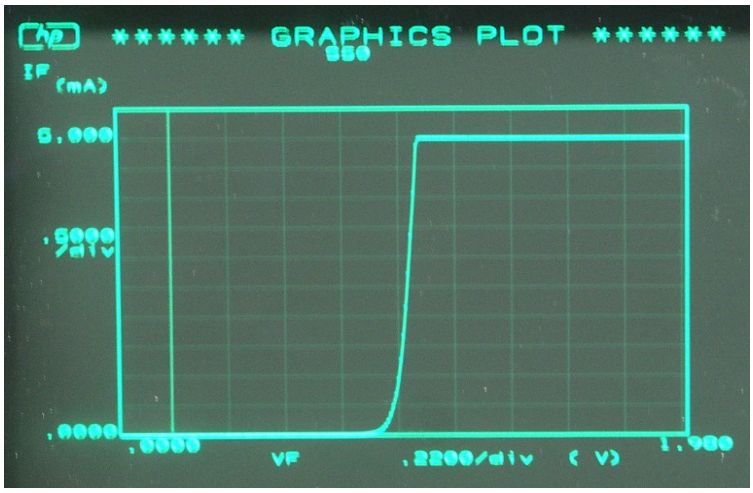
In this dissertation, we focused on the total dose radiation-tolerant SiGe BiCMOS MMICs. Using the X and Ku band SiGe MMICs, we performed pre and post total dose radiation tests up to 1000k rad(Si). Comparing the results between pre and post radiation tests, it shows that the MMICs developed in this project have high radiation tolerant.

The octagonal PIN diode is used for switch, attenuator and phase shifter design. As we have mentioned, compared with the rectangle and square design at given anode size, the octagonal shape has smaller periphery-to-area ratio. The effective minority carrier life time is determined by the recombination occurring at the bulk intrinsic region and surface recombination occurring at the diode periphery. The boundary of the PIN diode causes imperfections in the regular array of crystal atoms that creates energy states within the otherwise disallowed bandgap of the silicon. Therefore, its peripheral recombination probability is much larger when compared to a silicon crystal of infinitely extended dimensions [4]. Small periphery-to-area ratio (*P/A*) is desirable for PIN diode design because the long minority carrier lifetime can reduce the current-based resistance, while also improving radiation tolerance of the device by reducing the lifetime killing effects introduced by radiation exposure. Thus, the MMICs designed with octagonal PIN diode have better radiation tolerant performance than the ones with square and rectangle PIN diodes.

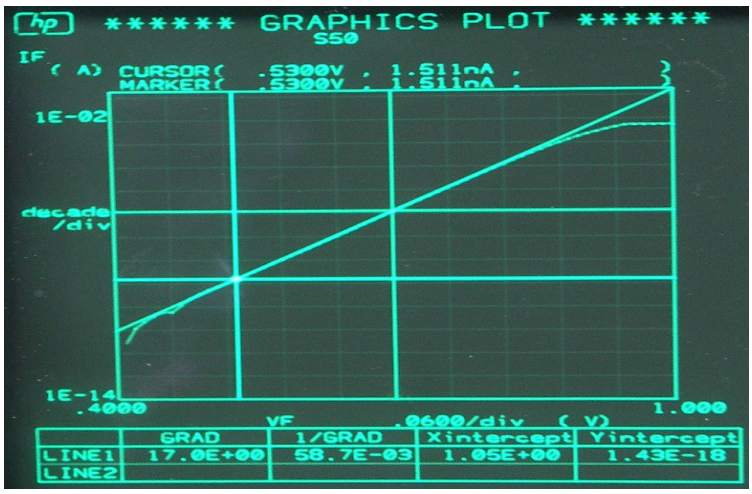
The pre-radiation dc test is performed for a 50-μm^2 shunt PIN diode. Fig. 26 (a) shows the micrograph of a 50-μm^2 shunt PIN diode with a transmission line connected to the PIN diode's anode and cathode terminals. The PIN diode DC measurement



(a)



(b)

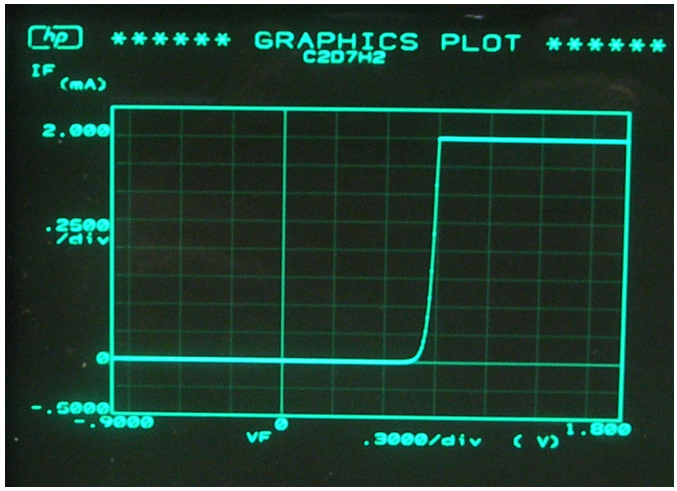


(c)

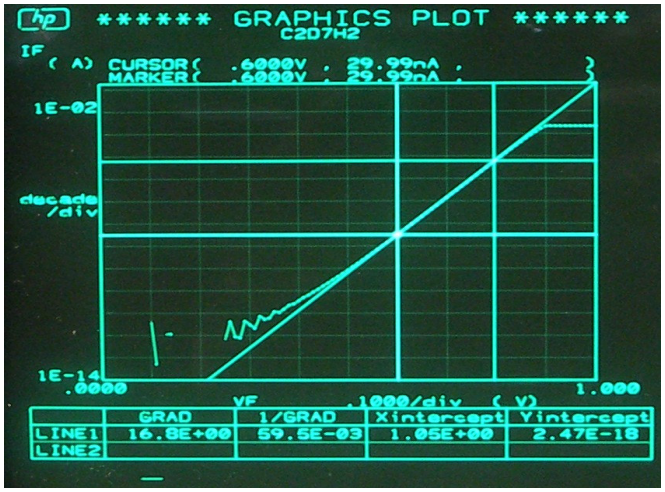
Fig. 26 (a) Chip diagram of 50 μm^2 PIN diode, (b) DC I-V characteristic and (c) Log (I) versus voltage before TID test

performance is shown in Fig. 26(b) and 26 (c). The saturation current *Is*, the ideality factor and the junction reverse breakdown voltage V_b are found to be *Is* = 1.47 x 10-18, *n* = 1.001, at *T* = 300 K, and V_b =-11V respectively.

A radiation evaluation was performed on the PIN diode in DIP 14 package, to determine the total dose tolerance of these parts. The irradiation was performed at the Boeing Radiation laboratory using a GAMMACELL 220 EXCEL (GC-220E). Data points were captured after irradiation levels 250, 350, 450, 650 and 1000 Krads. The



(a)



(b)

Fig. 27 50-µm^2 shunt diode after TID test (a) DC I-V characteristics, (b) Log (I) versus voltage

dose rate was 234 rads/s (Si). Higher dose rate Total Ionizing Test (TID) was not performed due to limited test time in Boeing Radiation laboratory. Fig. 27 shows the 50 μm^2 shunt diode's DC performance after TID test. After 1000 krad dose radiation, Is = 2.47 x 10^{-18} A, n = 1.0021, at T = 300 K, and V_b =-10 V.

The performance of saturation current, ideal factor and breakdown voltage has demonstrated a strong degree of hardness to TID radiation. Due to the device's robustness, it is usable in applications where it is subjected to Gamma radiations of up to 1000 krads.

CHAPTER FOUR

HIGH ISOLATION, LOW INSERTION LOSS PIN DIODE SWITCH DESIGN

The T/R switch is of crucial importance for the accuracy of the phase and amplitude control in combination with the maximum control range. It is a key building block in phased array communication systems. PIN diodes enable new design approaches for the SPDT switch improving both isolation and insertion loss. The low insertion loss, high isolation PIN diodes have been modeled in Jazz SBC18 SiGe process and are used to implement a high performance SPDT switch.

4.1 Conventional SPDT PIN diode switch design

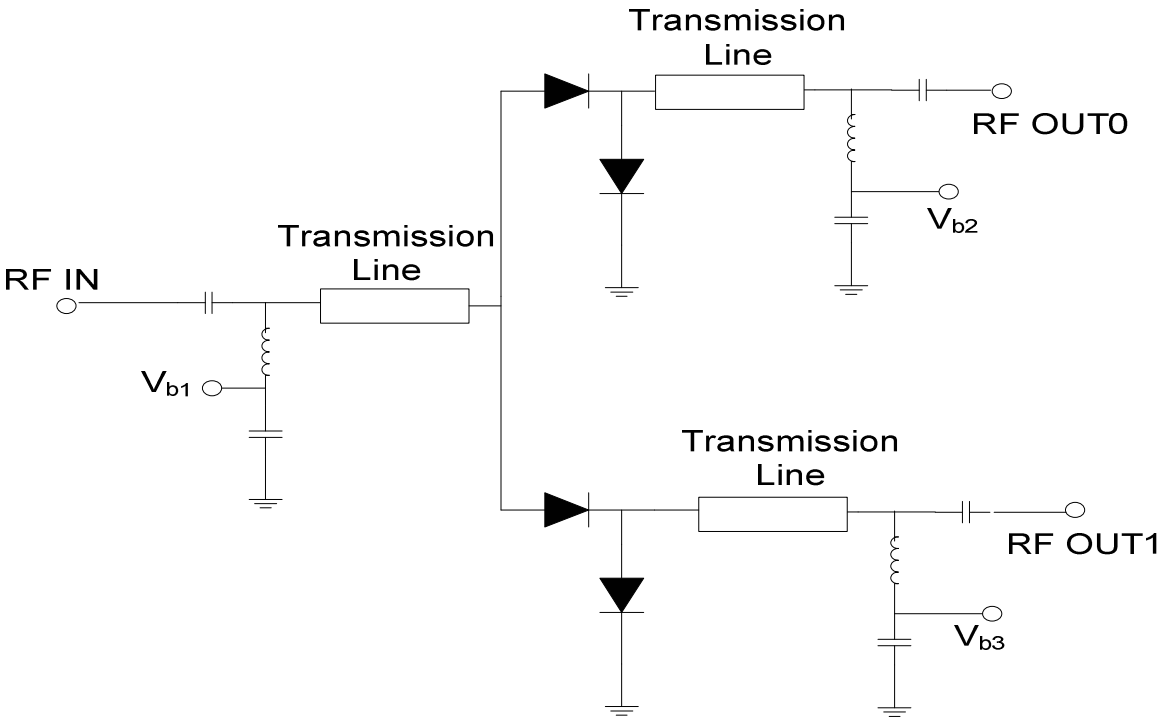


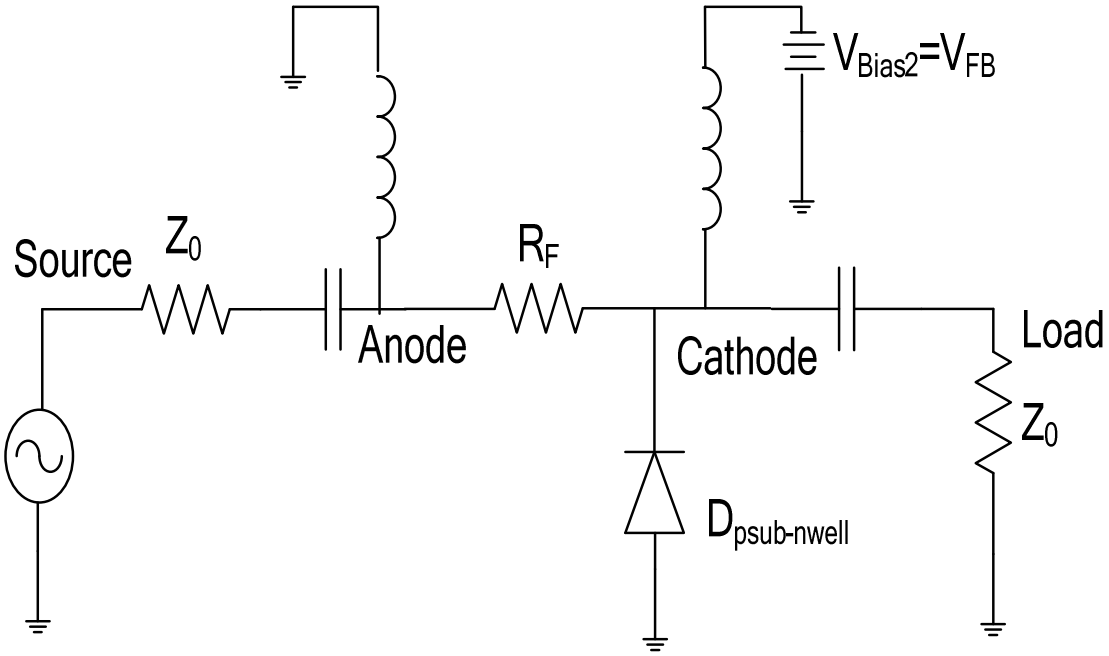
Fig. 28 SPDT switch chip schematic

The conventional series-shunt SPDT structure is favored in most broadband switch designs. Fig.28 shows the SPDT switch schematic having a series-shunt diode combination in each arm. This topology was chosen as the best compromise between minimizing the insertion loss and maximizing the isolation.

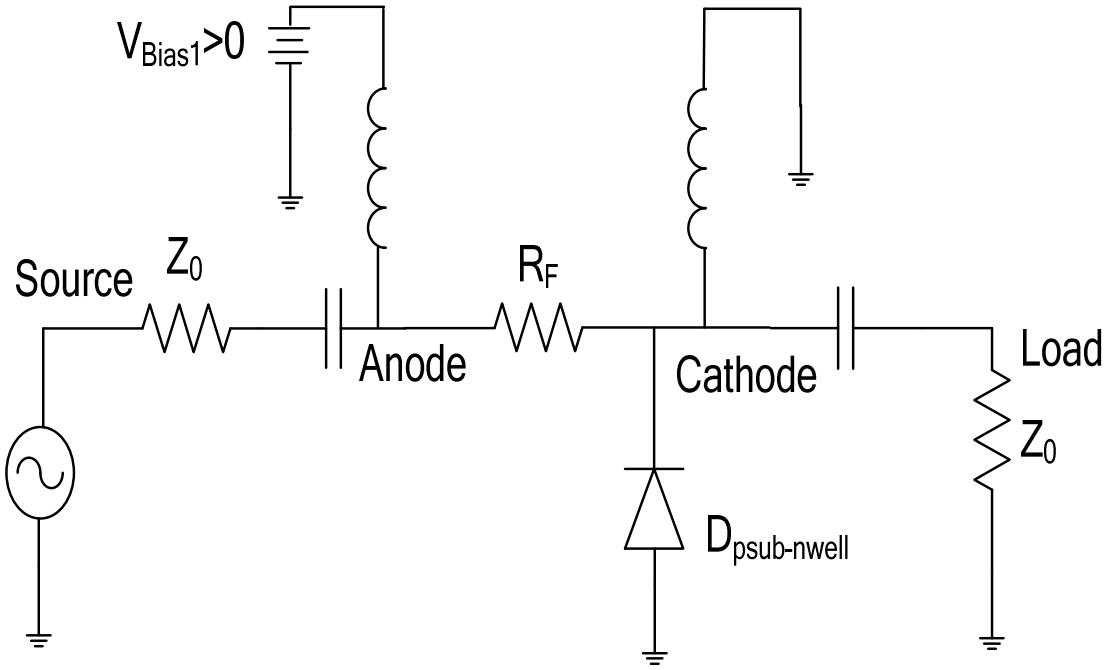
A through path between RFIN and RFOUT1 exists when $V_{b2} > V_{on}$ and $V_{b1} = 0$, the V_{FB} is the forward bias voltage of the PIN diode switch to achieve a given amount of forward bias current, causing the series diode to become forward biased while the shunt diode is reversed biased. Similarly, an isolation path exists between ports RFIN and RFOUT2 when V_{b3} is reverse biased and the shunt diode is forward biased to maximize the switch isolation. However, this design doesn't consider the effects of *Psub-Nwell* parasitic diode, which degrades the circuit's insertion loss.

4.2 The effect of parasitic diode at negatively biased cathode

Fig. 29 illustrates two bias conditions for the parasitic *Psub-Nwell* diode, which result in different insertion loss performance. The resistance R_F represents the PIN diode's forward bias resistance, V_{bias1} is the anode bias voltage, V_{bias2} is the cathode bias voltage, where the V_{FB} is the forward bias voltage of the PIN diode switch to achieve a given amount of forward bias current. In Fig.29 (a), the anode is shorted to ground through the inductor and the cathode is biased at the $-V_{FB}$ to turn on the PIN diode. However, at the same time, the parasitic diode *Psub-Nwell* diode is also forward biased and there is leakage through the parasitic diode to the ground that degrades the insertion loss. Fig.29 (b) demonstrates another bias method for removing the PIN diode forward bias leakage. In this case, the anode is biased at V_{FB} and the cathode is shorted to ground, the parasitic



(a)



(b)

Fig. 29 Simplified large-signal models for a forward biased series PIN diode with cathode: (a) negatively biased and (b) grounded

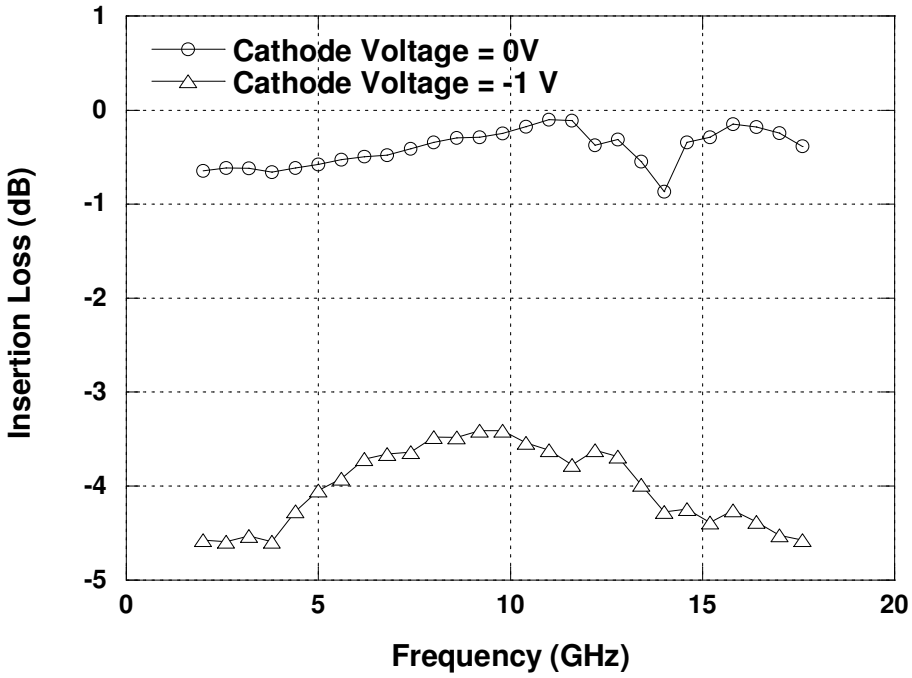
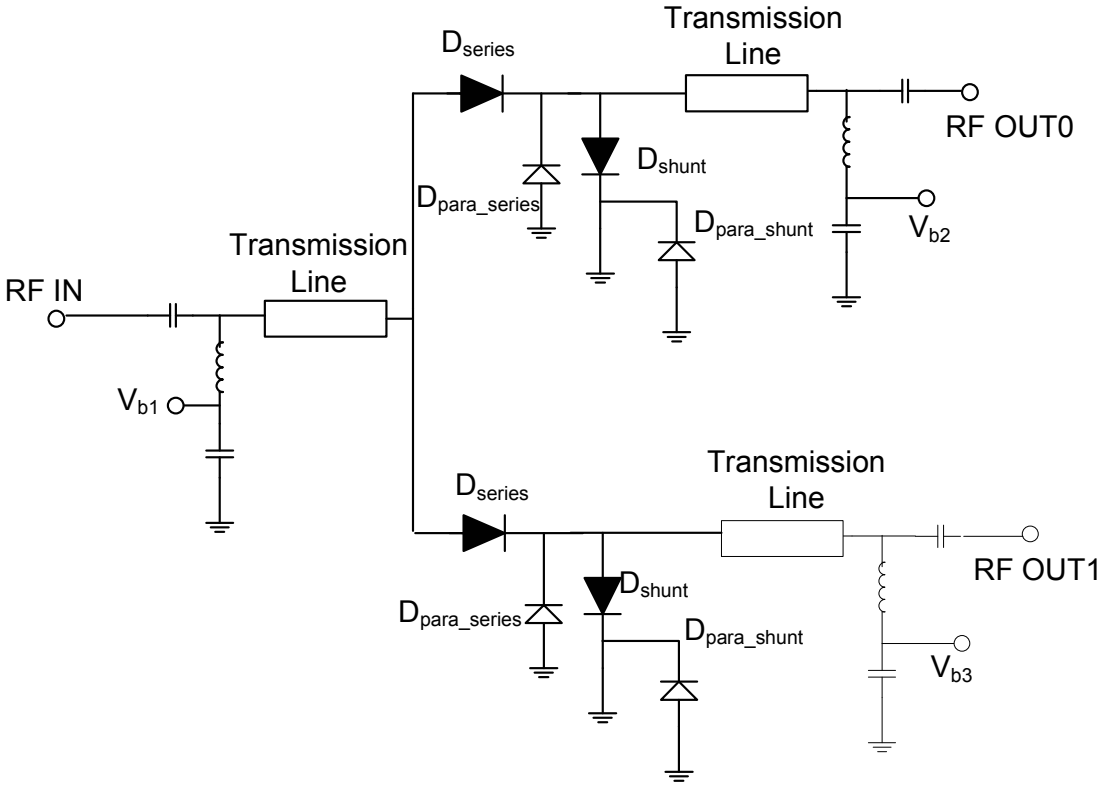


Fig. 30 Measured data of insertion loss of 25 μm^2 octagonal PIN diode switch with different cathode bias octagonal and square (I_{FB} = 1 mA)

diode is turned off and the loss in the substrate is avoided. As the Fig. 30 shows, for 25-um^2 octagonal PIN diode, the grounded biased cathode shows more than 3 dB improvement in insertion loss than the negatively biased cathode case.

4.3 New configuration PIN Diode SPDT switch

Fig.31 (a) shows the conventional SPDT switch. In this design, the through path between RFIN and RFOUT1 exists when $V_{b2} < -V_{RF}$ and $V_{b1} = 0$, where V_{FB} is the forward bias voltage of the PIN diode switch to achieve a given amount of forward bias current, causing the series diode to become forward biased while the shunt diode is reversed biased. Similarly, an isolation path exists between ports RFIN and RFOUT2 when series diode is reverse biased and the shunt diode is forward biased to maximize



(a)

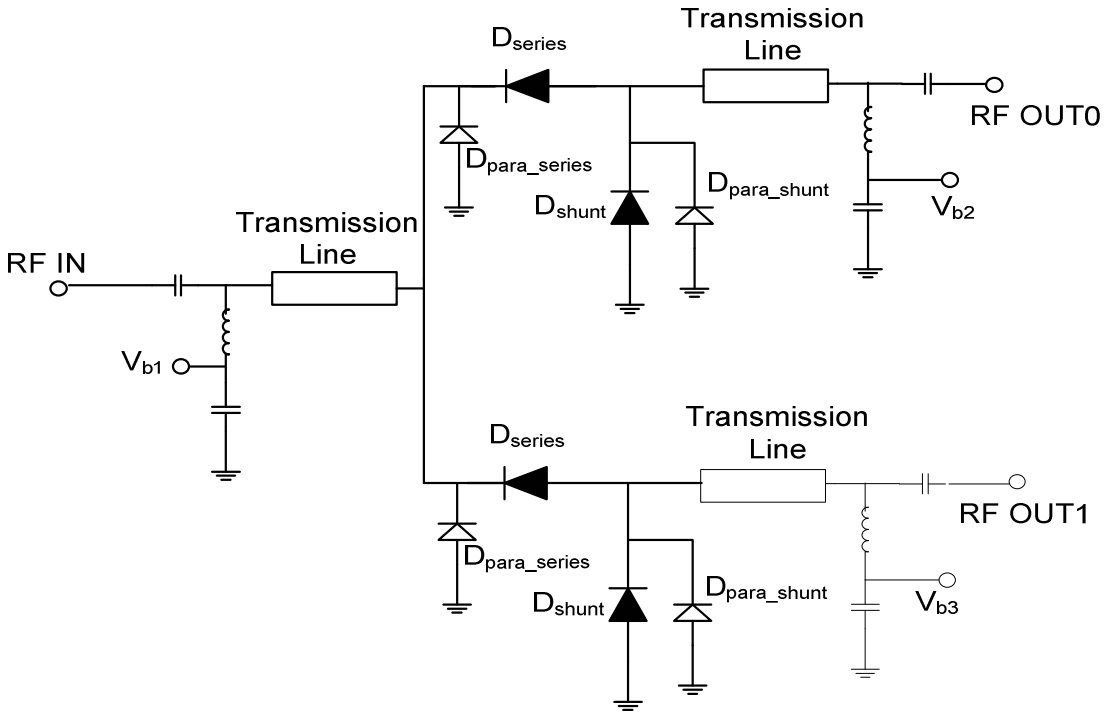


Fig.31 (a) Conventional (b) improved series-Shunt PIN diode SPDT switch

the switch isolation. However, in the through path, the *Psub-Nwell* parasitic diode D_{para_series} from series arm PIN diode D_{series} is in opposite direction of the shunt arm PIN diode D_{shunt}. Thus, when D_{shunt} is reverse biased, the D_{para_series} is forward biased and cause series leakage in the through path. For the D_{para_shunt}, its cathode and anode are both shorted to the ground and thus doesn't affect the insertion loss.

The leakage problem in the conventional design can be improved by changing the direction of the series-shunt arm connection. As shown in Fig.31 (b), the series-shunt arms are connected in the opposite direction than in the conventional design. In this case, the through path between RFIN and RFOUT1 exists when $V_{b2} > V_{RF}$ and $V_{b1} = 0$, causing the series diode to become forward biased while the shunt diode is reversed biased. Similarly, an isolation path exists between ports RFIN and RFOUT2 when the series diode is reverse biased and the shunt diode is forward biased to maximize the switch isolation. In the through path, since both the cathode and anode of the $D_{para\text{-}series}$ are at ground voltage, the D_{para_series} is turned off and this alleviates the leakage problem. For the D_{para_shunt}, its cathode and anode at the same direction as the shunt diode D_{shunt} and thus, doesn't affect the insertion loss.

4.4 The device selection for SPDT switch implementation

The SPDT switch schematic has a series-shunt diode combination in each arm. This topology was chosen as the best compromise between minimizing the insertion loss and maximizing the switch isolation.

For the series PIN diode, the 6.25 μm^2 diode is used since it has low junction capacitance, and therefore, high isolation. The 50 μm^2 PIN diode is used for the shunt

connection since it has low insertion loss. This combination results in high isolation while maintaining low insertion loss.

4.5 The measurement results of SPDT switch

The switch measurements are performed on wafer. Fig. 32 shows the SPDT chip photograph. The chip size is only 560um×382um. Short 50 ohm transmission lines are used to reduce the chip size. Off-chip bias networks are also employed to get small chip size. Fig.33 shows the measured insertion loss, isolation and return loss. A through-path loss of 1.2 to 1.8 dB and an isolation path loss of 51 to 36 dB over a wide frequency range (2 to 18 GHz) have been measured. The retune loss of switches is less than 14 dB between 2 and 18 GHz.

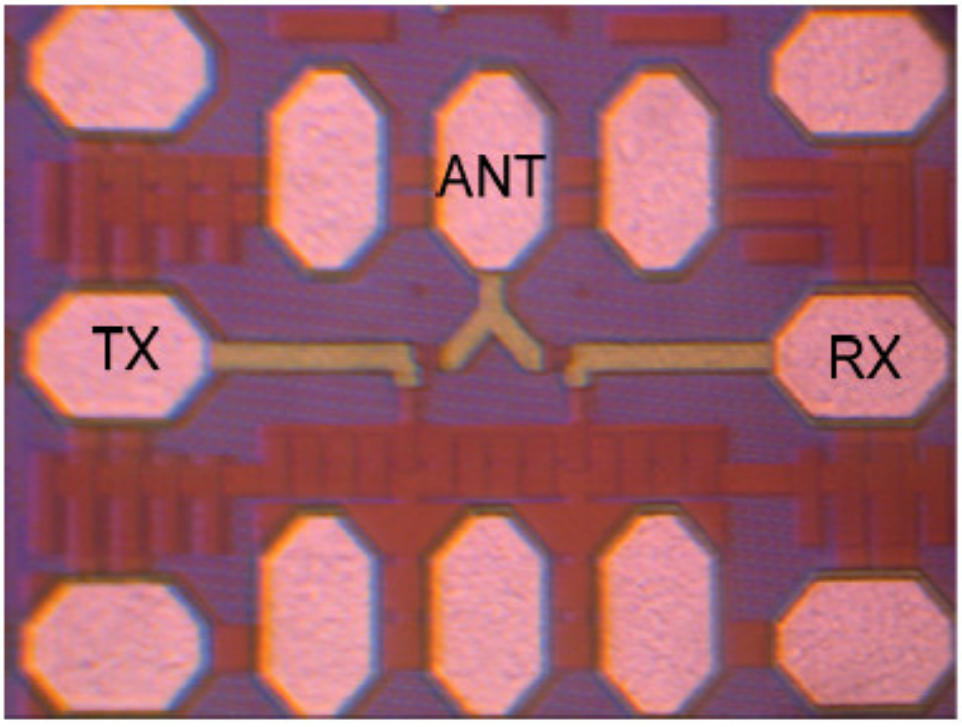
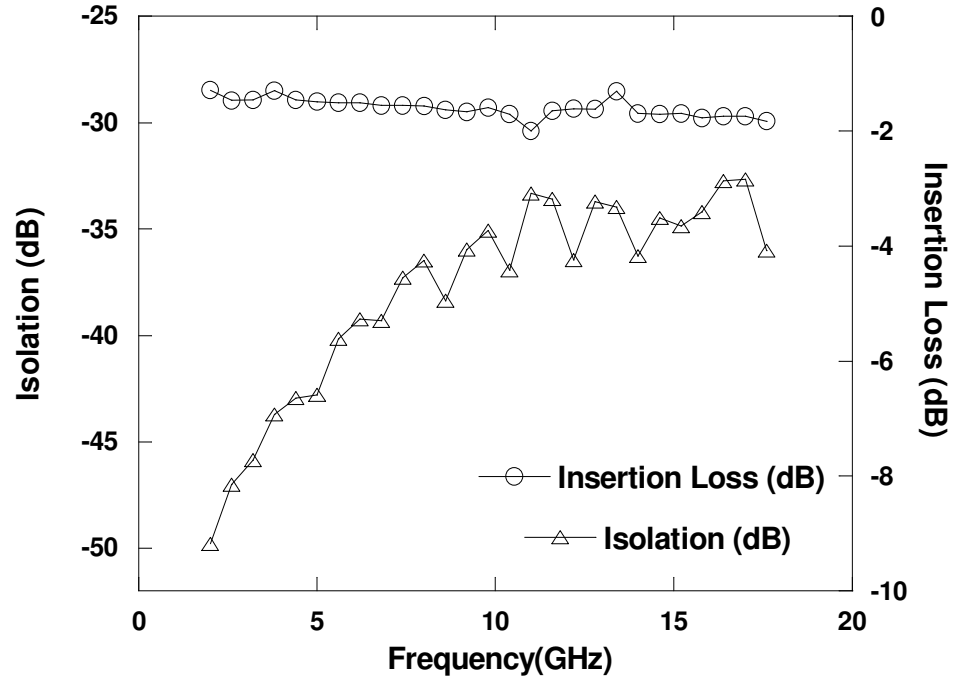
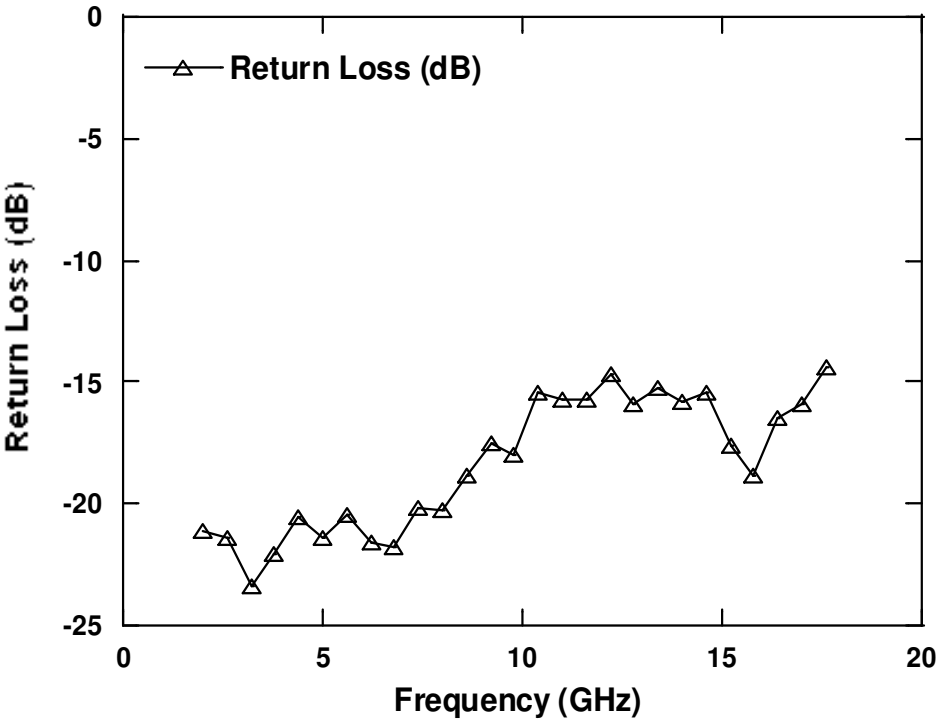


Fig. 32 SiGe SPDT Switch Chip (560um×382um)



(a)



(b)

Fig.33 Measured SPDT switch performance (a) insertion loss and isolation (b) return loss

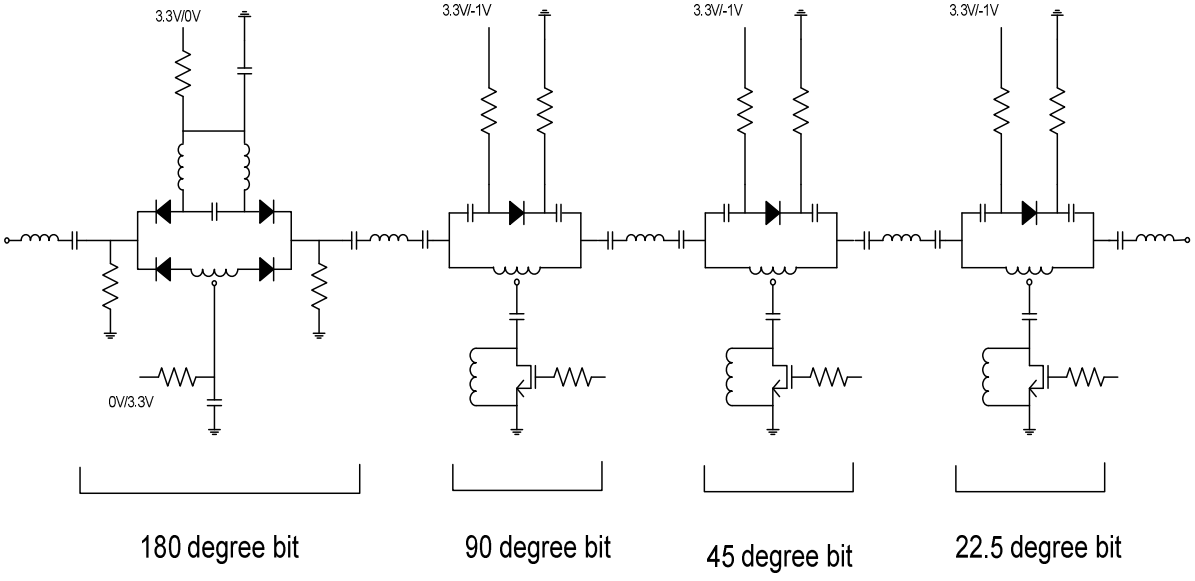
CHAPTER FIVE

HIGH LINEARITY LOW POWER PIN DIODE PHASE SHIFTER DESIGN

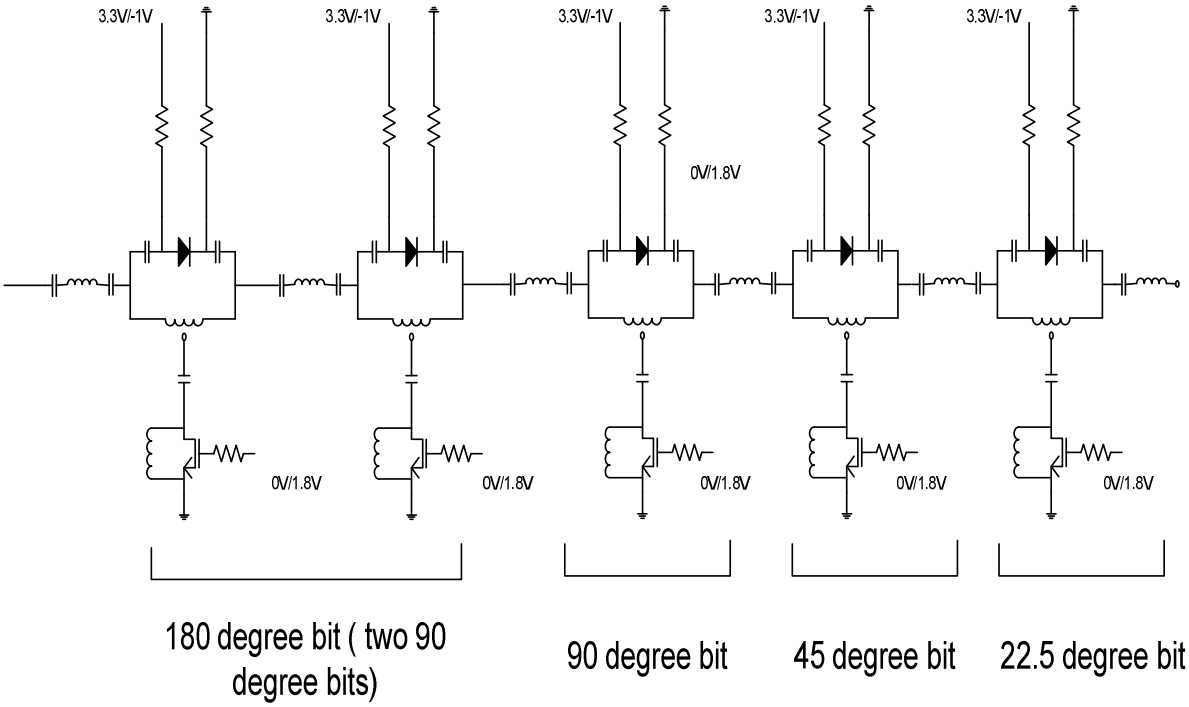
Phase shifters are widely used as beam-steering devices in phased array antenna systems to electronically control the directivity of transmit and receive paths for maximum receiver sensitivity. A conventional broadband phase shifter is made by switching between separate high-pass and low-pass filters. The switching elements are located external to the filters. Traditionally phase shifters have been implemented in GaAs IC technologies or micro-electromechanical systems (MEMS) for high-end commercial and military applications [30]-[31]. However, high cost and low integrative capability is a big disadvantage. MOSFETs can also be used as switching elements. In such a design the off-state capacitance of the FETs tends to degrade the performance and limit the bandwidth of the phase shifter. Development in Silicon Germanium (SiGe) BiCMOS technology offers microwave performance with high integration level that makes the design of low cost, compact, and high performance phase shifters possible. The low insertion loss, high isolation, high linearity PIN diode can be used to improve the phase shifter's RF performance. This technique is applied to implement the 4-bit phase shifter.

5.1 Architecture of the phase shifter

In this dissertation, a MMIC phase shifter was developed in a standard six-level metal SiGe BiCMOS process, which offers high performance transistors with peak *Ft* of 155-GHz and high quality passive components.



(a)



(b)

Fig.34 The 4-bit phase shifter architecture (a) L.wang's high power version (b) new low power version

R. Tayrani recently demonstrated a 6-bit switched filter phase shifter with PIN diode switches, but the bulky transmission-line structures make chip area considerably large [10]. For a miniature design, differential inductors are firstly proposed here to replace the transmission lines. Due to reduced parasitic resistance, insertion loss would improve with the use of differential inductors.

In 2006, L. Wang has designed a Ku-band 4-bit PIN diode phase shifter with hybrid switched filters shown in Fig.34 (a) [33]. The 180^{o} bit uses high-pass/low-pass filter. The 90^{0}, 45^{0}, and 22.5^{0} bits use bridged-T filter. Low insertion loss SiGe PIN diodes are used for switching. The 180^{0} bit employs high-pass/low-pass filter since this structure intends to achieve large phase shift over a wide frequency range. High pass π-shape filter (HPF) has the least negative phase delay, which serves as a reference path. A low pass T-shape filter (LPF) has the most negative phase delay which serves as delay path. The 90^{0}, 45^{0}, and 22.5^{0} bits use bridged-T filter since it has lower insertion loss and provides medium phase shift. The differential inductor is used instead of two single-ended transmission lines to minimize chip area. The DC blocking capacitors which have little impact on the phase delay. The die size is 1.6 mm × 0.37 mm excluding the testing pads, which is only 5% of the area of the phase shifter reported in [10].

However, in both the reference path and the delay path, the 180^{0} bit always consumes 2mA current. It leads to large power consumption when the phase shifter integrated in the large phase array with thousands of elements.

A new design which reduces the phase shifter's average power consumption is proposed (shown in Fig.34 (b)). The 4-bit phase shifter consists of 5 stages of phase shifting elements. The first two 90^{0} phase shifters are tied together to become the 180^{0} bit,

and the 90^0, 45^0, 22.5^0 bits are placed in series afterwards. Each bit is designed using a bridged-T filter. The average current consumption is only 2.5mA, a saving of 1mA.

5.2 The bridged-T phase shifter bit design

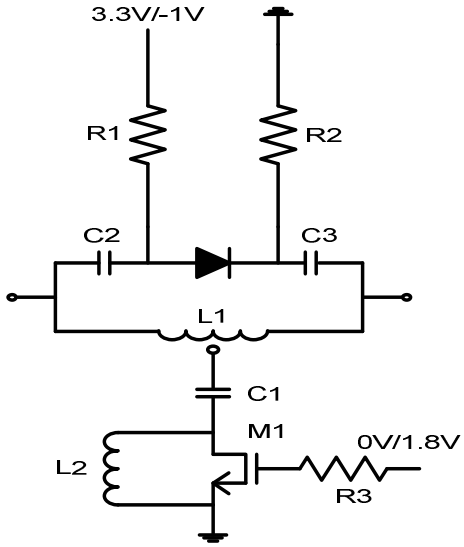


Fig. 35 The schematic of bridged-T type filter phase shifter bit

The 50 μm^2 PIN diodes are used as single-pole-single-throw (SPST) switching devices to switch between the reference path and the delay path. R_3 (2K Ω) provides a high RF impedance to reduce the signal leakage and some ESD protection for the n-MOSFET, which switches in/out the inductor L_2 between on/off states

When the PIN diode is forward biased, the reference path dominates the signal route. *L2* is chosen to resonate with the parasitic capacitance *Cp* from M1 at 15-GHz to float the LPF. When PIN diode is reverse biased, *L2* is shorted by the on-resistance of M1 and the LPF routes the signal. *L1* and *C2* are based on Eq. (30)-(31) [32]. *L5* is derived from Eq. (32):

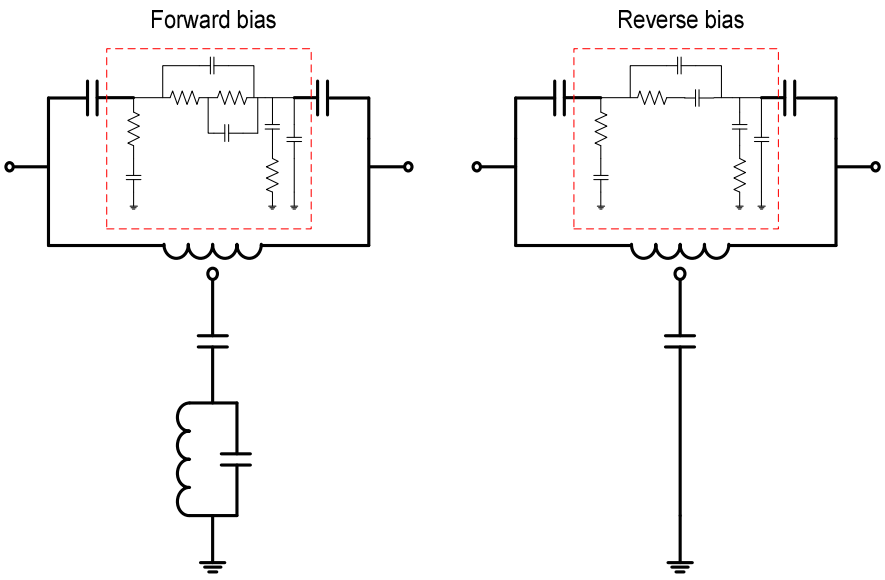


Fig. 36 Simplified equivalent circuit diagrams for the bridged-T type phase bit when the PIN diode is (a) on (b) off [33]

$$\frac{L_1}{2} = Z_0 \frac{1-\cos(\phi)}{\omega \sin(\phi)} \tag{30}$$

$$C_2 = \frac{\sin(\phi)}{\omega Z_0} \tag{31}$$

$$L_5 = \frac{1}{\omega^2 C_p} \tag{32}$$

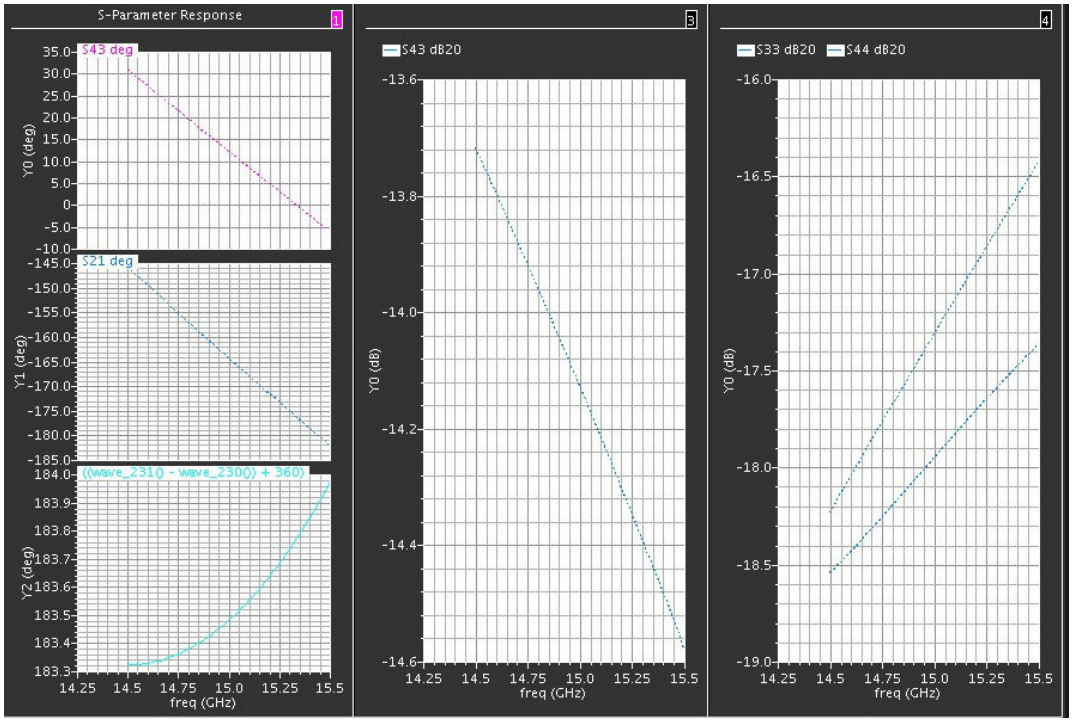
5.3 The 4-bit phase shifter performance

The simulation results are shown in Fig. 37. For a 14.5 GHz to 15.5GHz operating range, the delta phase delay of 180^0 bit is 0.7^0 (183.3^0 ~184^0), the delta insertion loss is 0.85 dB (13.72 dB-14.57 dB); the delta phase delay of 90^0 bit is 0.06^0 (92.33^0 -92.39^0), the delta insertion loss is 0.09 dB (10.63 dB -10.72 dB); the delta phase delay of 45^0 bit is 0.37^0 (47.15^0 ~47.52^0), the delta insertion loss is 0.22 dB (9.99 dB-

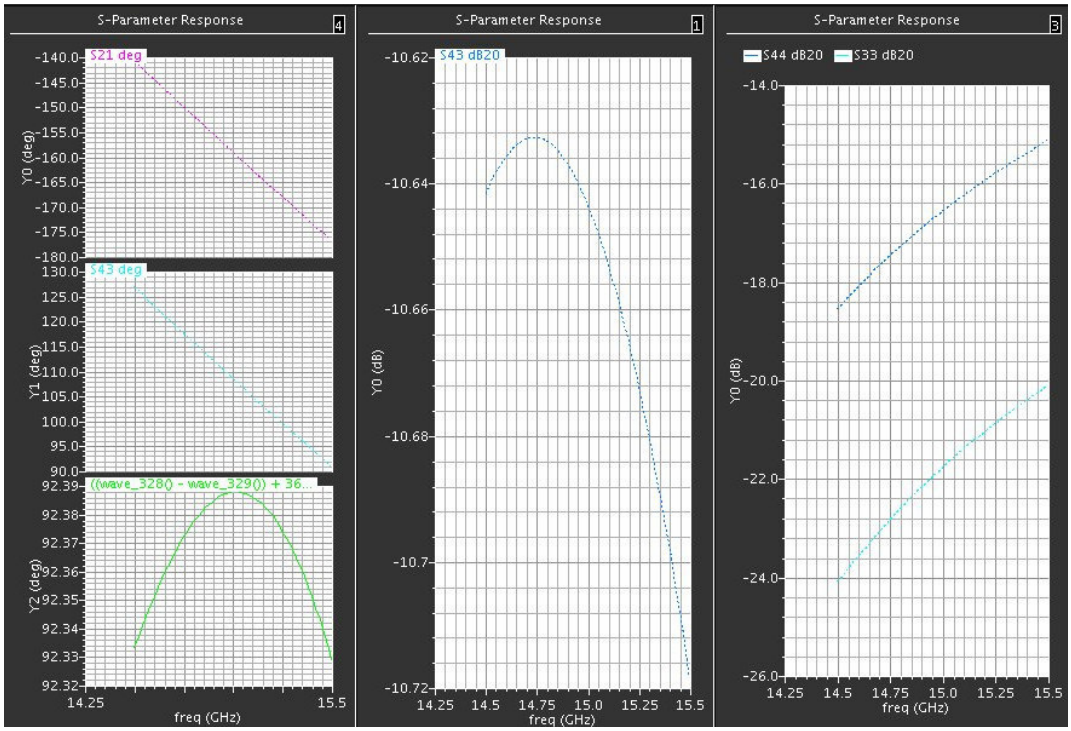
10.21dB); the delta phase delay of the 22.5^0 bit is 0.4^0 (23.6^0-24^0), the delta insertion loss is 0.31 dB (9.97 dB-10.28 dB). All of the 4 bit's input and output return loss is better than 15 dB. Table IV summarize the phase shifter's performance.

TABLE IV
PERFORMANCE OF 4-BIT PHASE SHIFTER

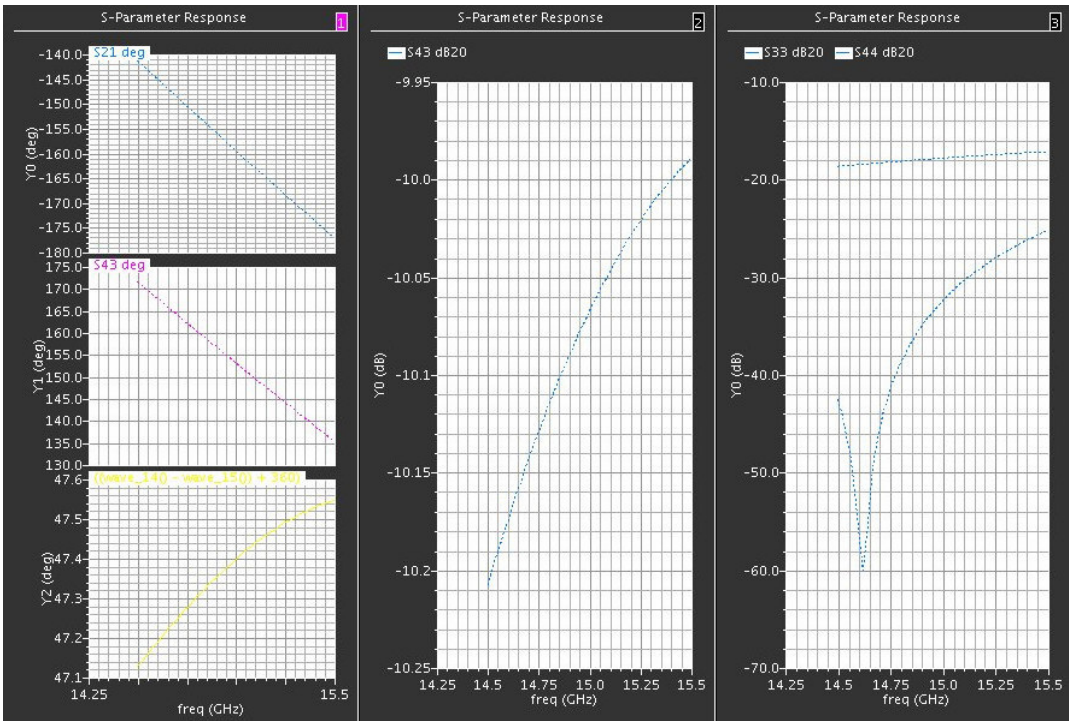
Control Voltage	3.3V for Pin Diode; 1.8V for MOSFET
Current Consumption	0 mA to 5 mA (Average current 2.5mA)
Delta Phase Delay	3.54^0 from 14.5 GHz to 15.5 GHz
Delta Insertion Loss	< 1 dB for single phase bit over the freq. range
Insertion Loss	(16.68 dB, 18.04 dB)
Return Loss	(Input 15.2~14.3dB, 19.5~21.5dB)
4 Bit Phase Delay	180^o, 90^o, 45^o, and 22.5^o


S-Parameter Response
S43 deg
S21 deg
((wave_231() - wave_230()) + 360)
Y0 (deg)
Y1 (deg)
Y2 (deg)
freq (GHz)
S43 dB20
Y0 (dB)
S33 dB20
S44 dB20

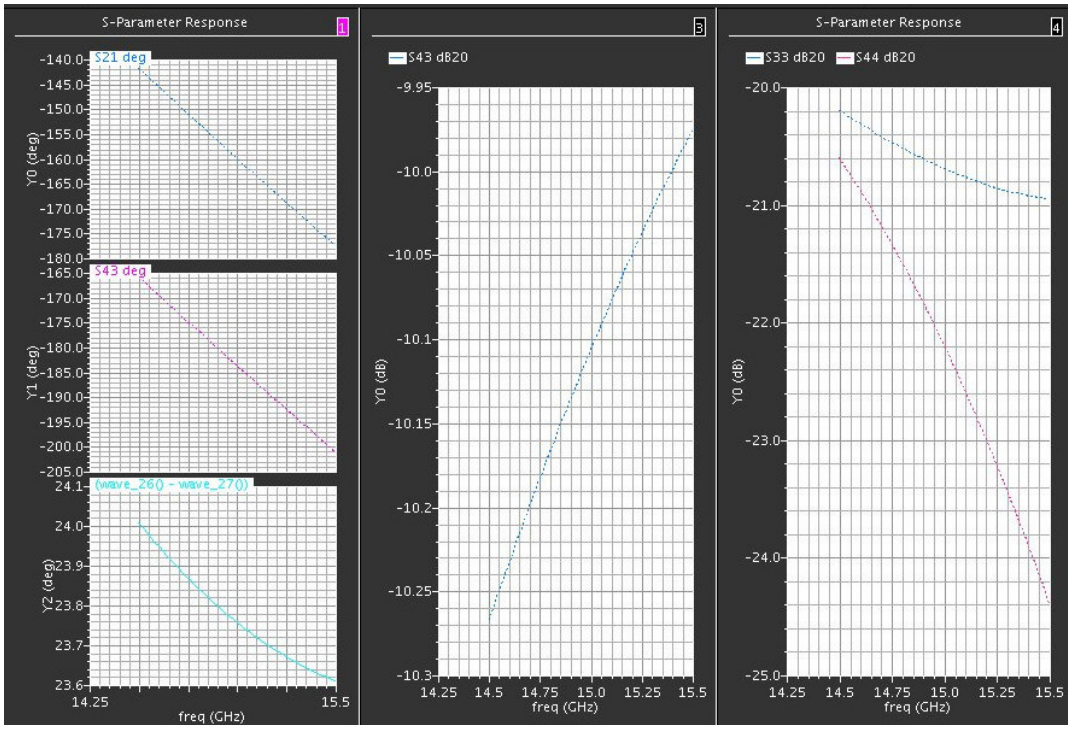
(a)


S-Parameter Response
S21 deg
S43 deg
((wave_328() - wave_329()) + 36..
Y0 (deg)
Y1 (deg)
Y2 (deg)
freq (GHz)
S43 dB20
Y0 (dB)
S44 dB20
S33 dB20

(b)



(c)



(d)

Fig.37 The phase delay, insertion loss and return loss of (a) 180^0 bit, (b) 90^0 bit, (c) 45^0 bit (d) 22.5^0 bit

5.4 The active power combiner

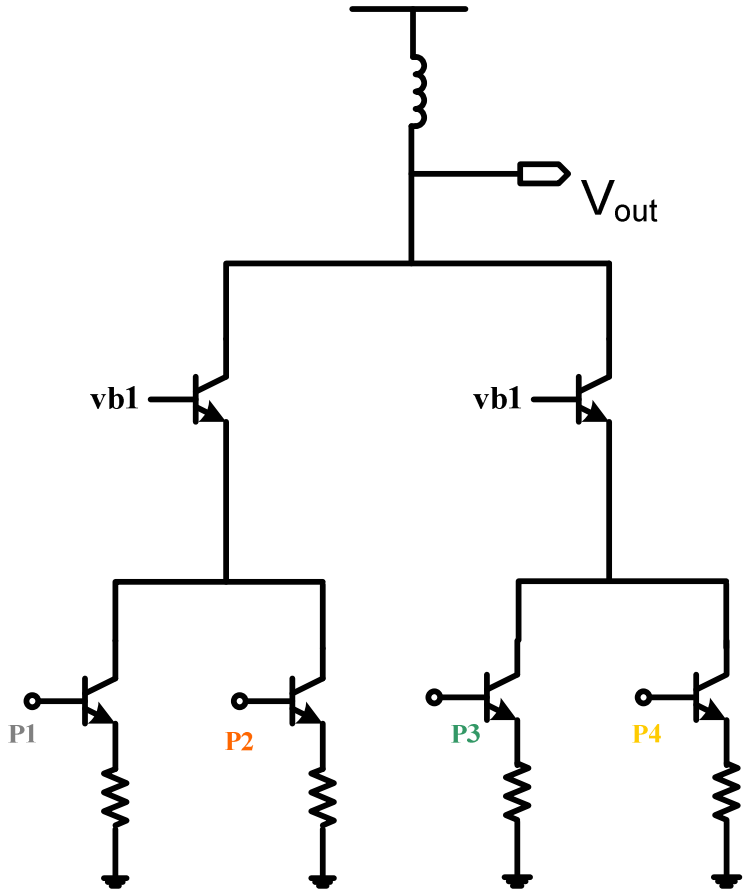


Fig.38 The schematic of 4:1 power combiner

The power combiner uses the gain cell with *N* input paths to deliver received signals from an *N*-antenna array to a single output path. The 4-path 15-GHz signals were combined through an active combining amplifier, as shown in Figure 38. The amplifier with resistive degeneration converts the 15-GHz signal from voltage domain to current domain. The cascode transistor is inserted at each combining junction, isolating the input ports and output ports. The output of the amplifier is loaded with an inductor. Single-ended instead of the differential structures [16]-[17] are used in this design, because the input from the phase shifters are single-ended and the signal-ended structure dissipates

half amount of power compared with the differential structure. Compared to the passive combining structure, the active signal combining technique can compensate the transmission line loss and provide good isolation between the input and output by using the cascode transistor. BJTs are preferred over MOSFETs for more current driving capability.

TABLE V
PERFORMANCE OF 4:1 POWER COMBINER

Topologies	4:1 power combiner
Supply Voltage	3.3 V
Frequency	14.5GHz-15.5 GHz
DC current	2 mA
Voltage gain	2.7 dB
Linearity	Input P1dB around – 6.6dBm
Process	0.18um SiGe BiCMOS

CHAPTER SIX

CONCLUSION

The low cost and reconfigurable phased array communication systems have received remarkable attention with the explosive growth in satellite and mobile communication markets. For the T/R module in phased array applications, high performance switching circuits and phase shifting circuits are critical components to successful system integration.

In this dissertation, new techniques in designing low insertion loss, high isolation and highly linear switching components and highly linear phase shifting components have been discussed.

Low insertion loss and highly linear PIN RF SPST switches are presented with an analysis of geometry effects. Theoretical analysis supported by the measurement results show that a PIN diode with a reduced anode-to-cathode distance, smaller *P/A* ratio and positively biased cathode improves both the insertion loss and the power handling capability of the RF switch. The 50 μm^2 PIN RF switch can achieve 0.65 dB insertion loss, which is the best value reported for a standard 0.18-μm SiGe PIN SPST switch with the same anode size. The measured P_{1dB} of 16 dBm is well suited for phased array communication systems.

New high performance SPDT architecture has been presented. The new architecture can alleviate the leakage caused by the *Psub-Nwell* parasitic diodes. The measurement results show that the SPDT switch can achieve a through-path loss of 1.2 to 1.8 dB and an isolation path loss of 51 to 36 dB over a wide frequency range (2 to 18 GHz). The retune loss of switches is less than 14 dB between 2 and 18 GHz.

The design of a low power high linearity Ku-band 4-bit PIN diode phase shifter is presented. The bridged-type filter is used for the180^0, 90^0, 45^0 and 22.5^0 bit design. By employing differential inductors and hybrid switched filters, this phase shifter achieves compact chip area, flat phase response, low delta insertion loss and high return loss over a wide frequency range. Compared with the previous design [33], the new phase shifter design reduces the average current consumption from 3.5mA to 2.5 mA, which is significant for phase array with thousands of elements. The active power combining technique is used to combine the phase shifter into a phase shifter array.

Integration of the developed PIN RF SPST, SPDT and phase shifter with other RF components is an attractive solution for achieving highly integrated low cost SoC T/R modules in satellite communication applications.

BIBLIOGRAPHY

[1] P.Sun, D.Heo, S. Fong, "Radiation-Tolerant SiGe BiCMOS Smart MMICs for Space Communications," AFRL Proposal, July 2004

[2] D. Hoag, J. Brogle, T. Boles, D. Curcio and D. Russell, "Heterojunction PIN diode switch," in *IEEE MTT-S Int. Microwave Symp. Dig.,* Long Beach, CA, pp. 255-258, 2003. Xiang Guan

[3] J. A. Torres and J. C. Freire, "Monolithic transistors SPST switch for L-band," *IEEE Trans. Microwave Theory Tech*., vol. 50, no.1, pp. 51-56, Jan. 2002.

[4] Z. Li and K. K. O, "15-GHz Fully Integrated NMOS switches in 0.13-µm CMOS process," *IEEE J. Solid-State Circuits*, vol.40, no. 11, pp. 2323-2328, Nov. 2005.

[5] Y. Jin and C. Nguyen, " Ultra-compact high-Linearity high- power fully integrated DC-20 GHz 0.18-µm CMOS T/R switch," *IEEE Trans. Microwave Theory and Tech.,* vol.55, no.1, pp.30- 36, Jan. 2007.

[6] Q.Li, Y.P.Zhang, S.Y. Kiat, W. M. Lim, "16.6- and 28-GHz Fully Integrated CMOS RF Switches With Improved Body Floating", *IEEE Trans. Microwave Theory and Tech.,* vol.56, no.2, pp.339-345, Feb. 2008.

[7] J. D. Cressler, "SiGe HBT reliability issues associated with operation in extreme environments," in *Proc. 6th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems,* San Diego, CA, Jan. 2006, pp.3-7.

[8] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Norwood, MA: Artech House, 2003.

[9] J. P. Comeau, A. K. Sutton, B. M. Haugerud, J. D. Cressler, W.L. Kuo, P. W. Marshall, R. A. Reed, A. Karroy, R. V. Art, "Proton tolerance of advanced SiGe HBTs fabricated on different substrate materials," *IEEE Trans. Nucl. Sci.,* vol.51, no. 6, pp. 3743-3747, Dec. 2004.

[10]R. Tayrani, M. A. Teshiba, G. M. Sakamoto, Q. Chaudhry, R. Alidio, Y. Kang, I. S. Ahmad, T. C. Cisco, M. Hauhe "Broad-Band SiGe MMICs for phased- array radar applications," *IEEE J. Solid-state Circuits*, vol. 38, no. 9, pp.1462 -1471, Sept. 2003.

[11] P. Sun, P. Upadhyaya, L. Wang, D. Jeong and D. Heo , " High performance PIN diode in 0.18-um SiGe BiCMOS process for broadband monolithic control circuits," in *Proc. 1th European Microwave Integrated Circuits Conf.*, Manchester, UK, Sept. 2006, pp.148-152.

[12] P. Sun, L. Wang, P. Upadhyaya, and D. Heo, " High Isolation 10GHz to 20 GHz SPDT Switch Design Using Novel Octagonal PIN diode structure," in *Proc. IEEE Workshop on Microelectronics and Electron Devices*, Apr. 2005, pp. 38-41.

[13] P. Sun, P. Upadhyaya, D. Jeong, D. Heo and G. S. La Rue, " A novel SiGe PIN diode SPST switch for broadband T/R module," *Microwave Wireless Compon. Lett*., vol. 17, no.5, pp.352-354, May 2006.

[14] B.A. Orner, Q. Liu, J. Johnson, R. Rassel, X. Liu, D. Sheridan, A. Joseph and B. Gaucher, "P-i-n diodes for monolithic millimeter wave BiCMOS applications," in *Proc. 3 rd Int. SiGe Technology and Devices*, Princeton, NJ, May 2006, pp.1-2.

[15] Cameron T. C., "A Calibrated Phase and Amplitude Control System for Phased-Array Transmitters," Ph.D. Thesis, University of Washington, 2006

[16] X.Guan, "Microwave integrated phase array receivers in silicon", Ph.D. Thesis, Caltech, 2005

[17] K. Koh, G. M. Rebeiz, "An X- and Ku-Band 8-Element Phased-Array Receiver in 0.18-um SiGe BiCMOS Technology," *IEEE J. Solid-state Circuits*, vol. 43, no. 6, pp.1360 -1371, June. 2008

[18] B. Razavi, *RF Microelectronics*, Upper Saddle River, NJ, Prentice-Hall, Inc, 1997

[19] Reinhold Ludwig, *RF Circuit Design-Theory and Applications,* Upper Saddle River, NJ, Prentice-Hall, Inc, 2000

[20] Microsemi, "The PIN diode circuit designers' handbook"

[21] R.H. Caverly, G. Hiller, "Distortion in Microwave and RF Switches by Reverse Biased PIN diodes," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June. 1989, vol. 3, pp. 1073–1076

[22] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw Hill, 2001.

[23] R. Curby and L. Nevin, " Low resistance, low bias current PIN diodes," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers,* Philadelphia, PA, Feb. 1976, pp. 118-119.

[24] T. Kimoto, N. Miyamoto and H. Matsunami, "Performance Limiting Surface Defects in SiC Epitaxial p-n Junction Diodes," IEEE Trans. Electron Devices, vol.46, no. 3, pp. 471-477, Mar. 1999.

[25] R. H. Caverly and G. Hiller, " Distortion in p-i-n Diode Control Circuits," *IEEE Trans. Microwave Theory Tech*., vol. 35, no.5, pp. 492-501, May 1987.

[26] F. Hirose, K. Kurita, Y. Takahashi, and M. Mukaida, " Operation Mechanism on SiGe/Si/Si PIN Diodes Explained using Numerical Simulation," *Electrochemical and Solid State Lett.*, 8(7), G160-G163, 2005.

[27] E. P. Vandemme, D. M.M.-P. Schreurs and C.V. Dinther, " Improved Three-step De-Embedding Methods to Accurately Account for the Influence of Pad Parasitics in Silicon On-Wafer RF Test-Structures," *IEEE Trans. Electron Devices,* vol.48, no. 4, pp. 737-742, Mar. 1999.

[28] J.D. Cressler, M.C. Hamilton, G.S. Mullinax, Y. Li, G. Niu, C.J. Marshall, P.W. Marshall, H.S. Kim, M.J. Palmer, A.J. Joseph, G. Freeman, "The effect of Proton irradiation on the lateral and vertical scaling of UHV/CVD SiGe HBT BiCMOS," *IEEE Trans. Nuclear Science*, vol. 47, no. 6, pp.2515-2530, Dec 2000.

[29] P.W. Marshall, M.A. Carts, A. Campbell, D. McMorrow, S. Buchner, R. Stewart, B. Randall, B. Gilbert, R.A. Reed, R.A, "Single Event Effects in circuit-hardened SiGe HBT logic at gigabit per second data rates," *IEEE Trans. Nuclear Science*, vol. 47, no. 6, pp. 2515-2530, Dec. 2000.

[30] C. F. Campbell and S. A. Brown, "A compact 5-bit phase-shifter MMIC for K-band satellite communication systems," IEEE Trans. Microwave Theory Tech., vol. 48, no. 12, pp. 2652-2656, Dec. 2000.

[31] N. S. Barker and G. M. Rebeiz, "Optimization of distributed MEMES transmission-line phase shifters U-band and W-band designs," *IEEE Trans. Microwave Theory Tech.*, vol. 48, no. 11, pp. 1957-1966, Nov. 2000.

[32] D. W. Kang, H. D. Lee, C. H. Kim, and S. Hong, "Ku-Band MMIC Phase Shifter Using a Parallel Resonator With 0.18-µm CMOS Technology," *IEEE Trans. Microwave Theory and Tech.*, vol. 54, no. 1, Jan. 2006

[33] L.Wang, P.Sun, R. Bonebright, D. Heo, "A Ku-band 4-bit PIN Diode Phase Shifter with Hybrid Switched Filters," submitted to *Microwave Wireless Compon. Lett.*