PHASE NOISE SUPPRESSION TECHNIQUES FOR 5-6GHZ OSCILLATOR DESIGN

By

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A thesis submitted in partial fulfillment of
the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

WASHINGTON STATE UNIVERSITY
School of Electrical Engineering and Computer Science

DECEMBER 2007

To the Faculty of Washington State University:

The members of the Committee appointed to examine the thesis of YANG ZHANG find it satisfactory and recommend that it be accepted.

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Chair

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ACKNOWLEDGMENT

I would like to express my gratitude to all those who gave me the opportunity to complete this thesis. Special thanks are due to my advisor, Dr. Deuk Heo, for his expert guidance and constant support. I would also like to thank my thesis committee members, Dr. George Larue and Dr. John Ringo for their insightful comments and valuable suggestions. My gratitude is also given to the National Science Foundation Center for Analog and Digital Integrated Circuits (CDADIC) for funding the projects related with my thesis work, to Jazz Semiconductor Corp. and National Chip Implementation Center in Taiwan for generously providing the fabrication of my test circuits, and to the interface group of National Seminconductor Corp. in Federal Way, WA for providing me the test environment and valuable suggestions.

I am also very grateful to my ARMAG (Advanced RF and Mixed-Signal Application Group) team members at WSU, Parag Upadhyaya, Le Wang, Pinping Sun, Peng Liu, Lanchuan Zhou and Jaeyoung Jung for their constant support technically and non-technically. I also appreciate the helpful discussions and friendship offered by Dirk Robinson, Wei Zheng, Prasanna Upadhyaya and other students in the ETRL lab.

Finally I would like to thank to my family for their deeply love, endless trust and support.

PHASE NOISE SUPPRESSION TECHNIQUES FOR 5-6GHZ OSCILLATOR DESIGN

ABSTRACT

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This thesis presents novel designs of low-phase-noise 0.18μm CMOS LC voltage controlled oscillator (VCO) and quadrature VCO (QVCO) for 5-6GHz wireless communications applications. Using a new capacitor tapping technique, the phase noise of CMOS LC oscillators is lowered based on the improvement of loaded-Q improvement and suppression of flicker noise up-conversion. As a proof of concept, a 4.6GHz LC VCO using this technique is implemented and shows measured phase noise of -120dBc/Hz at 1MHz offset while drawing 7mA from a 1.8V supply. Bottom-series coupling is a low-phase-noise coupling method for QVCOs reported by other researchers recently. In this thesis, new analysis of bottom-series coupling is proposed and proves its phase noise advantage. A 5.3GHz LC QVCO using bottom-series coupling and capacitor tapping is implemented. The measured phase noise is -123dBc/Hz at 1MHz offset while drawing 10mA from a 1.8V supply and is -118dBc/Hz at 1MHz offset while drawing 10mA from a 1V supply. Bulk coupling is another coupling method reported for low-phase-noise QVCO design. Combining bulk coupling and capacitor tapping techniques, a 5.6GHz LC QVCO is implemented and shows measured phase noise of -118dBc/Hz at 1MHz offset while drawing

10mA from a 1.8V supply. Overall, all the proposed VCO and QVCOs show good measurement performance and meet the design expectation.

This work also gives an overview of the operating principles and phase noise mechanism of CMOS LC VCOs and QVCOs. The important role of high-performance signal generation circuits for 5-6GHz wireless communications is also addressed.

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2. Yang Zhang, Peng Liu, Tang-Nian Luo, Yi-Jan Emery Chen, Deukhyoun Heo, “A Low-Phase-Noise LC QVCO with Bottom-Series Coupling and Capacitor Tapping,” submitted to *IEEE International Symposium on Circuits and Systems’08* in October 2007.

3. Yang Zhang, Peng Liu, Tang-Nian Luo, Yi-Jan Emery Chen, Deukhyoun Heo， “Low-Phase-Noise *LC* Quadrature VCO Design Based on Analysis of Resonator Phase Shift,” will be submitted to *IEEE Microwave and Wireless Component Letters*.

4. Le Wang, Parag Upadhyaya, Pinping Sun, Yang Zhang, Deukhyoun Heo, Yi-Jan Emery Chen, DongHo Jeong, "A 5.3 GHz Low-Phase-Noise LC VCO With Harmonic Filtering Resistor," in *Proc. IEEE International Symposium on Circuits and Systems*, May 2006.

5. Upadhyaya, P., Rajashekharaiah, M., Yang Zhang, Deukhyoun Heo, Yi-Jan Emery Chen, “A 5 GHz novel 0.18-µm inductor-less CMOS sub-harmonic mixer,” In *Proc. IPSN 2005*, pp. 71-74, April 2005.

6. Upadhyaya, P., Rajashekharaiah, M., Yang Zhang, Deukhyoun Heo, Yi-Jan Emery Chen, “A 5 GHz novel 0.18-µm inductor-less CMOS sub-harmonic mixer,” in *Proc. WMED*, pp. 71-74, April 15, 2005.

DEDICATION

TO MY FAMILY

CHAPTER 1 INTRODUCTION

1.1. Background and Motivation

Wireless communications is the fastest growing segment of the communications industry. Cellular systems have experienced exponential growth over the last decade and have become a critical business tool and part of everyday life worldwide. In addition, wireless local area networks currently supplement or replace wired networks in many homes, business, and campuses. Many new applications, including wireless sensor networks, smart home and appliances are emerging from research ideas to concrete systems [1].

There is increased interest in 5-6GHz frequency band wireless communication systems other than the traditional 2.4GHz applications. The 5-6GHz band has much greater available spectrum. In this band there are 12 non-overlapping channels, each with 20MHz of bandwidth. This means significantly better performance as compared to the 2.4GHz band. The entire 2.4GHz band is 80MHz wide, which only allows three non-overlapping channels. 2.4GHz WLANs can also experience interference from cordless phones, microwaves, and other applications in this band while 5-6GHz system is relatively free from interfering sources. Seen from Figure 1-1,

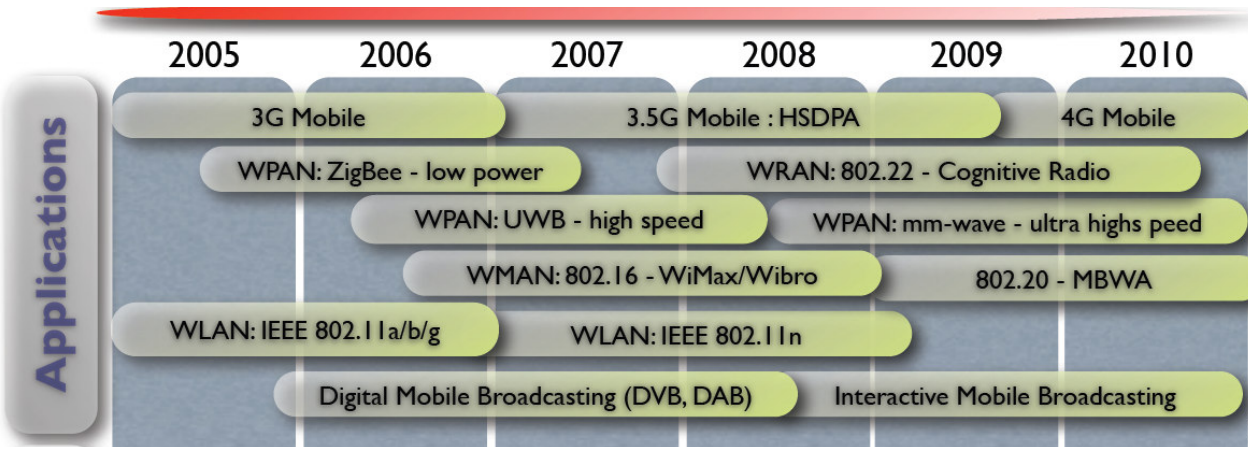


Figure 1-1. Roadmap for the wireless communication applications.

Wireless Metropolitan Area Networks (WMAN) 802.16 and Wireless Local Area Networks (WLAN) 802.11n are the recent emerging wireless communications technologies and they both have application in the 5GHz frequency band. The widely used WLAN 802.11a technology is also at 5GHz.

Transceivers are the main component of a wireless communication system. Figure 1-2 shows the simplified block diagram of a transceiver which includes a receiver path and a transmitter path. A major challenge in the design of transceiver is the design of the local

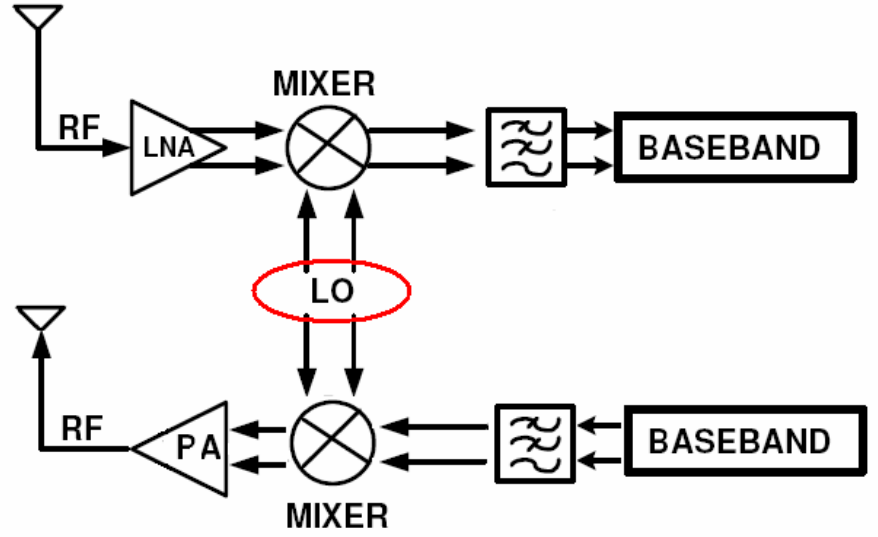


Figure 1-2. Simplified block diagram for a transceiver.

oscillator (LO) carrier signal. The phase noise of the LO is one of the most critical parameters for the quality and reliability of the information transfer. Phase noise is a measure of signal spread. For multi-channel applications, if the signal spreads from one channel to adjacent channels, it would increase the noise level and thus reduce the signal to noise ratio (SNR) of that particular channel as well as limiting data bandwidth. Usually the LO has the frequency tuning capability through a DC control voltage and becomes a voltage controlled oscillator (VCO). The LO shown

in Figure 1-2 is differential and quadrature LO signals may also be required in some transceiver structures, like direct-conversion transceiver (DCT) as shown in Figure 1-3 [2]. For the quadrature LO, phase accuracy is another important specification besides phase noise. A quadrature LO with frequency tuning capability is called a quadrature voltage controlled oscillator (QVCO).

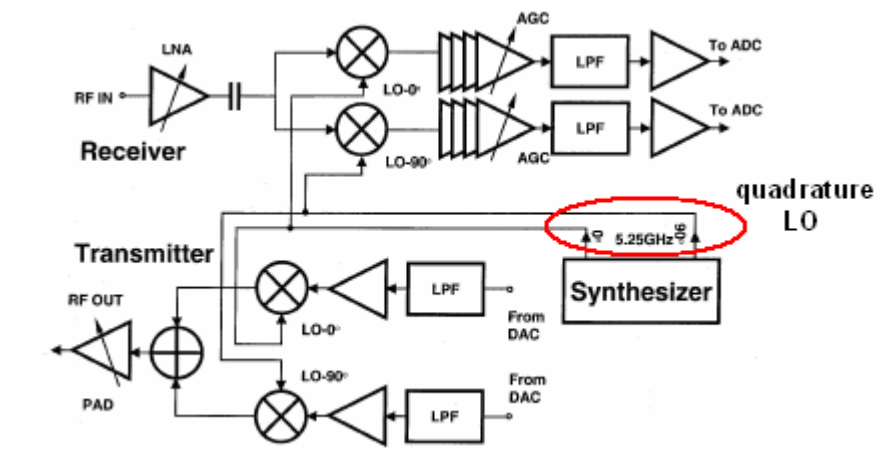


Figure 1-3. Block diagram for a direct-conversion transceiver.

1.2. Thesis Objective

As mentioned in the previous section, VCO and QVCO are two important circuit components in a transceiver system and their phase noise is one of most critical parameters for the quality of the system. A lot of research has been done for improving the phase noise of VCOs and QVCOs, however, the challenge is still existent especially when the supply voltage goes down with the technology node scaling and low power consumption is demanded for portable applications. Therefore, the target of this thesis is to provide new techniques and design perspectives for low-phase-noise VCO and QVCO design at low-voltage and low-power applications.

1.3. Thesis Organization

This thesis is organized into 7 chapters. Chapter 2 will discuss the principle of oscillation and specifications of VCOs and QVCOs. Chapter 3 will discuss the phase noise mechanism of LC oscillators which serves as the base for the low-phase noise oscillator designs in this work. Chapter 4 to 6 will present three original low phase noise 5-6GHz VCO and QVCO designs, which are the core of this thesis. In Chapter 4, a new capacitor tapping technique will be proposed to improve the loaded-Q of the resonator and the phase noise of the VCO. A 4.6GHz LC VCO using this technique has been implemented and proves the concept. In Chapter 5, a novel analytical framework will be presented for the bottom-series coupling method for LC QVCOs and show that this coupling method adds zero phase shift to the resonator and leads to low phase noise. Combining bottom-series coupling and capacitor tapping technique, a 5.3GHz LC QVCO was then implemented to achieve ultra low phase noise performance. In Chapter 6, bulk coupling method for QVCO will be discussed and used with the capacitor tapping technique to design a low-phase-noise 5.6GHz LC VCO. All the three designs show good measured performance and prove the low-phase-noise design concepts. Finally, final thoughts and conclusions are summarized in Chapter 7.

CHAPTER 2 GENERAL THEORY OF VCOS AND QUADRATURE VCOS

2.1. General theory of VCOs

2.1.1. Principle of Oscillation of Feedback Oscillators

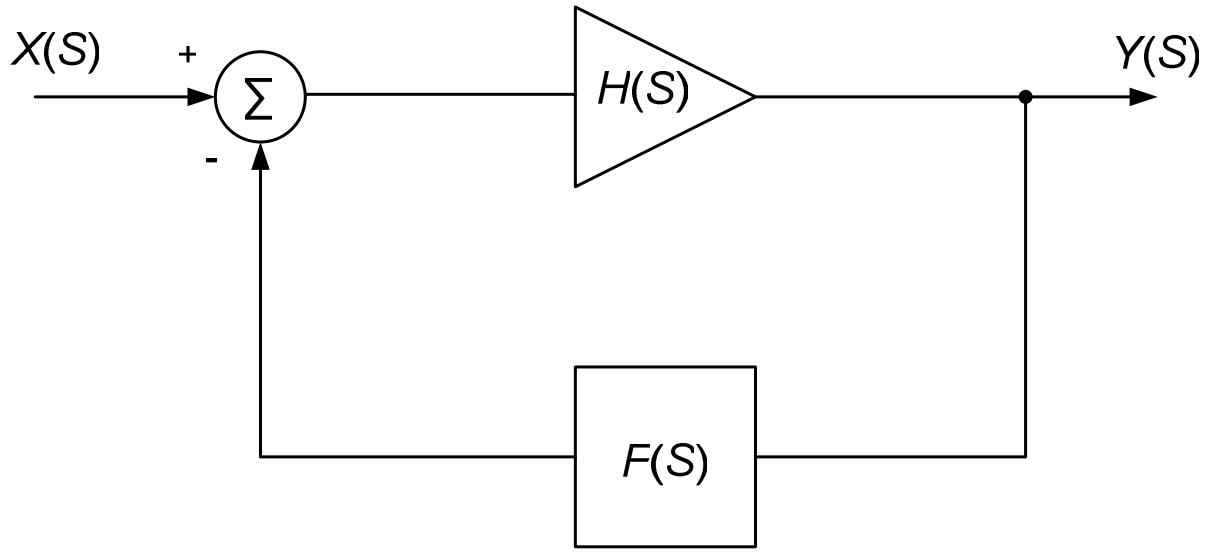


Figure 2-1. Block diagram for the oscillation principle of a feedback oscillator.

An oscillator generates a periodic output. As such, the circuit must entail a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal [3]. Most RF oscillators can be viewed as feedback circuits. Consider the simple linear feedback system depicted in Figure 2-1, with the overall transfer function

$$\frac{Y(S)}{X(S)} = \frac{H(S)}{1 + H(S)F(S)}. \tag{2-1}$$

A self-sustaining mechanism arises at the frequency S_0 if $H(S_0)F(S_0)$ =-1 which means the oscillator is actually a positive feedback system and the loop gain, $L(S)$, can be defined as

$$L(S) = -H(S)F(S). \tag{2-2}$$

To maintain the oscillation amplitude constant, S_0 must be purely imaginary, i.e., $S_0=j\omega_0$. Thus, for steady oscillation, two conditions must be simultaneously met at ω_0. Firstly, the loop gain must be unity

$$\left|H(j\omega_0)F(j\omega_0)\right|=1 \tag{2-3}$$

and secondly, the total phase shift around the loop must be 180°

$$\angle\{H(j\omega_0)F(j\omega_0)\}=180^\circ. \tag{2-4}$$

The above can be summarized as follows: If in a negative-feedback system, the open-loop gain has a total phase shift of 180° at some frequency ω_0, the system will oscillate at that frequency provided that the open-loop gain is unity. If the gain is less than unity at the frequency where the phase shift is 180°, the system will be stable, whereas if the gain is greater than unity, the system will be unstable. The conditions for stability are also known as Barkhausen's criteria.

2.1.2. LC-Resonator Oscillators

In most RF oscillators, a frequency-selective network, e.g., an LC tank, is included in the

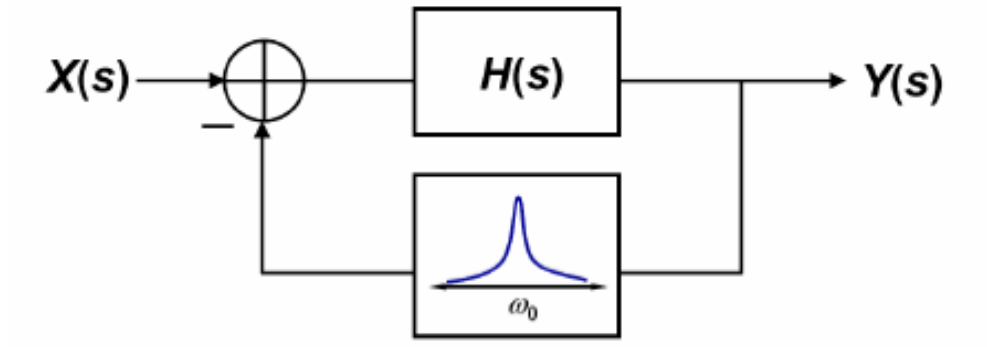


Figure 2-2. Block diagram for a feedback oscillator with a frequency-selective network.

loop so as to stabilize the frequency. This is illustrated conceptually in Figure 2-2. The frequency-selective network is also called a "resonator" which ensures that loop gain is sufficient for only a small range of frequencies.

Figure 2-3 shows the topology of a typical LC cross-coupled oscillator. The resonator is

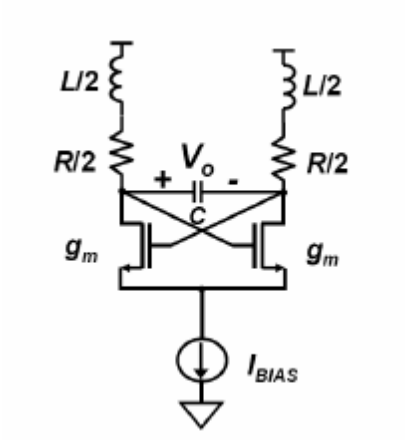


Figure 2-3. Schematic of a typical LC cross-coupled oscillator.

formed by connecting the inductor L and capacitor C in parallel, and R is the series resistance of L. To sustain steady oscillation, the positive resistance R has to be cancelled by a negative resistance as shown in Figure 2-4 conceptually. In the LC cross-coupled oscillator, the negative resistance

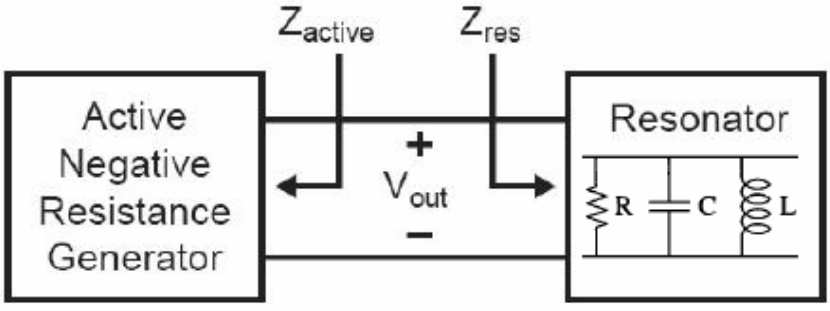


Figure 2-4. Concept of resistance cancellation for steady oscillation.

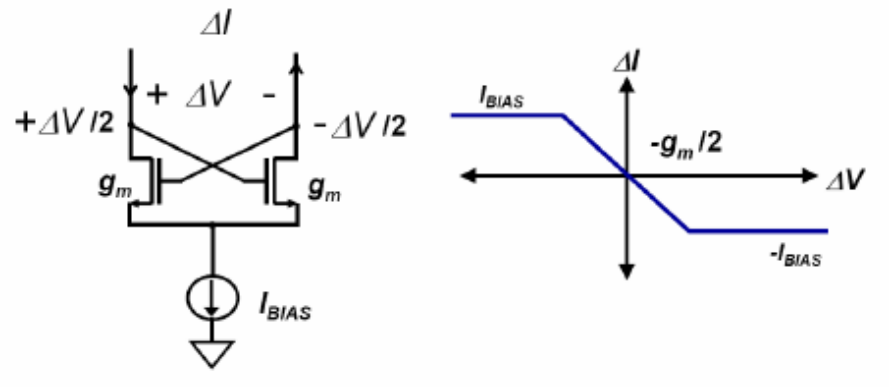


Figure 2-5. Calculation of the equivalent negative resistance of a cross-coupled pair.

cell is realized by a cross-coupled transistor pair. As illustrated in Figure 2-5, in differential mode, the drain voltages of the two switching FETs are $+\Delta V/2$ and $-\Delta V/2$ respectively. The FET with a positive drain voltage is turned off, and the other FET is turned on in which the current can be expressed as $g_m \cdot (\Delta V/2)$ flowing into the drain. Thus, the equivalent resistance looking into the drains of the cross-coupled pair can be written as

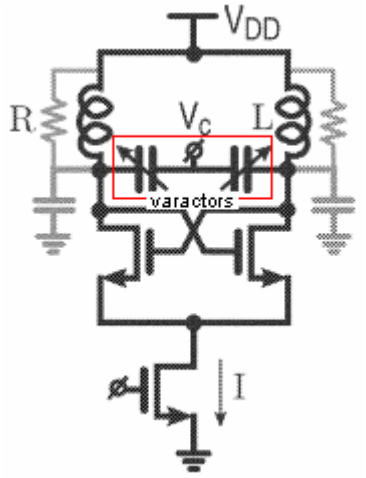
$$R_{active} = \frac{\Delta V}{\Delta I} = \frac{\Delta V}{-g_m(\Delta V/2)} = -\frac{2}{g_m} \tag{2-5}$$

which has a negative value. This negative resistance cancels the positive resistance of the resonator and sustains oscillation.

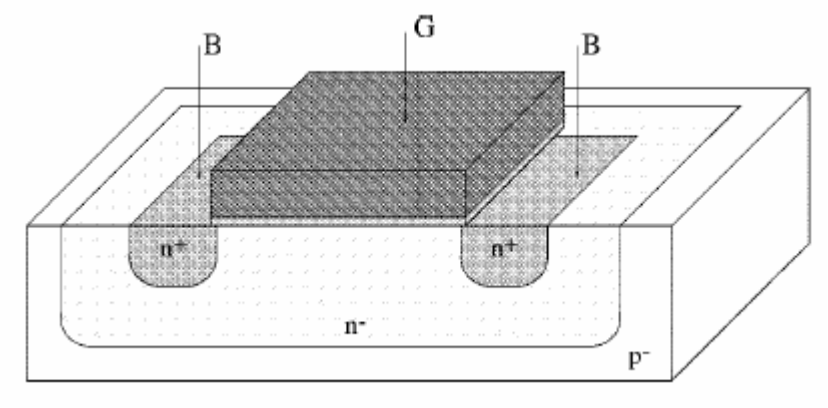
2.1.3. Performance Parameters of LC VCOs

A voltage-controlled oscillator (VCO) is a type of LC oscillator of which the oscillation frequency can be tuned by a control voltage. The frequency tuning device is usually a variable capacitor, called a varactor. The capacitance of a varactor is varied by changing the voltage across it. Figure 2-6(a) shows a cross-coupled LC VCO with a pair of accumulation-mode MOS (A-MOS) varactors. V_c is the control voltage applied at the Bulk (B) terminal as shown in Figure

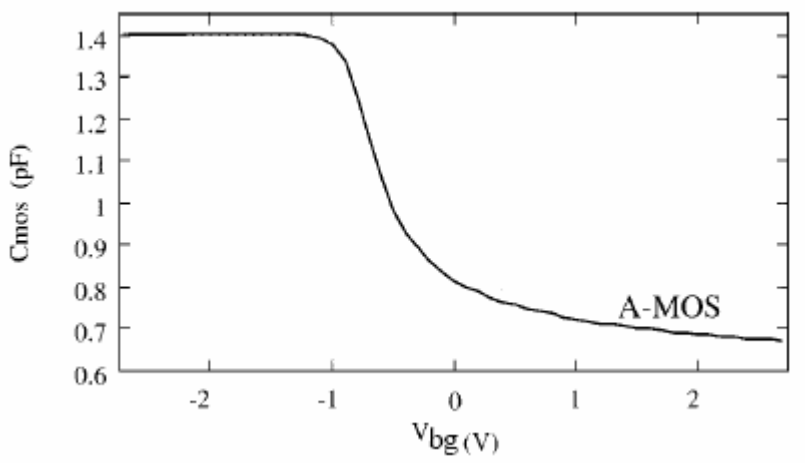
2-6(b) [4]. The A-MOS varactor is accomplished with the removal of the D–S diffusions (p-doped) from the PMOS device. At the same time, we can implement the bulk contacts (n^+) in the place left by D–S, as shown in Figure 2-6(b), which minimizes the parasitic n-well resistance of the device. The tuning characteristic of the A-MOS varactor is shown in Figure 2-6(c).



(a)



(b)



(c)

Figure 2-6. (a) Schematic of a cross-coupled VCO with varactors. (b) Implementation of A-MOS varactor. (c) Tuning characteristic of the A-MOS varactor.

The important and relevant parameters for a VCO [5] are now discussed.

Frequency Range —— The output frequency of a VCO can vary over a wide range by controlling the frequency tuning components. The frequency range is determined by the architecture of the oscillator. A standard VCO has a frequency range typically less than 30%.

Tuning Linearity —— For stable synthesizers, a linear deviation of frequency versus tuning voltage is desirable. It is also important to make sure that there are no breaks in tuning range, for example, that the oscillator does not stop operating with a tuning voltage of 0V.

Tuning Sensitivity —— This term, typically expressed in megahertz per volt (MHz/V), characterizes how much the frequency of a VCO changes per unit of tuning voltage change.

Phase Noise —— Oscillators do not generate perfect signals. The various noise sources in and outside of the transistor modulate the VCO, resulting in energy or spectral distribution on both sides of the carrier. This occurs via modulation and frequency conversion. The noise, or better, AM and FM noise is expressed as the ratio of output power divided by the noise power relative to 1Hz bandwidth measured at an offset of the carrier. The diagram in Figure 2-7 shows the definition of phase noise at an offset frequency, $L(f_m)$. Suppose the resolution bandwidth is

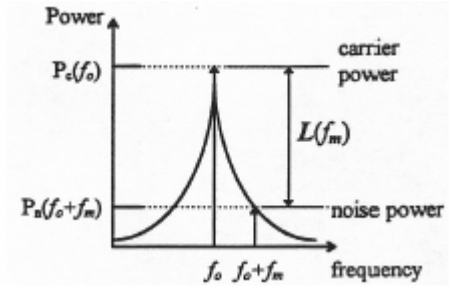


Figure 2-7. Phase noise definition.

BW, $L(f_m)$ can be expressed as

$$L(f_m) = 10 * \log\{\frac{P_n(f_0 + f_m)/P_c(f_0)}{BW}\} \quad (2\text{-}6)$$

At different offset frequency ranges, the phase noise has different change characteristic. Generally the offset frequencies can be split into three regions, $1/f^3$, $1/f^2$ and white noise floor regions.

Output Power —— The output power is measured at the designated output port of the frequency synthesizer. Practical designs require one or more isolation stages between the oscillator and the output. A typical output power level for a VCO is -15 to +10 dBm.

Frequency Pulling —— This is the change in oscillation frequency with change in supply voltage. It is caused by the change in the transistor's S-parameter and Gain with change in DC bias voltage. The supply voltage can drift with time, temperature, and load variations. Frequency pulling can be reduced by oscillator design with higher loaded quality factor (Q) of resonator.

Frequency Pushing —— It is the total output frequency deviation due to load perturbation. It can be minimized by using an output isolator, buffer amplifier, or high oscillator external Q.

Power Consumption —— This characteristic conveys the DC power, usually specified in milliwatts and sometimes qualified by operating voltage, required by the oscillator to function properly.

2.2. General Theory of Quadrature VCOs

2.2.1. Principle of Oscillation for LC Quadrature Oscillators

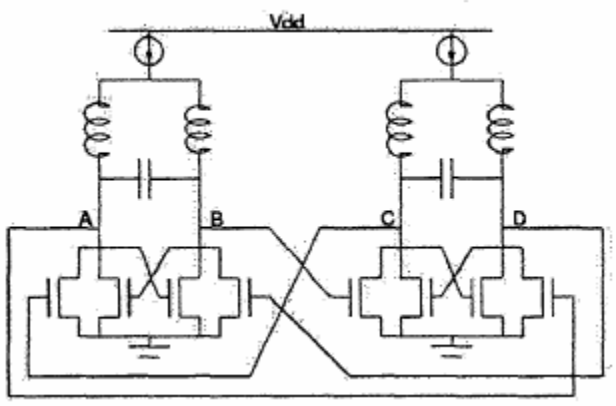


Figure 2-8. Schematic of a typical LC quadrature oscillator.

Figure 2-8 shows a typical LC quadrature oscillator. Its behavior can be modeled by a linear feedback network, as shown in Figure 2-9 [6]. It is composed of two band-pass filters representing the two oscillator cores of the quadrature oscillator. The gain stage of the differential oscillator core is represented by a negative impedance $-1/G_{m0}$, the LC-tank is represented by a parallel RLC model (L_p, C_p, R_p), and the coupling stage is represented by a transconductance G_{mc}.

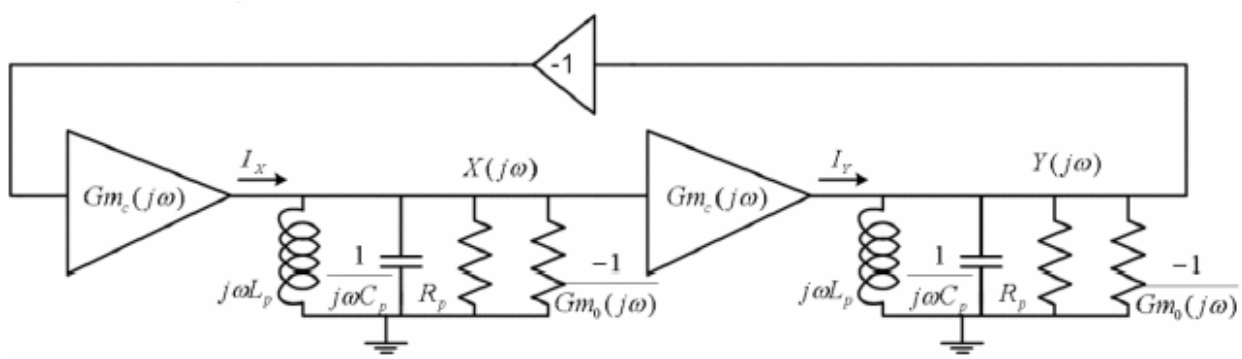


Figure 2-9. Linear feedback network model for LC quadrature oscillator.

The transfer function of the band-pass filter is given by

$$H_{1,2}(j\omega) = \frac{Gm_c(j\omega)\cdot j\omega L_p}{1 + j\omega L_p[\frac{1}{R_p} - Gm_0(j\omega)] - \omega^2 L_p C_p}. \tag{2-7}$$

At steady state, the outputs of the two band-pass filters satisfy the following equations:

$$\begin{aligned} X(j\omega) &= -H_1(j\omega)\cdot Y(j\omega) \\ Y(j\omega) &= H_2(j\omega)\cdot X(j\omega). \end{aligned} \tag{2-8}$$

Since $H_1(j\omega)$ and $H_2(j\omega)$ and are identical and X and Y are nonzero when the quadrature oscillator is in stable oscillation, the above equations will result in $X(j\omega) = \pm jY(j\omega)$. This indicates that X and Y are in a quadrature (90° phase shift) phase relationship.

2.2.2. Performance Parameters of LC Quadrature VCOs

By replacing the capacitors in Figure 2-8 with varactors, a LC quadrature VCO (QVCO) is formed. The performance parameters of a LC QVCO include all the parameters of a LC VCO, as listed in Section 2.1.3, and another important one, which is phase error.

Phase Error —— Any circuit mismatch could cause the phase difference between the quadrature outputs to shift from 90°. This shift is called phase error and is a measure of signal phase accuracy.

CHAPTER 3 PHASE NOISE MECHANISM OF LC OSCILLATORS

3.1. Thermal Noise Induced Phase Noise

3.1.1. Resonator Noise

We represent the white thermal noise of the tank conductance as a current source across the tank with a mean-square spectral density of [7]

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R_p}. \tag{3-1}$$

where k is the Boltzmann's constant, T is the temperature in Kelvins, and R_p is the parallel resistance of the resonator. This current noise becomes voltage noise when multiplied by the effective impedance facing the current source. In computing this impedance, however, it is important to recognize that the energy restoration element must contribute an average effective negative resistance that precisely cancels the positive resistance of the tank. Hence, the net result is that the effective impedance seen by the noise current source is simply that of a perfectly lossless LC network. For relatively small offset frequency from the center frequency, the

impedance of an LC tank may be approximated by

$$Z(\omega_0 + \Delta\omega) = -j\frac{\omega_0 L}{2\frac{\Delta\omega}{\omega_0}}. \tag{3-2}$$

The unloaded tank quality factor (Q) is defined as

$$Q = \frac{R_p}{\omega_0 L}. \tag{3-3}$$

Solving (3-3) for L and substituting into (3-2) yields

$$|Z(\omega_0 + \Delta\omega)| = \frac{R_p}{2Q}\left(\frac{\omega_0}{\Delta\omega}\right). \tag{3-4}$$

Thus, we have traded an explicit dependence on inductance for a dependence on Q and R_p. Next, multiply the spectral density of the mean-square noise current by the squared magnitude of the tank impedance to obtain the spectral density of the mean-square noise voltage

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f}|Z(\omega_0 + \Delta\omega)|^2 = 4kTR_p\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 = 4kTR_p\left(\frac{f_0}{2Q\Delta f}\right)^2. \tag{3-5}$$

The power spectral density of the output noise is frequency dependent because of the filtering action of the tank, falling as ***the inverse-square of the offset frequency***. This is called $1/f^2$ behavior. Note also that an increase in tank Q reduces the noise density, when all other parameters are held constant.

It is traditional to normalize the mean-square noise voltage density to the mean-square carrier voltage and report the ratio in decibels. This normalization yields the following equation

for the normalized single-sideband noise spectral density

$$L(\Delta f) = \frac{2kT}{P_{sig}} (\frac{f_0}{2Q\Delta f})^2. \quad (3\text{-}6)$$

where P_{sig} is the signal power.

3.1.2. Tail Current Noise

The switching action of the differential pair commutates noise in the tail currents like a single-balanced mixer. The noise is translated up and down in frequency, and enters the resonator. Here we only look into the down-conversion of the thermal noise at $2\omega_0$. The up-conversion of flicker noise will be investigated in a later section. The single-balanced mixer shows the largest conversion gain around the fundamental switching frequency, 1/3rd the current conversion gain around the 3rd harmonic, and so on. Therefore, only mixing by the fundamental is important. The phase noise caused by thermal noise of the tail current originally at $2\omega_0$, is [8]

$$L(\Delta f) = \frac{8}{9} \gamma g_{m,tail} \frac{kTR_p}{P_{sig}} (\frac{f_0}{2Q\Delta f})^2. \quad (3\text{-}7)$$

where γ is the noise factor of a single FET, typically 2/3 for the long-channel mode while it is between 2 to 3 for the short channel region [9]. $g_{m,tail}$ is the transconductance of the tail transistor and P_{sig} is the output signal power.

3.1.3. Differential Pair Noise

Noise originating in the differential pair is unlike the previous two cases. There, only certain parts of the noise spectrum contributed significantly to the total phase noise. White noise in the resonator is filtered at harmonics of the resonant frequency. White noise in the tail current

only experiences a significant conversion gain around the second harmonic of the oscillation frequency. However, an impulse train samples white noise in the differential pair and will cause it to accumulate without bound at any specified offset frequency ω_m.

In reality, any practical differential pair requires a non-zero input voltage excursion to switch, and this is provided by the oscillation waveform across the resonator. Therefore, noise in the differential pair is actually not sampled by impulses, but by time windows of finite width. The window height is proportional to transconductance, and width is set by tail current and the slope of the oscillation waveform at zero crossing. The input-referred noise spectral density of the differential pair is inversely proportional to transconductance. Thus, the narrower the sampling window, that is, the larger the sampling bandwidth, the lower the noise spectral density. Analysis shows that the noise bandwidth product is constant, and produces pure phase noise. After taking into account the accumulation of frequency translations throughout the sampling bandwidth, the following compact yet exact expression is reached [8]

$$L(\Delta f) = \frac{8 I_{tail} \gamma}{\pi V_0} \frac{kTR_p}{P_{sig}} \left(\frac{f_0}{2Q\Delta f} \right)^2 . \tag{3-8}$$

where V_0 is the voltage amplitude of the oscillation signal. The relationship between V_0 and P_{sig} is

$$P_{sig} = \frac{\left(V_0 / \sqrt{2} \right)^2}{R_p} \tag{3-9}$$

3.2. Flicker Noise Induced Phase Noise

Flicker noise in the tail current source at frequency ω_m is upconverted to $\omega_0 \pm \omega_m$ and enters the resonator as AM noise by the single-ended balanced mixer mechanism of the

switching pair. Assume the resonator oscillation frequency is ω_0, the DC bias current of the tail is I_b, the equivalent parallel resistance of the resonator is R_p, and the flicker noise of the tail is modeled as a voltage source in series with the gate, v_{fn}. The resonator differential output voltage can be expressed as

$$\begin{aligned} V_o &= \mathrm{sgn}\left[\cos(\omega_0 t)\right]\left(R_p I_b + R_p g_{m,tail} v_{fn}\right) \\ &= \left[\frac{1}{2} + \frac{2}{\pi}\cos(\omega_0 t) + ...\right]\left(R_p I_b + R_p g_{m,tail} v_{fn}\right). \end{aligned} \tag{3-10}$$

The term $\frac{2}{\pi}\cos(\omega_0 t)\left(R_p I_b + R_p g_{m,tail} v_{fn}\right)$ represents the AM noise at the resonator output generated from the flicker noise of the tail. Now let us look at the AM to FM conversion through varactors. The AM-to-FM factor can be defined as [10]

$$K_{AMFM} = \frac{\partial \omega_0}{\partial V} = \frac{\partial}{\partial V}\left(\frac{1}{\sqrt{LC_{eff}}}\right) = -\frac{1}{2}\frac{\omega_0}{C_{eff}}\frac{\partial C_{eff}}{\partial V}. \tag{3-11}$$

where C_{eff} is the effective capacitance of the varactor and V is the voltage across the varactor. Improving the symmetry of the VCO can reduce the value of K_{AMFM} [10]. We can use standard formulas to predict the spectral density of these FM sidebands at an offset from the oscillation frequency,

$$L(\Delta f) = J_1^{\,2}\left[\frac{1}{2\pi\Delta f} K_{AMFM} V_{fn}^{\,2}(\Delta f)\right] \simeq \left(\frac{K_{AMFM}}{4\pi\Delta f}\right)^2 V_{fn}^{\,2}(\Delta f). \tag{3-12}$$

since v_{fn} at the frequency of Δf can be expressed as

$$v_{fn}^{\ 2}(\Delta f) = \frac{K}{WLC_{ox}\Delta f} \tag{3-13}$$

where K is dependent on device characteristics and can vary widely for different devices in the same process. The variables W, L, C, and C_{ox} represent the transistor's width, length, and gate capacitance per unit area, respectively. Plugging (3-13) into (3-12)

$$L(\Delta f) = \left(\frac{K_{AMFM}}{4\pi\Delta f} \right)^2 \frac{K}{WLC_{ox}\Delta f}. \tag{3-14}$$

Therefore, the power spectral density of the output noise due to the flicker noise of the tail falls with ***the inverse-cubic of the offset frequency***. This is called $1/f^3$ behavior.

3.3. Phase Noise Model of LC Oscillators

Based on the analysis above, a unified model for the phase noise of LC oscillators in log scale can be defined as below [7]

$$L(\Delta f)_{\log} = 10 \cdot \log \left\{ \frac{2FkT}{P_{sig}} \cdot \left[1 + \left(\frac{f_0}{2Q\Delta f} \right)^2 \right] \cdot \left(1 + \frac{\Delta f_{1/f^3}}{|\Delta f|} \right) \right\}. \tag{3-15}$$

where $\Delta f_{1/f3}$ is the $1/f^3$ corner frequency and F is a noise factor for the region where phase noise falls at -20dBc/Hz which can be defined as

$$F = 1 + \frac{4\gamma R_p I_{tail}}{\pi V_0} + \gamma \frac{4}{9} g_{m,tail} R_p \tag{3-16}$$

Note (3-14) is a modified Lesson's model [11]. It consists of a factor to account for the noise in the $1/f^2$ region, an additive factor of unity (inside the braces) to account for the noise floor, and a

multiplicative factor (the term in the second set of parentheses) to provide a $1/f^3$ behavior at sufficiently small offset frequencies. With these modifications, the phase-noise spectrum appears as in Figure 3-1.

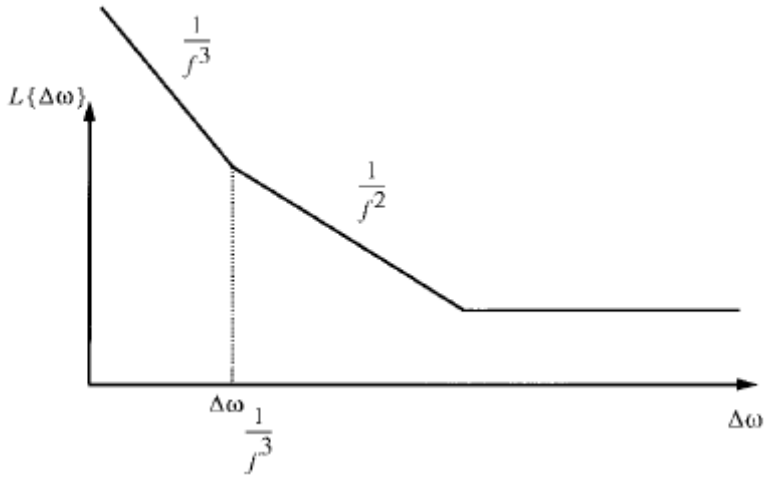


Figure 3-1. Phase noise plot over different frequency regions.

CHAPTER 4 DESIGN OF A LOW-PHASE-NOISE VCO WITH CAPACITOR TAPPING

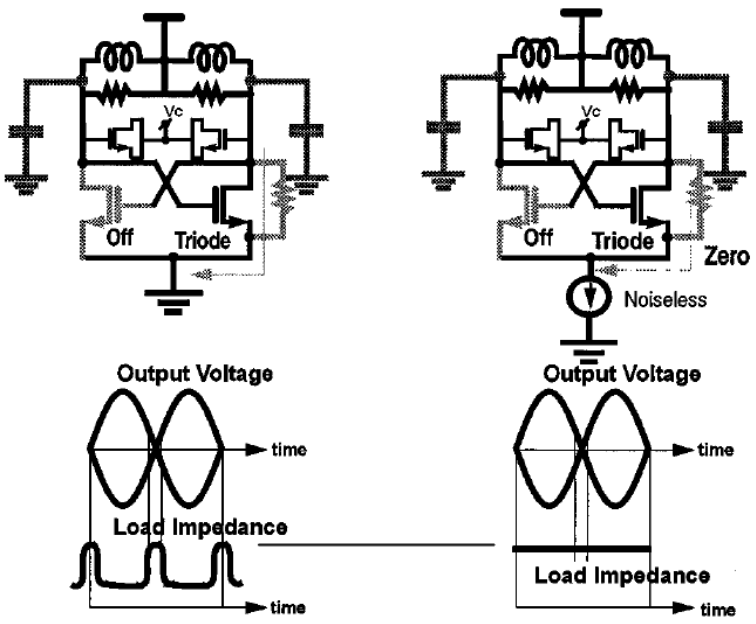
4.1. Introduction

Resonator voltage amplitude has an important effect on the phase noise, as emphasized by the presence in the denominator of the phase noise expression derived in Chapter 3. Seen from (3-

15), the phase noise can be lowered by increasing P_{sig}, which is proportional to the square of the oscillation voltage amplitude.

The resonator quality factor is affected by the impedance of the current source. Considering the differential LC VCO where the current source is replaced by low impedance to ground; in the extreme case a short circuit as shown in Figure 4-1(a) [12]. This circuit still produces steady-state oscillation. The oscillator topology forces V_{GD} of the two FETs to be equal in magnitude but with opposite signs to the differential voltage across the resonator. At zero differential voltage, both switching FETs are in saturation, and the cross-coupled transconductance offers a small-signal negative differential conductance that induces startup of the oscillation. As the rising differential oscillation voltage crosses V_t, the V_{GD} of one FET exceeds $+Vt$, forcing it into the triode region, and the other FET is turned off. The r_{DS} of the FET in triode is the load impedance to the tank, and its small value degrades the loaded quality factor of the tank. (4-1) formulizes the relationship between loaded Q, Q_L and unloaded Q, Q_U for LC tank as a function of the loading resistance $R_{L,}$ tank inductance L and oscillation frequency ω_0.

$$Q_L = \frac{Q_U R_L}{Q_U \omega_0 L + R_L}. \tag{4-1}$$



(a) **(b)**

Figure 4-1. Role of the current source. (a) No current source. (b) Ideal noiseless current source.

Now, suppose an ideal noiseless current source is present in the tail of the differential pair, as shown in Figure 4-1(b). Close to zero differential voltage, the two FETs conduct and present a negative conductance across the resonator. Suppose that in the balanced condition when each FET carries $I/2$, the W/L is chosen such that $(V_{GS}-V_t) < V_t$. When the differential voltage drives one FET into triode, it turns off the other FET. As no signal current can flow through the g_{DS} of the triode FET, this FET does not load the resonator, thus preserving quality factor of the unloaded resonator. The differential pair injects noise into the resonator only over the short window of time when both FETs conduct.

Based on the description above, high source-to-drain impedance is required for the current source in order to prevent the loss of resonator quality factor. For that purpose, the current source needs to be maintained in the saturation region, which is a big challenge for low voltage design. As illustrated in the first paragraph, large oscillation amplitude is desired for low phase noise, but

can push the current source into triode region, which is especially the case for low voltage design. If the VCO uses a PMOS current source and NMOS cross-coupled switching pair, which is usually the optimal VCO structure due to the low flicker noise of PMOS and large transconductance of NMOS, a large oscillation signal can also push the switching transistor into triode and generate a low impedance path to ground that adds more loss to the resonator quality factor. Figure 4-2 illustrates the situation.

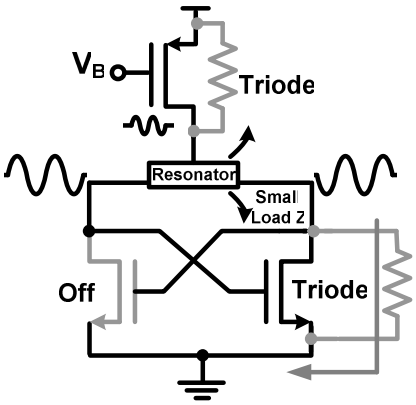


Figure 4-2. Low load impedance caused by the large oscillation amplitude.

4.2. Proposed Architecture and Design Implementation

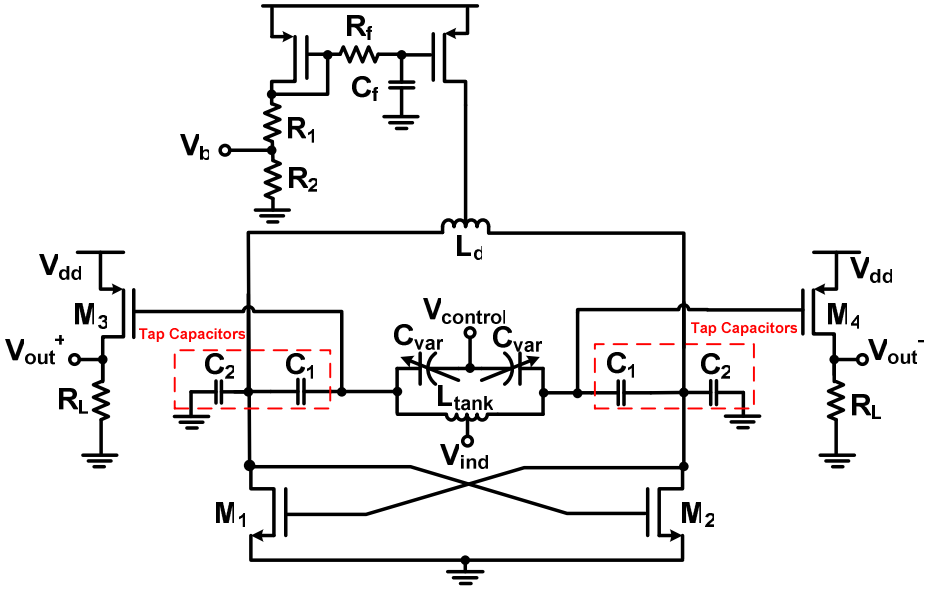


Figure 4-3. Proposed LC VCO with capacitor tapping technique.

Figure 4-3 shows the proposed LC VCO with capacitor tapping technique. PMOS is adopted for the current source because PMOS has lower flicker noise than NMOS [13] and as we know from Section 3.2, the flicker noise of current source can be upconverted to phase noise. The length of the PMOS is 1μm, which is large for the purpose to reduce flicker noise. NMOS is adopted for the cross-coupled pair because NMOS has higher transconductance than PMOS. As shown in Section 3.1.3, large transconductance of the cross-coupled pair leads to large oscillation amplitude and smaller sampling window which mean lower phase noise. Since the flicker noise of cross-coupled pair does not affect phase noise as illustrated in Section 3.2., the larger flicker noise in the pair caused by NMOS is not a problem to phase noise.

Seen from Figure 4-3, tap capacitors C_1 and C_2 are inserted between the resonator and the cross-coupled pair. They are equivalent to a voltage divider and scale down the voltage at the drains of the cross-coupled pair, V_{drain}. Thus, V_{drain} can be expressed as

$$V_{drain} = V_{\tan k} \frac{C_1}{C_1 + C_2}. \tag{4-2}$$

where V_{tank} is the tank output voltage. In this way, even though V_{tank} has a large value, V_{drain} can be small due to the capacitive voltage division. Therefore, the current source and turned-on cross-coupled transistor can be maintained in saturation leading to large loaded Q while the amplitude of the oscillation signal at the tank is still large leading to a large signal-to-noise ratio (SNR) as shown in Figure 4-4. Both of the effects contribute to low phase noise and the tradeoff between oscillation amplitude and loaded Q illustrated in Section 4.1 is solved.

The idea of capacitor tapping was used in differential Clapp VCO [14] for a purpose to avoid transistor breakdown, but is for the first time to be used in a cross-coupled LC QVCO for loaded Q enhancement.

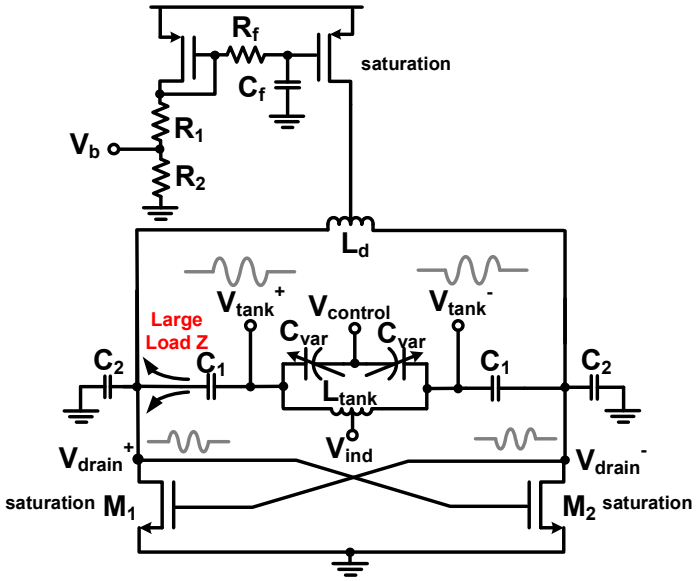
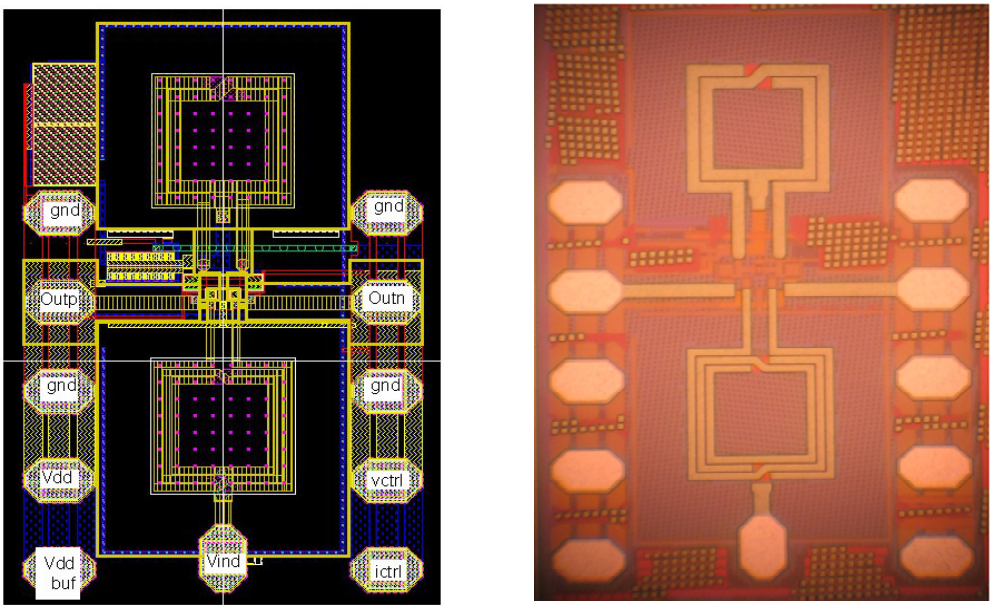


Figure 4-4. Impact of capacitor tapping on load impedance (load Z).

Figure 4-5 shows the layout and the chip photo of the proposed VCO implemented in Jazz 0.18µm RF CMOS process. The resonator consists of a center-tapped differential square



(a) **(b)**

Figure 4-5. (a) Layout of the proposed VCO. (b) Chip photo of the proposed VCO.

spiral inductor and a pair of accumulation-mode MOS varactors. The resonator inductor has an inductance of 1.28nH and a *Q* of 12 at 5.8GHz. The bias inductor at the drain of current source is

sized to 0.52nH with a Q of 16 at 5.8GHz. Surrounding the inductors, there are guard rings connected to ground for substrate noise suppression. Precision of the tapping ratio is important so MIM capacitors are used for the tapping capacitors. C_1 is 1.08pF and C_2 is 1.08pF. The divide ratio should be about 2 according to (4-2). The two output buffers employ a common source amplifier structure and the output PMOS devices need to be small to minimize its negative impact on frequency tuning capability. In addition to that, all the RF signal paths are routed with the top metal, where possible, in order to mitigate the impact of substrate noise on the VCO performance. The final size of the VCO die is 636μm by 980μm.

4.3. Simulation and Measurement Results

4.3.1. Simulation Results

Simulation was run in Cadence SpectreRF. Drawing 5mA from a 1.2V supply, the VCO oscillates at 5.6 to 5.8GHz when the control voltage tunes from 0 to 1.8V. Figure 4-6 shows its phase noise plot at 100Hz to 1MHz offsets from the carrier frequency of 5.6GHz. The phase noise is -101.8dBc/Hz at 100kHz offset and -122.3dBc/Hz at 1MHz offset. According to the

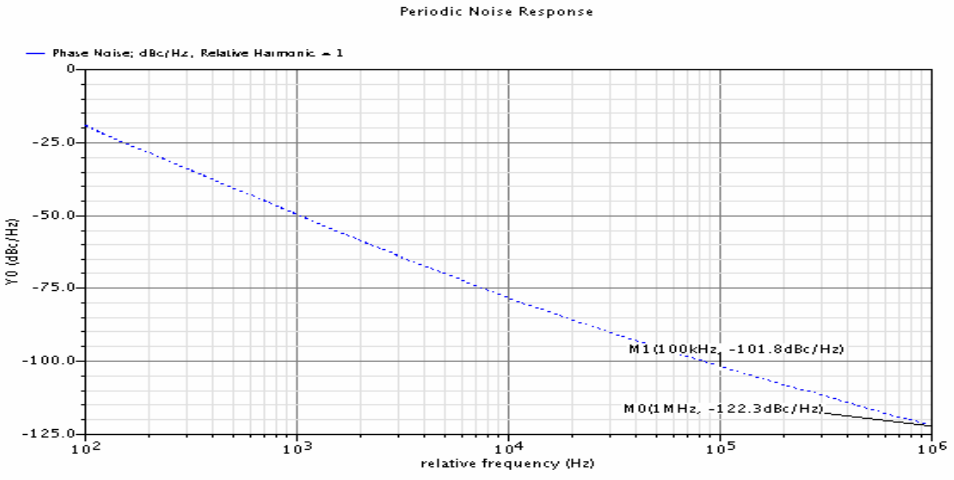
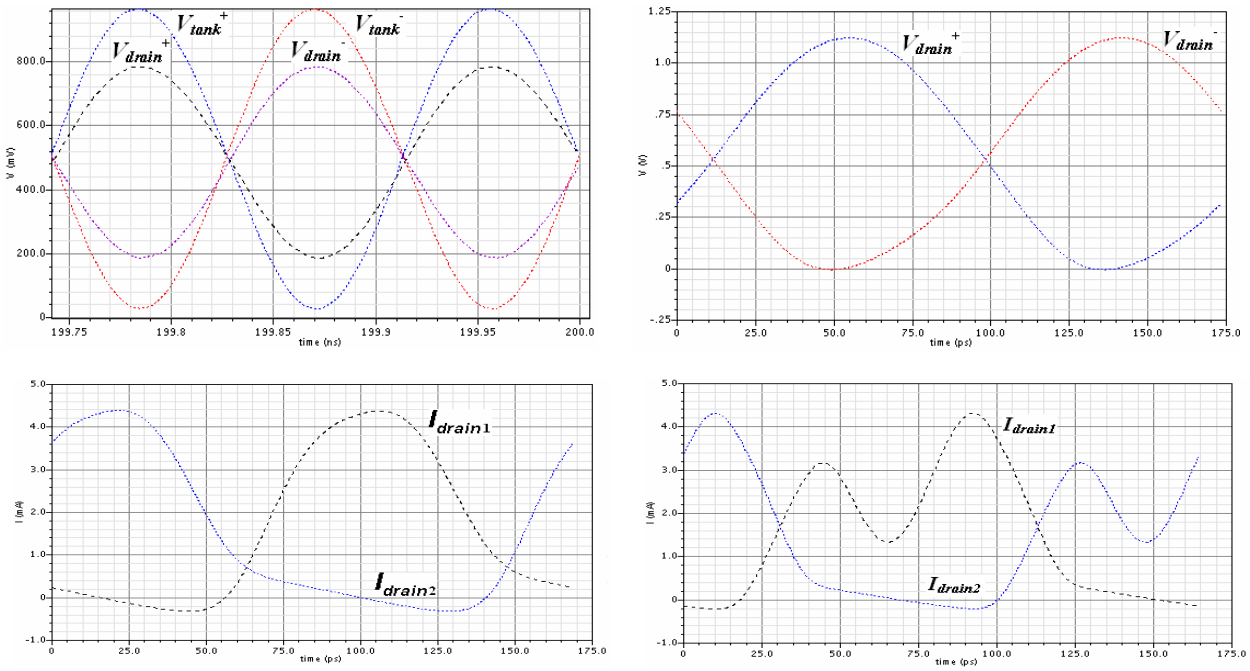


Figure 4-6. Simulated phase noise of the proposed VCO.



(a) **(b)**

Figure 4-7. Simulated voltage and current responses of the proposed VCO (a) with capacitor tapping (b) without capacitor tapping.

equation for figure-of-merit (FOM) of VCOs as below

$$FOM = -L(\Delta f) + 20\log(\frac{f_o}{\Delta f}) - 10\log(P) \qquad (4\text{-}3)$$

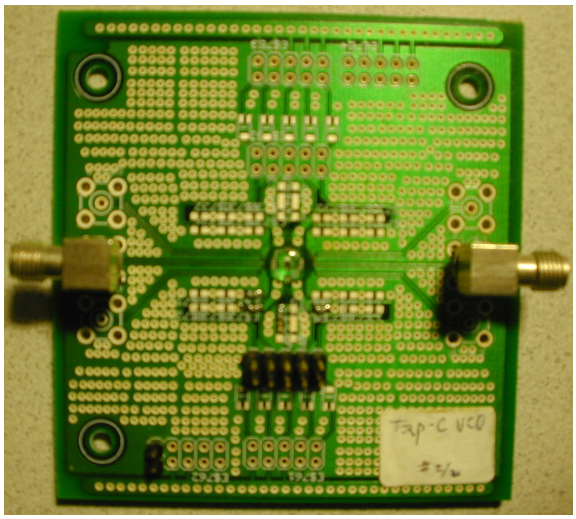
the simulated FOM of the proposed VCO is -189.5dBc/Hz at 1MHz offset.

To see the effect of capacitor tapping on the circuit operation, voltage and current responses of the proposed VCO with and without capacitor tapping are compared in Figure 4-7. When capacitor tapping is employed, as shown in Figure 4-7 (a), though the peak-to-peak tank output voltage V_{tank} is almost 1V, the peak-to-peak value of the drain voltage of the cross-coupled pair V_{drain} is only 600mV, close to the threshold voltage of the NMOS transistor, which means the NMOS cross-coupled transistors are in saturation during most of the time when they are turned on. The positive peak of V_{drain} is 800mV which is also far away from pushing the

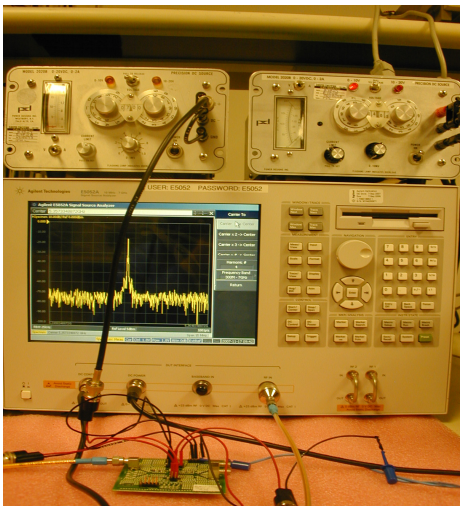
PMOS into the triode region. The drain current of the cross-coupled transistors shows the normal differential operation. However, without using the capacitor tapping, the 1V peak-to-peak V_{drain} would push both the current source and cross-coupled transistors in to triode. As shown in Figure 4-7 (b), the drain current shows the second-harmonic effect which implies that the bias current is not constant.

4.3.2. Measurement Results

The VCO chip is wire-bonded to a PCB board for characterization. This is a four-layer FR-4 (Flame Retardant 4) board with copper covering. The RF paths on the board are exactly symmetric. Three 0603 chip capacitors, which have a good spread of value as 10pF, 10nF, 0.1uF, are put in parallel at the power lines and gate bias lines of the current source to filter out high-frequency noise. Figure 4-8 (a) shows the photo of the board and Figure 4-8 (b) shows the measurement setup. A Agilent E5250A Signal Source Analyzer is used as both a spectrum analyzer and a phase noise analyzer capable of measuring up to 7GHz. It has a DC control voltage output and a DC power voltage output and can lock a free-running VCO by internal PLL. Precision DC voltage supplies provide low-noise DC biases to the chip. All the RF connections including the SMA connectors, RF cables and the load impedance of the signal source analyzer have a 50Ohm characteristic to guarantee no signal reflection. Short and low-loss RF cables and DC wires are used as additional insurance for signal integrity.



(a)



(b)

Figure 4-8. (a) PCB board with the proposed VCO chip. (b) Measurement setup.

The VCO is tested at a 1.8V supply and draws a current of 7mA. Figure 4-9 shows it oscillates at 4.57GHz with an output power of -10.3dBm when the control voltage is 1.8V. The spectrum span in the figure is 3MHz. The phase noise plot at 1kHz to 40MHz offset from the carrier frequency of 4.57GHz is shown in Figure 4-10. The VCO achieves phase noise of -120dBc/Hz at 1MHz offset, -94dBc/Hz at 100kHz offset and -63dBc/Hz at 10kHz offset respectively. Thus, the measured FOM of the proposed VCO is -182.3dBc/Hz at 1MHz offset. Table 4-1 summarizes the simulated and measured results. The measured oscillation frequency is lower than simulation which could be caused by the inaccurate prediction of inductance value and parasitic capacitance value. However, overall, the measured FOM is close to the simulated result. Table 4-2 compares the performance of this work with the published results. The FOM of the proposed design is one of the best among the 5GHz VCO designs.

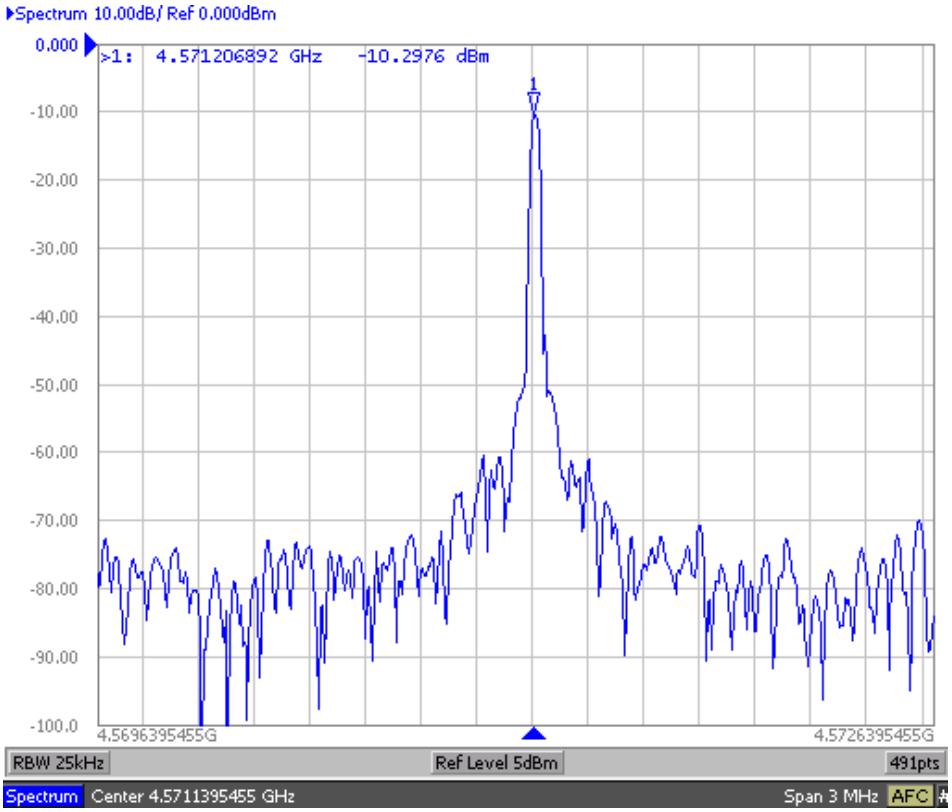


Figure 4-9. Spectrum of the VCO output under measurement.

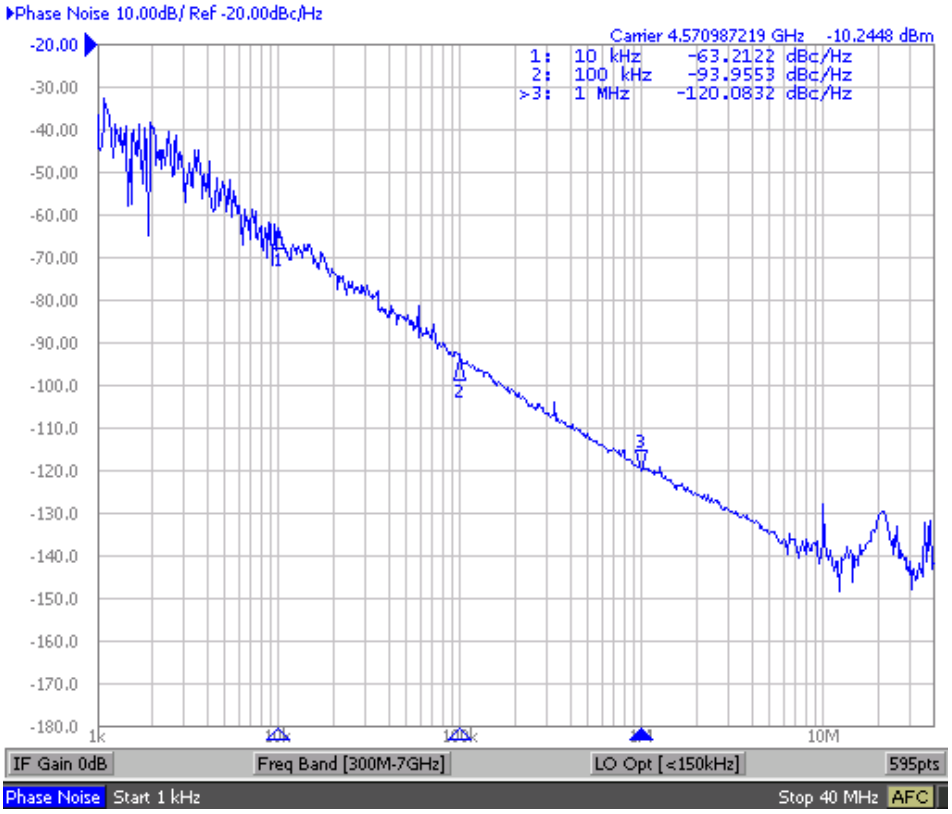


Figure 4-10. Phase noise plot of the VCO under measurement.

Table 4-1. Performance summary of the proposed VCO with capacitor tapping.

	Simulation Results	Measurement Results
Supply voltage (V)	1.2	1.8
Current consumption (mA)	5	7
Oscillation frequency (GHz)	5.62-5.80	4.37-4.57
Phase noise @ 1MHz offset (dBc/Hz)	-122.3 (5.62GHz)	-120.1 (4.57GHz)
Output power (dBm)	-7.5	-10.3
FOM (dBc/Hz)	-189.5	-182.3

Table 4-2. Performance comparison between the proposed VCO and the published VCO designs.

Ref.	**Tech.**	**F (GHz)**	**VDD (V)**	**P (mW)**	**L@ 1MHz (dBc/Hz)**	**FOM (dBc/Hz)**
[14]	0.18µm CMOS	4.95 5.97	1.8	9	-123.1@5.9G	-189 (simulated)
[15]	0.18µm CMOS	4.40 5.90	0.8	1.2	-109.65@5.52G	-184 (simulated)
[16]	0.18µm CMOS	4.92 5.12	1	6	-125@5G	-192 (measured)
[17]	0.25µm CMOS	4.32 5.30	2.5	7.3	-114.6 @4.95G	-180 (measured)
This Work	**0.18µm CMOS**	**4.37 4.57**	**1.8**	**12.6**	**-120.1 @4.57G**	**-182.3 (measured)**

CHAPTER 5 DESIGN OF A LOW-PHASE-NOISE QVCO WITH BOTTOM-SERIES COUPLING AND CAPACITOR TAPPING

5.1. Introduction

The conventional LC QVCOs topology is called parallel-coupled QVCO (P-QVCO) [18], because the coupling transistors are placed in parallel with the switching pairs. As shown in Figure 5-1 (a), M_s and M_c represent switching and coupling transistor respectively. However, the parallel coupling FETs cause the current injected into the tank to have a phase shift relative to the resonator voltage which degrades the quality factor of the tank and the phase noise of the QVCO. In this thesis, this current phase shift relative to the resonator voltage is called as resonator phase shift (RPS). As mentioned in [19], the resonator Q can be defined as

$$Q = \frac{\omega_0}{2}\left|\frac{\partial\phi}{\partial\omega}\right| \tag{5-1}$$

where Φ is RPS. As shown in Figure 5-2, the maximum $|\partial\Phi/\partial\omega|$ is reached when Φ equals 0°which means a zero RPS maximizes Q. However, the P-QVCO has a non-zero RPS and the parallel coupling FETs add additional noise sources and consume extra current. All this indicates the parallel coupling method is not an optimum choice for low power low phase noise QVCO. A modification of the original P-QVCO was reported, where phase shifters are added between cascaded LC resonators, allowing each resonator to be optimally driven at a zero-degree RPS [20]. However, phase shifters introduce some complication in the design and increase power

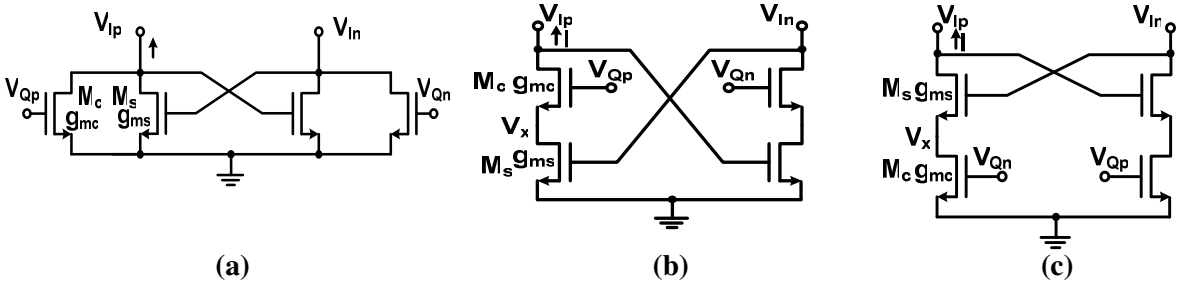


Figure 5-1. Topology of (a) parallel coupling (b) top-series coupling and (c) bottom-series coupling.

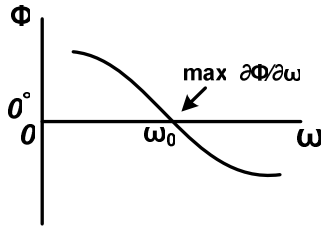


Figure 5-2. Phase characteristic of the resonator.

consumption. Therefore, a LC QVCO topology with an inherent zero RPS is needed.

Two series-coupled QVCO (S-QVCO) topologies as shown in Figure 5-1 (b)-(c) have also appeared in literature and showed much better phase noise performance than the P-QVCO. According to the position of coupling FETs, the S-QVCO which places the coupling transistors

at the top of the switching cross-coupled pair is called top-series-coupled QVCO (TS-QVCO) and the S-QVCO which places the coupling transistors at the bottom of the switching pair is called bottom-series-coupled QVCO (BS-QVCO). Measurement results showed that BS-QVCO has even better phase noise behavior than TS-QVCO [21], however, no theoretical explanation was given. It was pointed out that BS-QVCO has a zero RPS which benefits phase noise [22], however, the analysis was not in depth and did not show any hint for the RPS of TS-QVCO which would a good base for the comparison between different QVCO topologies. In this chapter of the thesis, a detailed analysis is provided indicating that BS-QVCO does have a zero RPS and TS-QVCO has a 90° RPS so BS-QVCO has lower phase noise than TS-QVCO. A closed-form expression of the optimal coupling ratio for the phase noise of BS-QVCO is also derived based on RPS analysis. Therefore, the bottom-series coupling method is chosen and combined with the capacitor tapping technique targeting to achieve a low-voltage low-phase-noise QVCO design.

5.2. RPS analysis for BS-QVCO and TS-QVCO

In Figure 5-1, V_{Ip}, V_{Qp} V_{In}, and V_{Qn} are the quadrature output signals among which the phase angles are increasing progressively in an order of 90°. For the series-coupling topologies in Figure 5-1 (b)-(c), since that V_X is much smaller than the quadrature output voltages due to source degeneration, it can be assumed that the top transistors work in saturation region while the bottom ones work in triode region during most of the oscillation period. Therefore, a compact circuit model fitting both S-QVCOs is developed as shown in Figure 5-3. M_1 and M_2 represent

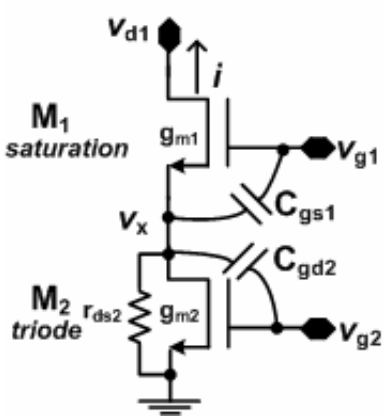


Figure 5-3. Small-signal circuit model diagram for S-QVCOs.

the top transistor and the bottom-transistor in the S-QVCOs respectively. The g_{m1} and g_{m2} are the small-signal transconductance of M_1 and M_2. C_{gs1} is the gate-source capacitance of M_1 in saturation region. C_{gd2} and r_{ds2} are the gate-drain capacitance and on-resistance of M_2 in triode region. The small-signal voltages v_{d1}, v_{g1} and v_{g2} represent the small-signal voltages, v_{Ip}, v_{Qp} and v_{In} for TS-QVCO and v_{Ip}, v_{In} and v_{Qn} for BS-QVCO. Therefore, v_{g2} equals to jv_{g1} for both the S-QVCOs. The small-signal i is the current injected into the tank. According to the definition of RPS, RPS for S-QVCOs is the phase angle between i and v_{d1}. The small-signal Kirchhoff's Current Law equation at node x can be written as

$$(v_{g1}-v_x)(g_{m1}+j\omega C_{gs1}) = g_{m2}v_{g2} + v_x/r_{ds2} + (v_x - v_{g2})\,j\omega C_{gd2} \tag{5-2}$$

where ω is the operation angular frequency. Considering v_{g2} equals to jv_{g1} as illustrated before, an expression of v_x can be derived as below

$$v_x = v_{g1}\frac{(g_{m1}-\omega C_{gd2}) + j(\omega C_{gs1} - g_{m2})}{(g_{m1}+1/r_{ds2}) + j(\omega C_{gs1} + \omega C_{gd2})}. \tag{5-3}$$

If the phase angle of v_x/v_{g1} is defined as θ, there is

$$\tan\theta = \left[(\omega C_{gs1} - g_{m2}) - \frac{(g_{m1} - \omega C_{gd2})(\omega C_{gs1} + \omega C_{gd2})}{g_{m1} + 1/r_{ds2}}\right] \Big/ \left[(g_{m1} - \omega C_{gd2}) + \frac{(\omega C_{gs1} - g_{m2})(\omega C_{gs1} + \omega C_{gd2})}{g_{m1} + 1/r_{ds2}}\right]. \quad (5\text{-}4)$$

Assuming (g_{m1}+1/r_{ds2}) is much larger than (ωC_{gs1}+ωC_{gd2}) when ω is much smaller than the transistors' cutoff frequencies, (5-4) can be approximated to

$$\tan\theta \approx (\omega C_{gs1} - g_{m2}) \big/ (g_{m1} - \omega C_{gd2}). \quad (5\text{-}5)$$

Since g_{m1} is much larger than g_{m2}, ωC_{gs1} and ωC_{gd2}, we can assume that (ωC_{gs1}-g_{m2}) is much smaller than (g_{m1}-ωC_{gd2}) which leads to a conclusion that tanθ is close to zero. This implies that v_x is almost in phase with v_{g1}. Therefore, the current i, which is -g_{m1}(v_{g1}-v_x), is 180° out of phase with v_{g1}. For BSQVCO, v_{g1} is v_{In}, thus i is 180° out of phase with v_{In}. In other words, i is in phase with v_{Ip} and the RPS is zero. For TSQVCO, v_{g1} is v_{Qp}, thus i is 180° out of phase with v_{Qp} and 90° out of phase with v_{Ip} which leads to a 90° RPS. The phasor diagrams are shown in Figure 5-4. Since zero RPS optimizes the tank Q and phase noise of QVCO as illustrated before, BS-QVCO has better phase noise performance than TS-QVCO.

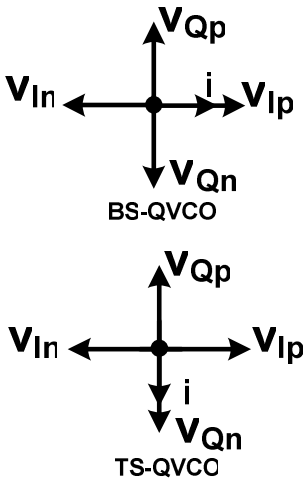


Figure 5-4. Phasor diagrams for BS-QVCO and TS-QVCO.

Though tanθ is close to zero according to (5-5), it equals to zero only when ωC_{gs1} equals to g_{m2}. The ωC_{gs1} for M_1 in saturation region can be expressed as

$$\omega C_{gs1} = (4/3)\pi f W_1 L_1 C_{ox} \tag{5-6}$$

where C_{ox} is the oxide capacitance, f is the operation frequency, W_1 and L_1 are the channel width and length of M_1. Assuming there is no channel length modulation, the DC bias current for M_2 in triode region can be expressed as

$$I_B = \mu_n C_{ox} (W/L)_2 \left[(V_G - V_{Tn}) V_X - V_X{}^2/2 \right] \tag{5-7}$$

where $(W/L)_2$ is the width over length ratio of M_2. V_G represents the same DC gate voltage that M_1 and M_2 have. Assuming V_G-V_{Tn}>>V_X, (5-7) leads to

$$g_{m2} = \mu_n C_{ox} (W/L)_2 V_X \approx I_B/(V_G - V_{Tn}). \tag{5-8}$$

The same DC bias current can also be written as the current going through M_1 in saturation region

$$I_B = \mu_n C_{ox}(W/L)_1(V_G - V_X - V_{Tn})^2/2$$
$$= \mu_n C_{ox}(W/L)_1\left[(V_G - V_{Tn})^2 + V_X{}^2 - 2(V_G - V_{Tn})V_X\right]/2. \quad (5\text{-}9)$$

From (5-7) it follows that

$$V_X{}^2 - 2(V_G - V_{Tn})V_X = -\frac{2I_B}{\mu_n C_{ox}(W/L)_2}. \quad (5\text{-}10)$$

Putting (5-10) into the second part of (5-9)

$$V_G - V_{Tn} = \sqrt{\frac{2I_B(1+\frac{(W/L)_1}{(W/L)_2})}{\mu_n C_{ox}(W/L)_1}}. \quad (5\text{-}11)$$

Plugging (5-11) into (5-8), g_{m2} then can be expressed as

$$g_{m2} = \frac{\sqrt{2}}{2}\sqrt{\frac{\mu_n C_{ox} I_B (W/L)_1}{1+\frac{(W/L)_1}{(W/L)_2}}}. \quad (5\text{-}12)$$

According to (5-6) and (5-12), ωC_{gs1} equals g_{m2} is valid when

$$\frac{(W/L)_1}{(W/L)_2} = \frac{9\mu_n I_B}{32\pi^2 C_{ox} f_0{}^2 L_1{}^3 W_1} - 1 = \frac{1}{\alpha_{BS,opt}} \quad (5\text{-}13)$$

where $\alpha_{BS,opt}$ is the optimal coupling ratio for the phase noise of BS-QVCO. Therefore, $\alpha_{BS,opt}$ is determined by the oscillation frequency, the bias current and the size of the switching FETs in a process. Simulation data in the next sections will prove the validity of (5-13) within the certain range allowed by the assumptions.

5.3. Proposed Architecture and Design Implementation

Since it is shown that BS-QVCO inherently has better phase noise behavior than TS-QVCO in the previous section, we choose bottom-series coupling for this QVCO design. Figure 5-5 shows the proposed bottom-series coupled LC QVCO with capacitor tapping technique. PMOS is adopted for the current sources and NMOS is adopted for the transconductance stages. The operation mechanism of capacitor tapping is the same as the one illustrated in Section 4.2. The QVCO outputs $V_{o,IP}$, $V_{o,Qp}$, $V_{o,In}$ and $V_{o,Qn}$ are still maintained large while the voltages at the drains of the cross-coupled pair, V_{Ip}, V_{Qp}, V_{In} and V_{Qn} are small. The two output buffers employ NMOS common source amplifier structure and are omitted in Figure 5-5.

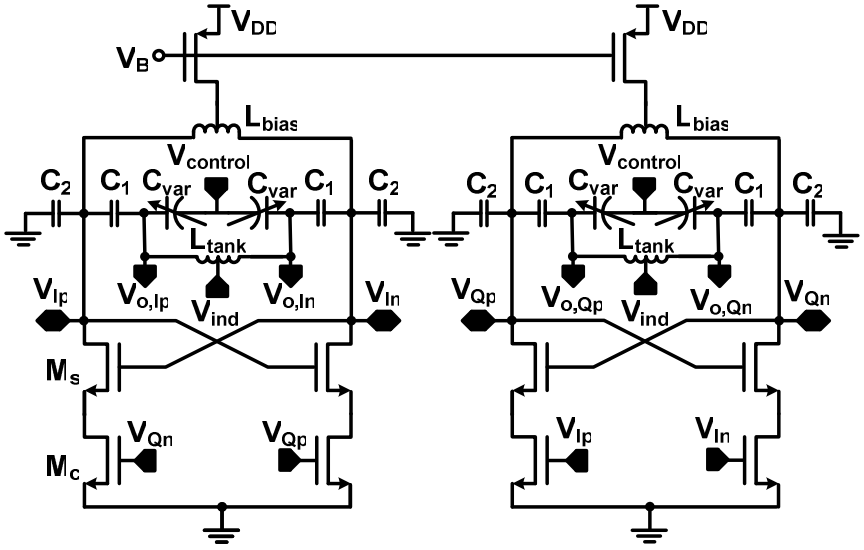
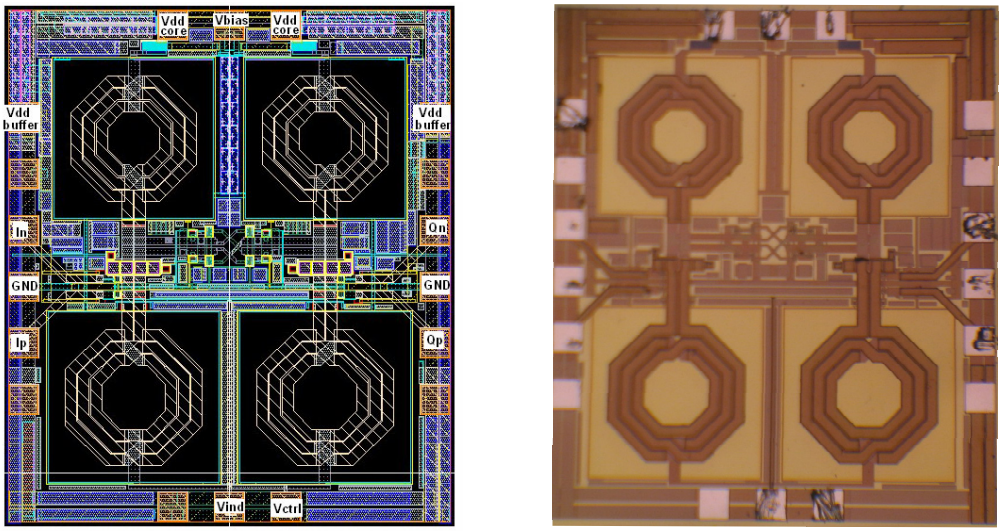


Figure 5-5. Proposed bottom-series coupled LC QVCO with capacitor tapping technique.

Figure 5-6 shows the layout and the chip photo of the proposed QVCO implemented in TSMC 0.18μm RF CMOS process. The resonator consists of a center-tapped differential octagonal spiral inductor and a pair of accumulation-mode MOS varactors. The resonator



(a) **(b)**

Figure 5-6. (a) Layout of the proposed BS-QVCO. (b) Chip photo of the proposed BS-QVCO.

inductor has an inductance of 2.5nH and a Q of 14 at 6GHz. The bias inductor at the drain of current source is sized to 2.1nH with a Q of 14 at 6GHz. Surrounding the inductors, there are guard rings connected to ground for substrate noise suppression. Precision of the tapping ratio is important so MIM capacitors are used as the tapping capacitors. C_1 is 500fF and C_2 is 400fF. The divide ratio is about 2 including the parasitic capacitance. The final size of the QVCO die is 1400μm by 1200μm.

The optimal coupling ratio for phase noise is determined by the (5-13) and the simulation results. Figure 5-7 shows the $\alpha_{BS,opt}$ simulated by Periodical Steady State (PSS) and Periodical AC (PAC) analyses. The W_c/W_s value at which the phase noise is the lowest is $\alpha_{BS,opt.}$ Seen from the figure, the optimal phase noise is -120.3dBc/Hz at 1MHz offset which is achieved when W_c/W_s equals 0.9. The design parameters are summarized in Table 5-1. The value of W_1 is relatively large to ensure that g_{m1} is large enough to meet the assumption that M_1 is in saturation. Seen from the table, the calculated $\alpha_{BS,opt}$ is 0.86 and has a percentage error of 4.4% from the simulated $\alpha_{BS,opt,}$ which is not significant.

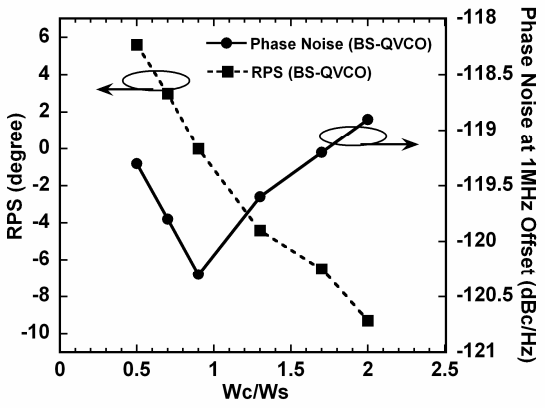


Figure 5-7. RPS and phase noise plots for determining the optimal coupling ratio.

Table 5-1. Summary of the optimal coupling ratio for the proposed BS-QVCO with capacitor tapping.

Specification	Value
I_B (bias current of single branch)	1.2mA
f_0	6GHz
W_1	250μm
L_1	0.18μm
Calculated $\alpha_{BS,opt}$	0.86
Simulated $\alpha_{BS,opt}$	0.9
Percentage Error	4.4%

5.4. Simulation and Measurement Results

5.4.1. Simulation Results

Figure 5-8 shows the simulated phase noise performance of the proposed QVCO at the carrier frequency of 6GHz under 1V power supply and 5mA bias current. The phase noise at 100kHz and 1MHz offset are -99.8dBc/Hz and -120.3dBc/Hz respectively. The transient responses of the quadrature outputs outside the buffers are shown in Figure 5-9. The single-ended output amplitude is 140mV which translates into an output power of -7dBm with a 50Ω load. The transient responses of $V_{o,Ip}$, V_{Ip} and I are shown in Figure 5-10. Seen from the plots, V_{Ip} is about half of $V_{o,Ip}$ which matches the divide ratio of capacitor tapping. I is the current injected into the

tank at node I_p and is almost in phase with V_{Ip} and $V_{o,\ Ip}$ which demonstrates the RPS of the proposed QVCO is close to zero.

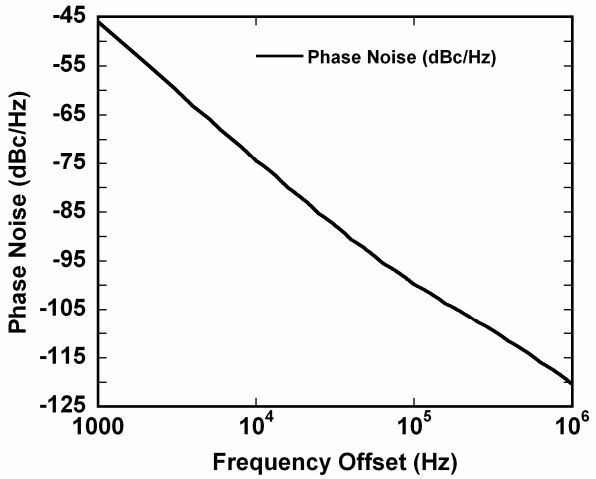


Figure 5-8. Phase noise plot for the proposed QVCO.

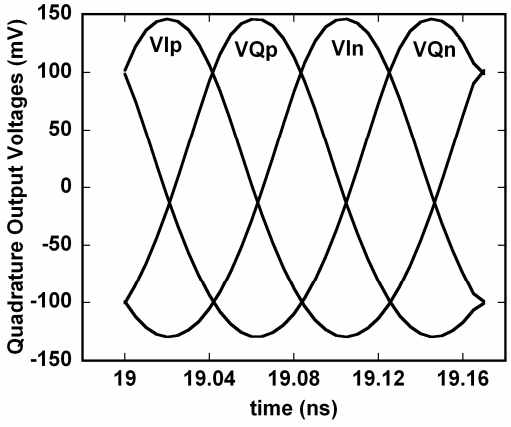


Figure 5-9. Transient responses of the quadrature outputs.

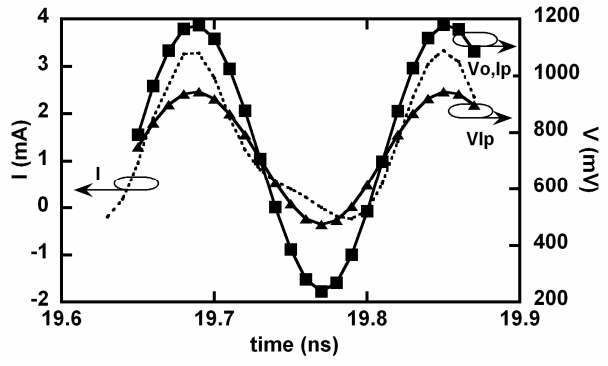
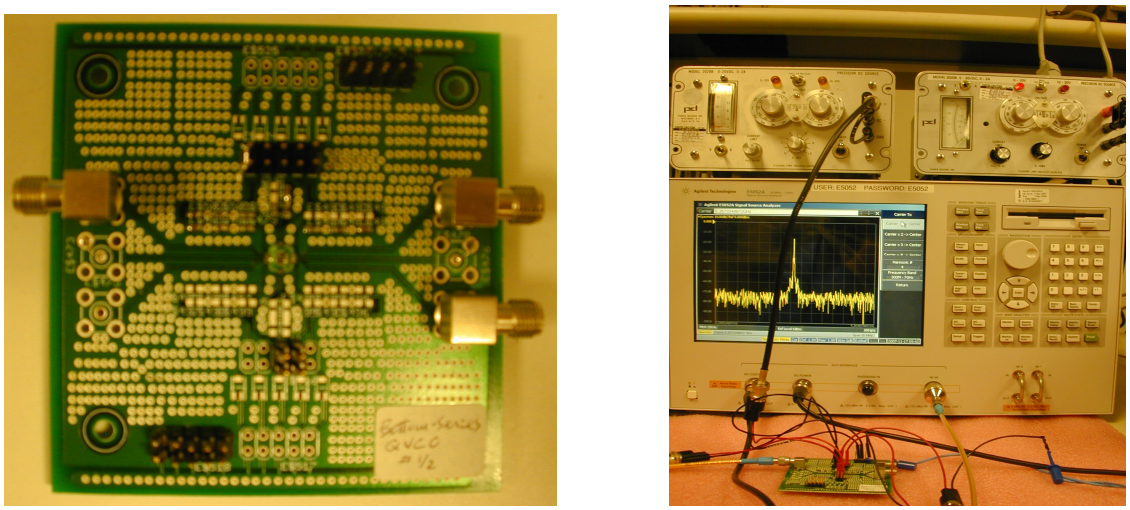


Figure 5-10. Transient responses of V_{Ip}, $V_{o,Ip}$ and I.

5.4.2. Measurement Results

The VCO chip is wire-bonded to a PCB board for characterization. Figure 5-11 (a) shows the photo of the board and Figure 5-11 (b) shows the measurement setup. The measurement setup is the same as the one for the VCO test in Chapter 4.



(a) **(b)**

Figure 5-11. (a) PCB board with the proposed BS-QVCO chip. (b) Measurement setup.

Figure 5-12 and Figure 5-13 show the measured QVCO performance at 1.8V supply voltage. Figure 5-12 shows the output spectrum at a carrier frequency of 5.34GHz. As shown in Figure 5-13, the QVCO achieves phase noise of -122.9dBc/Hz at 1MHz offset, -92.5dBc/Hz at 100kHz offset and -63.6dBc/Hz at 10kHz offset from the carrier frequency of 5.375GHz with an output power of -7.14dBm. The DC core current consumption is 10mA. The measured FOM of QVCO is -185dBc/Hz at 1MHz offset at 1.8V supply.

Figure 5-14 and Figure 5-15 show the measured QVCO performance at 1V supply voltage. Figure 5-14 shows the output spectrum at a carrier frequency of 5.325GHz. The output power is smaller than that at 1.8V supply even if biased at the same core current of 10mA. As shown in Figure 5-15, the QVCO achieves phase noise of -117.6dBc/Hz at 1MHz offset, -89.7dBc/Hz at 100kHz offset and -58.5dBc/Hz at 10kHz offset from the carrier frequency of

5.327GHz with an output power of -9.98dBm. The poorer phase noise compared to 1.8V condition is caused by the smaller output signal power. The measured FOM of QVCO is -182dBc/Hz at 1MHz offset at 1V supply.

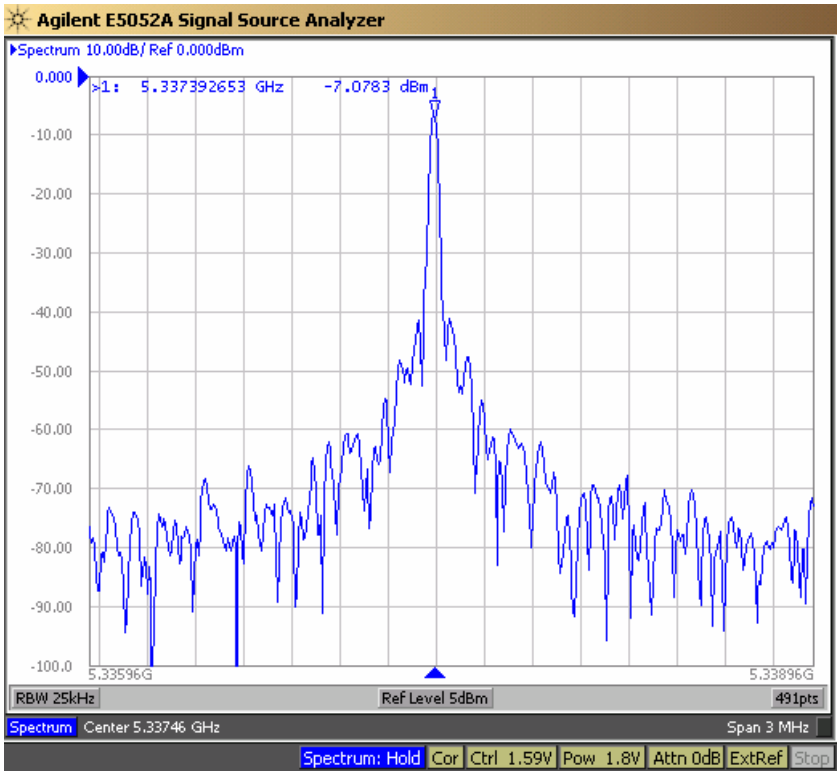


Figure 5-12. Output spectrum at the carrier frequency of 5.34GHz under 1.8V supply voltage under test.

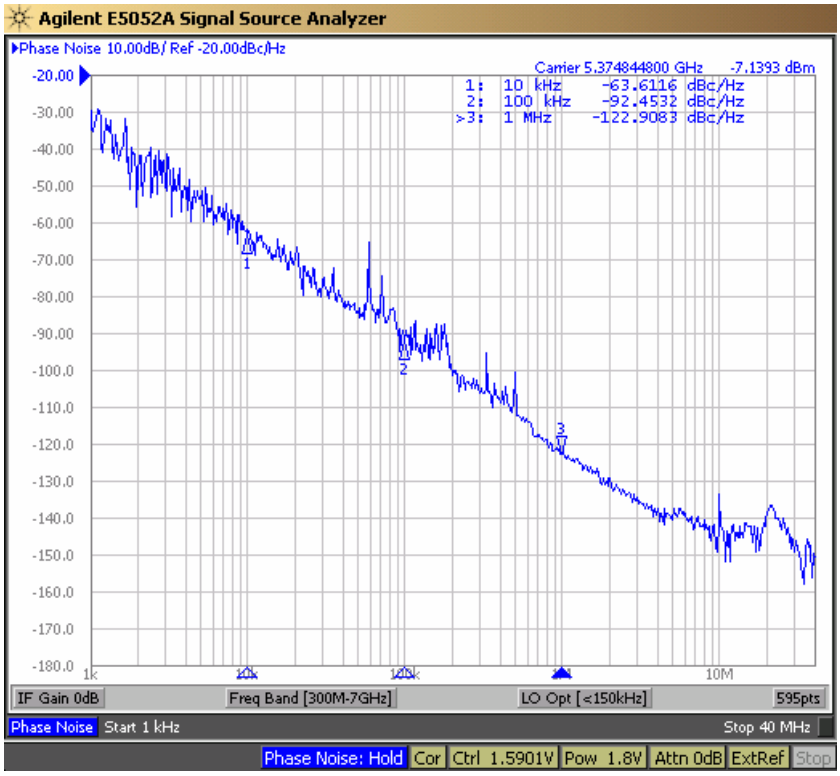


Figure 5-13. Phase noise at the carrier frequency of 5.375GHz under 1.8V supply voltage under test.

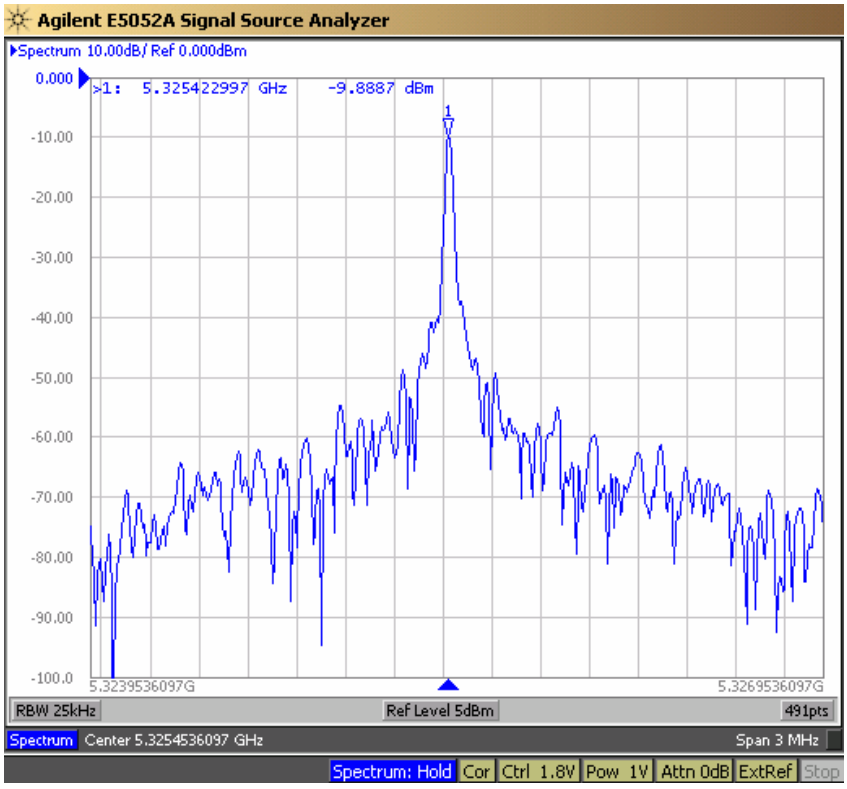


Figure 5-14. Output spectrum at the carrier frequency of 5.325GHz under 1V supply voltage under test.

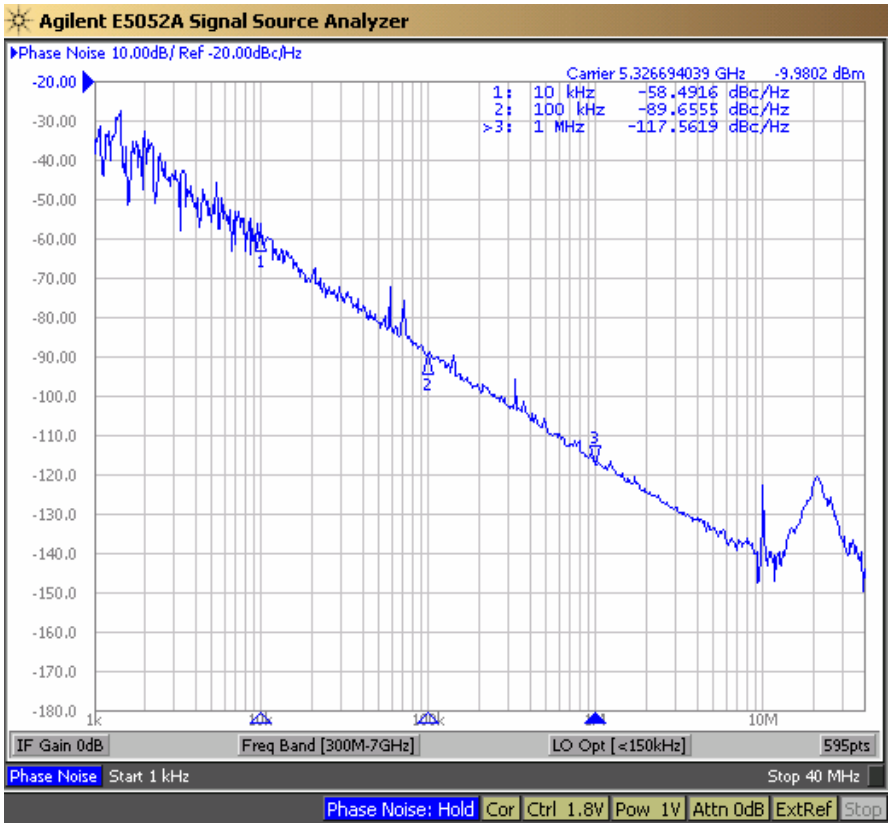


Figure 5-15. Phase noise at the carrier frequency of 5.327GHz under 1V supply voltage under test.

The simulation results and the measured results are summarized in Table 5-2. The measured FOM at 1.8V supply voltage is comparable to the simulated FOM, though the measured FOM at 1V supply is poorer than expected. However, considering 1V is a very low supply voltage for a 0.18µm process, the measured performance at 1V supply is still attractive. The lower oscillation frequency of the measurement than simulation could be caused by the drift of inductance and parasitic capacitance. Generally, the QVCO is functioning as expected under measurement. Future efforts need to address the improvement of low voltage operation.

Seen from Table 5-3, the FOM of the proposed QVCO design is one of the best among the published QVCO designs.

Table 5-2. Performance summary of the proposed BS-QVCO with capacitor tapping.

	Simulation Results	Measurement Results	
Supply voltage (V)	1	1	1.8
Core current consumption (mA)	4.95	10	10
Oscillation frequency (GHz)	5.95-6.13	5.21-5.33	5.27-5.40
Phase noise @ 1MHz offset (dBc/Hz)	-120.3 (6.13GHz)	-117.6 (5.33GHz)	-122.9 (5.37GHz)
Output power (dBm)	-8.9	-9.98	-7.14
FOM (dBc/Hz)	-189	-182	-185

Table 5-3. Performance comparison between the proposed BS-QVCO and the published QVCO designs.

Ref. No.	Technology	VDD (V)	Current (mA)	Operating Frequency (GHz)	Phase noise (dBc/Hz)	FOM (dBc/Hz)
[20] Parallel coupling with phase shifters	0.25µm CMOS	2	15	1.36-1.69	-133.5@600kHz	-187 (measured)
[21] Top-series	0.35µm CMOS	2	25	1.64-1.97	-140@3MHz	-179 (measured)
[22] Bottom-series	0.18µm CMOS	1.8	5.8	5.5-6.71	-115@1MHz (5.5GHz)	-182 (measured)
[23] Bottom-series	0.35µm CMOS	1.3	16	1.91-2.27	-140@3MHz	-184 (measured)
This Work BSQVCO with tap C	**0.18µm CMOS**	**1.8**	**10**	**5.27-5.40**	**-122.9@1MHz (5.37GHz)**	**-185 (measured)**

CHAPTER 6 DESIGN OF A LOW-PHASE-NOISE QVCO WITH BODY COUPLING AND CAPACITOR TAPPING

6.1. Introduction

For all the QVCO coupling methods that we have discussed, there is a pair of coupling FETs required in addition to the cross-coupled switching pair. So there are eight transistors in the QVCO not including the current sources and buffers. As a known fact, the more transistors there are, the more noise that can be generated. Thus, a new coupling method which does not need

additional coupling transistors was proposed, which is the body-coupling method [24]. No additional coupling FETs are necessary in this method, but the bodies of the cross-coupled FETs are used as the coupling gates. Obviously, the body-coupling method saves power and avoids the noise contribution from additional coupling FETs. Though the drain current is partially tuned by the body biasing, it is just a small portion compared to the portion controlled by the gate biasing because g_{mb} is much smaller than g_m. Thus, the RPS caused by the body coupling is still small.

6.2. Proposed Architecture and Design Implementation

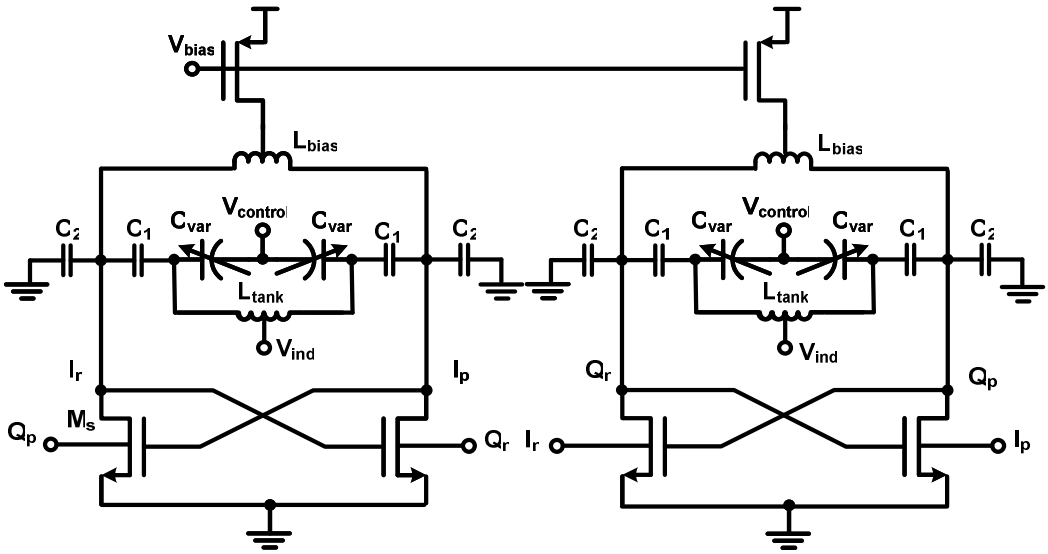


Figure 6-1. Proposed body-coupled LC QVCO with capacitor tapping technique.

The proposed QVCO in this section is a topology of body-coupled LC QVCO with capacitor tapping as shown in Figure 6-1. This QVCO still has a PMOS current sources and NMOS transconductance FETs. The design was implemented in TSMC 0.18μm CMOS process which is a triple-well process, thus the P-type bodies of the NMOS switching FETs are implemented in deep-NWELLs and isolated from the P-substrate. The parasitic capacitance of the P-body to deep-NWELL diodes, as modeled in Figure 6-2, contributes to the tank capacitance.

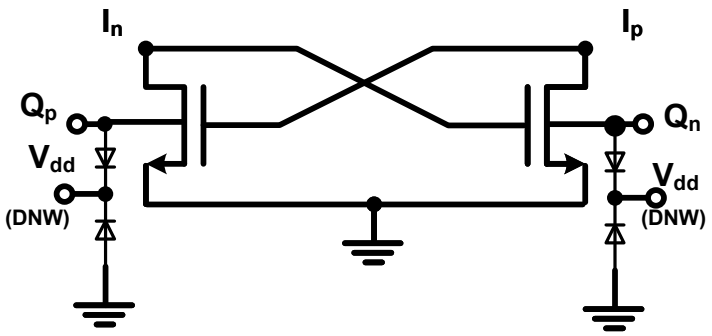
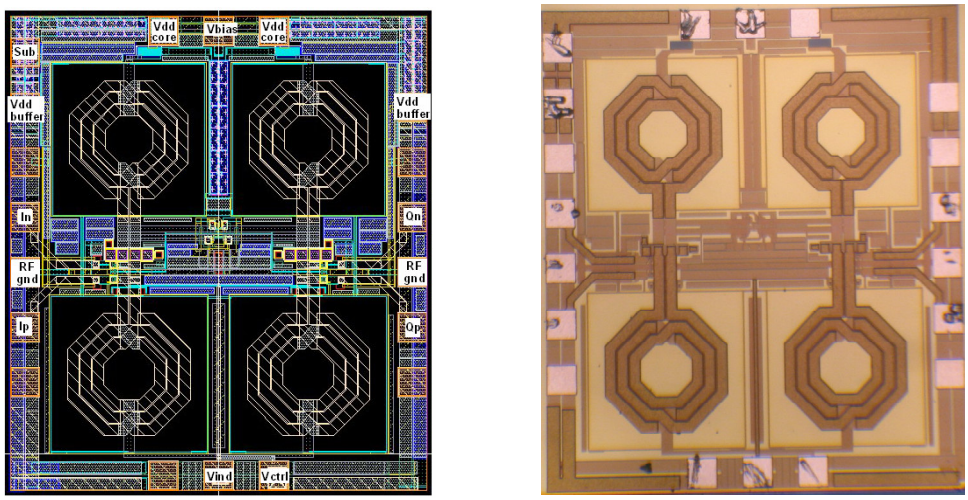


Figure 6-2. Schematic of the P-body to deep NWELL diode and deep NWELL to P-substrate diode.

Figure 6-3 shows the layout and the chip photo of the proposed QVCO implemented in TSMC 0.18µm RF CMOS process. The resonator consists of a center-tapped differential octagonal spiral inductor and a pair of accumulation-mode MOS varactors. The resonator



(a) **(b)**

Figure 6-3. (a) Layout of the proposed Body QVCO. (b) Chip photo of the proposed Body QVCO.

inductor has an inductance of 2.07nH and a *Q* of 14 at 6GHz. The bias inductor at the drain of current source is sized to 1.94nH with a *Q* of 14 at 6GHz. Surrounding the inductors, there are guard rings connected to ground for substrate noise suppression. Precision of the tapping ratio is important so MIM capacitors are used as the tapping capacitors. C_1 is 560fF and C_2 is 400fF. The divide ratio is about 1.7 including the parasitic capacitance. The final size of the QVCO die is

1300µm by 1200µm.

6.3. Simulation and Measurement Results

6.3.1. Simulation Results

Figure 6-4 shows the simulated phase noise performance of the proposed QVCO at the carrier frequency of 6GHz under 1V power supply and 5mA bias current. The phase noise at 100kHz offset and 1MHz offset are -100.1dBc/Hz and -120.8dBc/Hz respectively. Thus, the simulated FOM of this proposed QVCO is -189dBc/Hz at 1MHz offset.

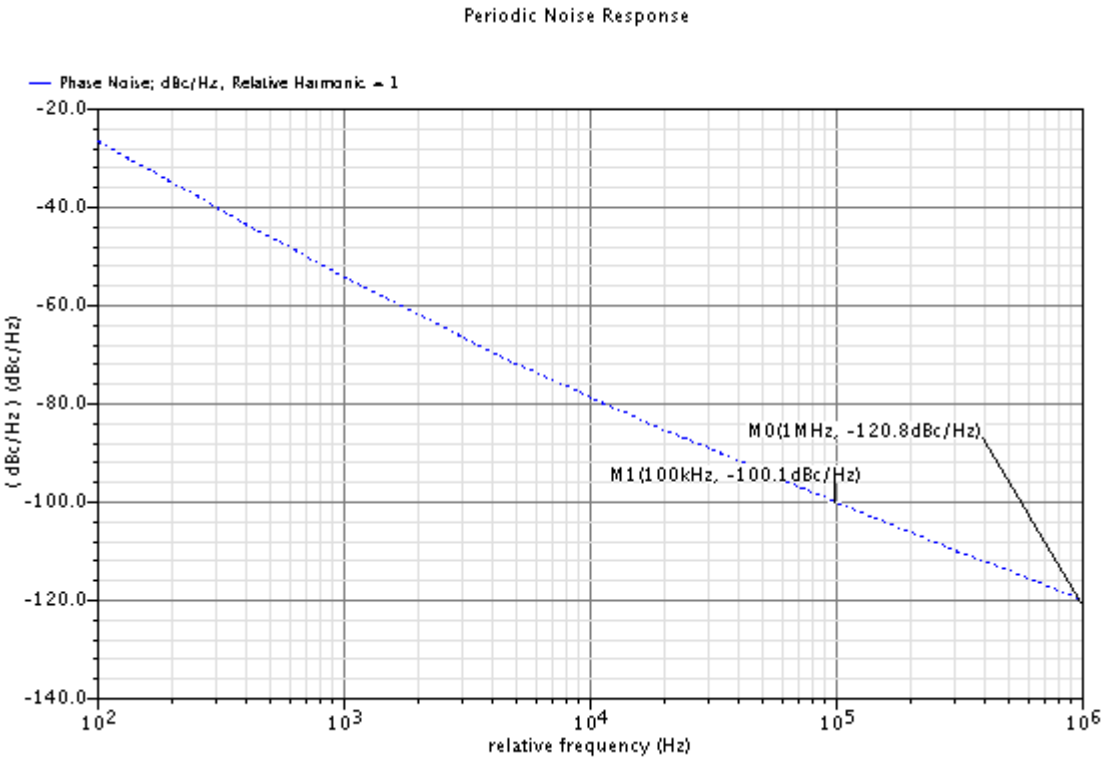
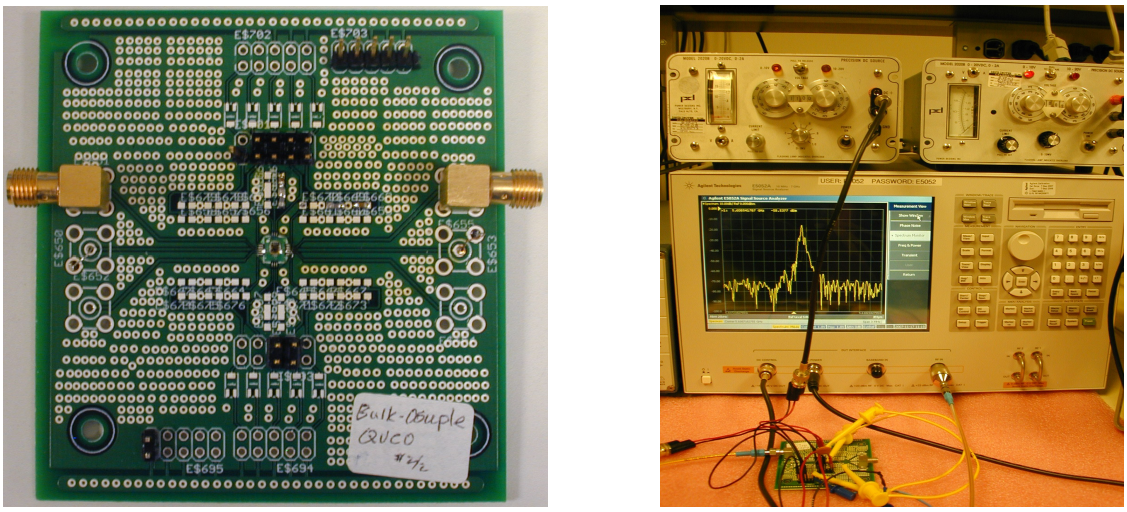


Figure 6-4. Simulated phase noise of the proposed BS-QVCO.

6.3.2. Measurement Results

The VCO chip is wire-bonded to a PCB board for characterization. Figure 6-5 (a) shows the photo of the board and Figure 6-5 (b) shows the measurement setup. The measurement setup is the same as the one for the VCO test in Chapter 4.



(a) (b)

Figure 6-5. (a) PCB board with the proposed body-coupled QVCO chip. (b) Measurement setup.

Figure 6-6 and Figure 6-7 show the measured QVCO performance at 1.8V supply show the measured QVCO performance at 1.8V supply voltage. Figure 6-6 shows the output spectrum at the carrier frequency of 5.61GHz. As shown in Figure 6-7, the QVCO achieves phase noise of -118.2dBc/Hz at 1MHz offset, -77.6dBc/Hz at 100kHz offset and -64.2dBc/Hz at 10kHz offset from the carrier frequency of 5.61GHz with an output power of -15dBm. The DC core bias current is 10mA. The measured FOM of QVCO is -181dBc/Hz at 1MHz offset.

Seen from Figure 6-6, the sideband signal at around 100kHz offset is large so that it causes the spur at around 100kHz in the phase noise plot. This low frequency noise could be generated from the test environment or from the design itself and be up-converted to the carrier frequency. Further investigation will be made for this issue.

Another problem is the measured output power level has a relatively large drop from the simulated value. At 1.8V supply, the largest measured output signal power is -14.9dBm while

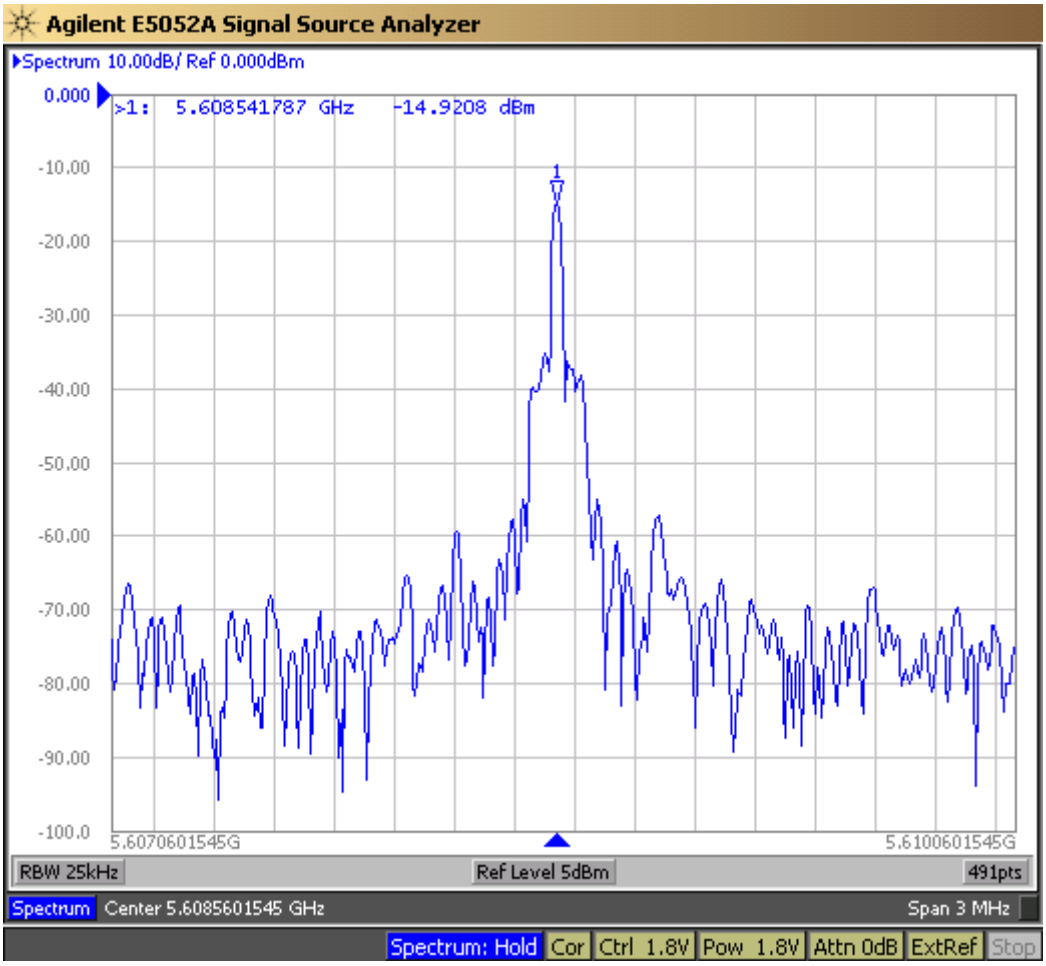


Figure 6-6. Output spectrum at the carrier frequency of 5.61GHz under 1.8V supply voltage under test.

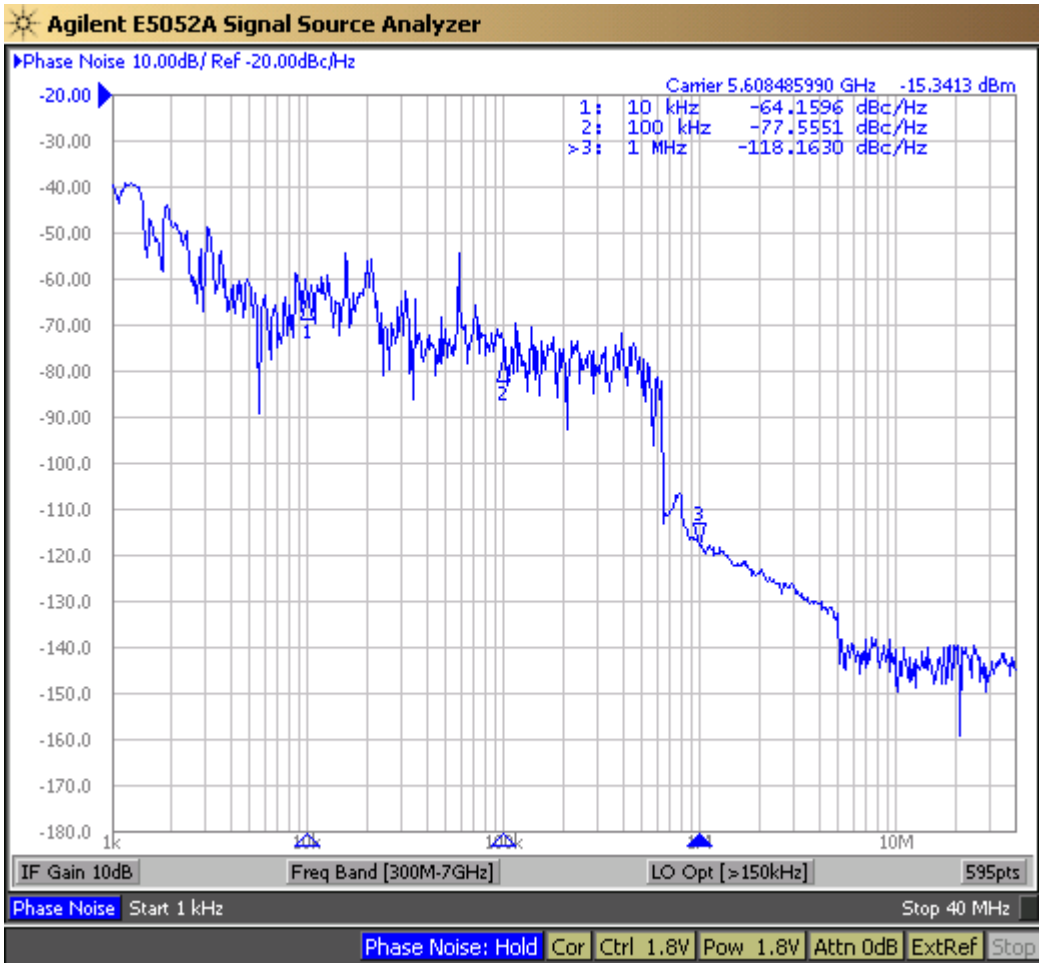


Figure 6-7. Phase noise at the carrier frequency of 5.61GHz under 1.8V supply voltage under test.

consuming 10mA core current. However, simulation shows an output power of -5.6dBm at 1V supply while consuming 5mA core current. Two reasons may account for this problem. One could be that the output buffer (NMOS common source buffer) does not provide enough gain. The other could be that the loaded Q of the tank is much smaller than expected. It is possible that the equivalent capacitance of C2 in Figure 6-1 is larger than the simulation value due to the capacitance variation in the bulk of the NMOS switching transistors, and causes degradation of the loaded tank Q.

The simulation results and the measured results are summarized in Table 6-1. The comparison between this work and the published results is shown in Table 6-2. The measured

FOM is 8dB worse than the simulated FOM, however, still comparable to the published 5GHz QVCO design. The lower oscillation frequency of the measurement compared to simulation could be caused by the drift of inductance and parasitic capacitance. The possible causes for the lower output power level are analyzed in the previous section. Overall, the QVCO is functional under measurement.

Table 6-1. Performance summary of the proposed BS-QVCO with capacitor tapping.

	Simulation Results	Measurement Results
Supply voltage (V)	1	1.8
Core current consumption (mA)	4.95	10
Oscillation frequency (GHz)	5.95-6.13	5.42-5.61
Phase noise @ 1MHz offset (dBc/Hz)	-120.8 (6.13GHz)	-118.2 (5.61GHz)
Output power (dBm)	-8.9	-14.9
FOM (dBc/Hz)	-189	-181

Table 6-2. Performance comparison between the proposed body-coupled QVCO and the published QVCO designs.

Ref. No.	**Tech.**	**VDD (V)**	**Current (mA)**	**Operating Frequency (GHz)**	**Phase noise (dBc/Hz)**	**FOM (dBc/Hz)**
[20] Parallel coupling	0.25µm CMOS	2	15	1.36-1.69	-133.5 @600kHz	-187 (measured)
[24] Backgate coupling	0.18µm triple-well CMOS	1.25	1.74	1.83-2.02	-124@1MHz	-187 (measured)
[22] Bottom-series	0.18µm CMOS	1.8	5.8	5.5-6.71	-115@1MHz (5.5GHz)	-182 (measured)
Bulk-coupling with tap C (This work)	**0.18µm triple-well CMOS**	**1.8**	**10**	**5.42-5.61**	**-118.2@1MHz (5.61GHz)**	**-181 (measured)**

CHAPTER 7 CONCLUSIONS AND DISCUSSIONS

This thesis is a study for novels designs of low-phase-noise VCOs and QVCOs at 5-6GHz frequency range for wireless communications applications. A capacitor tapping technique is proposed and proved to have the capability of enhancing the loaded quality factor of resonator while maintaining large oscillator output amplitude, both of which lead to low phase noise of LC oscillators. Integrating the capacitor tapping technique to several optimized LC VCO and LC QVCO topologies, three unique VCO and QVCO designs with good phase noise performance have been generated. Though the bottom-series coupling and bulk-coupling methods for QVCOs are not novel ideas from this work, they were recently reported and different from the traditional methods. This work proves their functionality and good integration with the capacitor tapping technique to achieve the best QVCO performance. For the bottom-series coupling method, novel theoretical analysis is developed to explain its good phase noise behavior and closed-form optimization equation for the coupling ratio is provided as a design guide for BS-QVCO, both of which also contribute to the novelty of this thesis work.

Besides the topology innovation, design optimization is addressed in this thesis work. Based on the phase noise mechanism of LC oscillators, the devices in the circuits are carefully selected and designed for phase noise reduction. For example, long-channel PMOS FETs are used for current sources to reduce the flicker noise. Short-channel NMOS FETs are used for switching pairs and coupling pairs to provide large transconductance. High-Q inductors are adopted, as differential inductors with a thick top metal and octagonal shape, and accumulation-mode varactors are chosen because they have been proved to have low power consumption and low phase noise at large offset frequencies from the carrier, like 1MHz. The device sizes are optimized by simulation.

The measurement results show good performance for all the three designs. In a summary, a LC VCO and two LC QVCOs with novel topologies have been designed and shown good FOMs. Those designs provide new insights for the low-phase-noise oscillator design.

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