SPDT SWITCH, ATTENUATOR AND 3-BIT PASSIVE PHASE SHIFTER BASED ON A NOVEL SIGE PIN DIODE

by

ALEX OLEGOVICH MIKUL

A thesis submitted in partial fulfilment of

the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

WASHINGTON STATE UNIVERSITY

School of Electrical Engineering and Computer Science

DECEMBER 2009

To the Faculty of Washington State University:

The members of the Committee appointed to examine the thesis of ALEX O. MIKUL find it satisfactory and recommended that it be accepted.

Deukhyoun Heo, Ph.D., Chair

Partha Pande, Ph.D.

John Ringo, Ph.D.

ACKNOWLEDGEMENT

Research for this thesis work was funded by National Science Foundation Centre for Analogue and Digital Integrated Circuits (CDADIC), a industry-universities consortium headquartered at Washington State University and headed by Dr. John Ringo whose help is greatly acknowledged. I would also like to express my gratitude toward CDADIC principal assistant Alaina McCully who was very helpful navigating the narrow straits of bureaucracy and departmental policies.

My special gratitude goes to Professor Deuk Heo, my advisor, whose support and guidance helped me reach my finish line in my research at Washington State University. I would also like to thank my fellow group members Yu You, Peng Liu, Parag Upadhyaya, Pinping Sun, Siqi Zhou and Jae Jung from ARMAG (Advanced RF and Mixed-Signal Application Group) who provided great collaboration and invaluable assistance in my research and who have lit my routine with humour. In addition, I would like to thank professor George La Rue and professor Mohammed Osman who enriched my knowledge in the field of electrical engineering and whose advises proved very valuable in my research.

Finally, I would like to thank my wife, Mariam, and my parents Oleg and Vira Mikulchenko who were very supportive of me during my research and who always encouraged me to aim higher in everything I do.

SPDT SWITCH, ATTENUATOR AND 3-BIT PASSIVE PHASE SHIFTER BASED ON A NOVEL SIGE PIN DIODE

ABSTRACT

Alex Olegovich Mikul, M.S.
Washington State University
December 2009

Chair: Deukhyoun Heo

This thesis explores the possible uses for a recently developed custom PIN diode SPST switch in SiGe BiCMOS process. The PIN diode utilises an octagonal anode shape for an improved insertion loss while maintaining high isolation and was measured to be advantageous to conventional MOSFET switches at *X* and *Ku* frequency bands.

This work will cover the following implementations of the novel octagonal PIN diode: SPDT switch, 3-bit attenuator and 4-bit passive highly linear phase shifter. The SPDT switch features the series-shunt and series-shunt-shunt diode combination for RX and TX arm, respectively. This combination was chosen for balancing between minimizing the insertion loss and maximizing the isolation. The combination of series-shunt-shunt 25 μm^2 - 50 μm^2 – 50 μm^2 PIN diodes results in an isolation of 53.7 to 45.5 dB and an insertion loss of 0.74 to 1.4 dB over the frequency range of 6 – 18 GHz. Such low insertion loss and high isolation will make this SPDT switch design attractive for beam forming systems that incorporate *X* and *Ku* band transceivers. The PIN diode 3-bit attenuator provides for an accurate attenuation with a resolution of 1 dB over the wide frequency range of 6 – 16 GHz. One bit occupies only 0.069 mm^2 which results in a small overall area. The passive topology provides for an increased P_{1dB} input referred

point. Due to the high integrative ability of a novel PIN diode, this attenuator can be fully implemented on SoC.

A fully integrated highly linear 4-bit phase shifter utilises the hybrid LPF/HPF switched topologies to provide a resolution of 22.5°. The return input/output losses of the entire structure are measured to be 20 dB ± 5 dB, the input-referred IP3 to be 37 dBm, and the phase variation to be ±1.8° over the range of 14.5 – 15.5 GHz. This phase shifter draws an average current of 3.5 mA from the 3.3 V source. The use of differential inductors instead of transmission lines helps minimise the layout area which results in lower cost implementation for SoC beam forming applications.

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

CHAPTER ONE

INTRODUCTION

As the satellite communication systems become more complex and more robust, they are encountered with such challenges as cost and integrative capabilities. Modern satellite communication is done primarily with the use of phased array antennae. A phased array antenna is composed of an array of radiating elements that emit signals with varied relative phases. The resulting radiation pattern of the formed beam is reinforced in a desired direction and suppressed in undesired directions. First phased array transmission was developed by Karl Ferdinand Braun in 1905 who demonstrated the possibility of transmission enhancement in one direction. Figure 1.1 depicts a BMEWS solid-state phased-array radar at Fylindales base of Royal Air Force.

Fig 1.1 BMEWS solid-state phased-array radar at RAF Fylindales [27]

Phased array antennae offer many significant advantages over conventional antennae:

- High gain width loss side lobes
- Ability to generate multiple steered beams from the same aperture
- Ability to allow the beam to instantaneously move from one target to another in a few microseconds
- Arbitrary modes of surveillance
- One faulty element will reduce the beam sharpness but the system will remain operational

The beam steering θ can be expressed in terms of phase shift between two successive elements φ, distance between two successive elements d, and a wavelength λ as follows (1.1):

$$\vartheta = \arcsin(\frac{\varphi \cdot \lambda}{360° \cdot d}) \qquad (1.1)$$

The disadvantages include high cost and very complex structure that consists of processor and phase shifters for each element. However, with the developments in a solid-state device technology, phased-array systems become more compact and more affordable.

Generally, there are two types of phase shifting: IF phase shifting and RF phase shifting. Fig. 1.2 shows the IF phase shifting architecture. The input RF signal is amplified by LNA and then undergoes down-conversion to IF band by mixing with the LO signal. Because the phase shifting and the power combining are performed at a low frequency, the IF phase shifter exhibits lower insertion loss and lower DC power consumption than the RF phase shifter. On the other hand, at low frequencies, the passive lumped components, such as inductors and capacitors, occupy significantly larger chip area than RF phase shifting. At the same time, the frequency mixers are connected to a

low directional antenna and are susceptible to interference from all directions. Also, the generated inter-modulation products can propagate throughout the array and cause further interference [1].

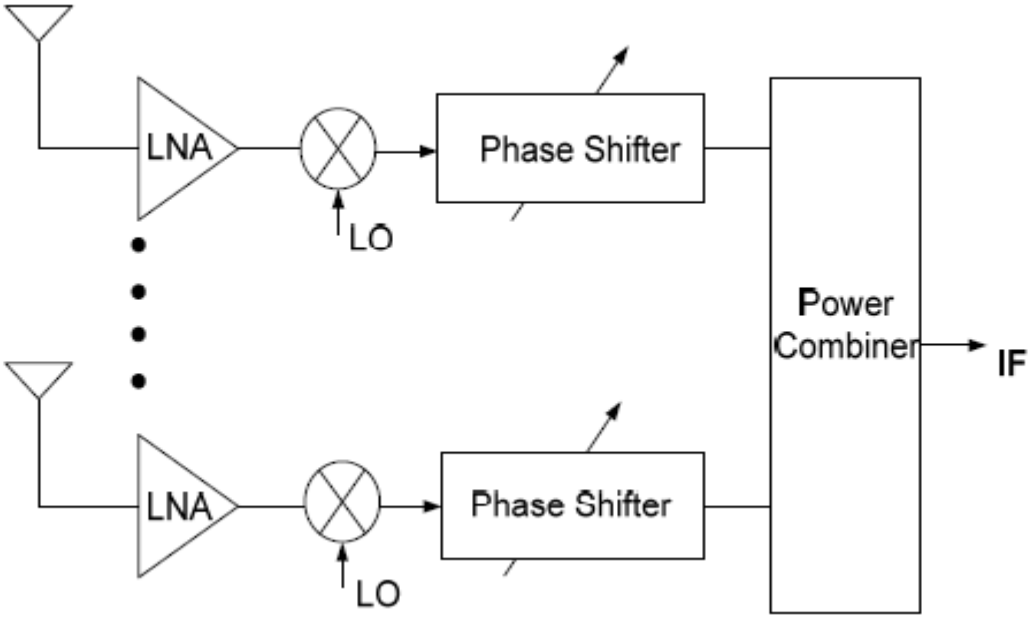


Fig.1.2 IF phase shifting architecture [13]

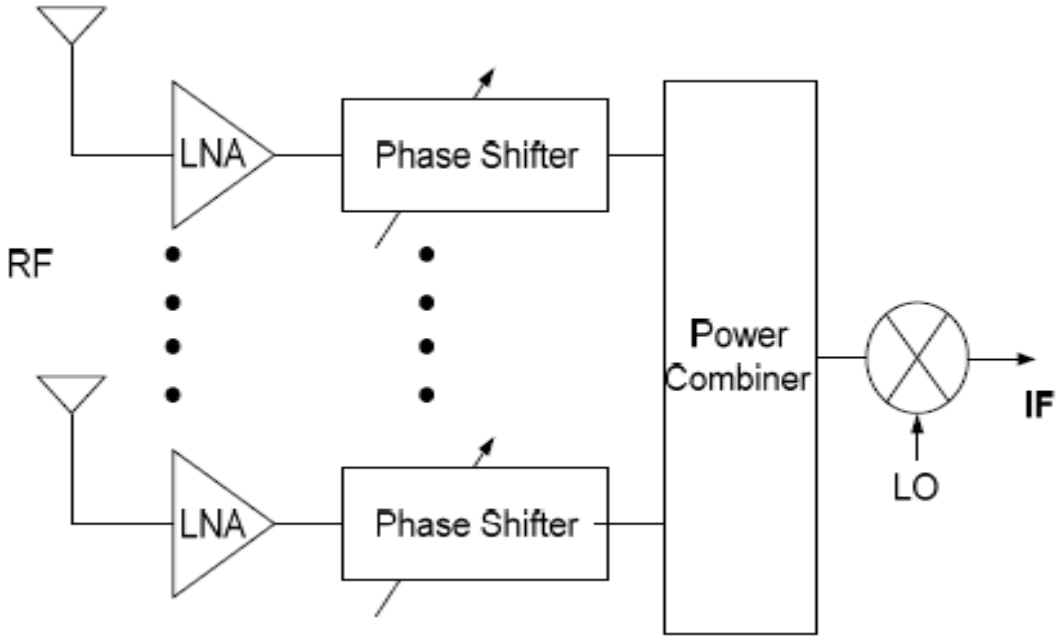


Fig.1.3 RF phase shifting architecture [13]

Phase shifting directly in the RF domain (Fig. 1.3) for each array element is widely employed in today's phased-array communication systems. The combined output RF signal after the RF combiner has high pattern directivity and can substantially reject an undesirable interference before the down-converting mixer. This can improve the system's signal to noise ratio (SNR) compared to the architecture that utilizes IF phase shifting and combining. In case of RF phase shifting, the LO distribution network is removed from the system which results in a simpler system. This dissertation work uses the RF phase shifting architecture for the proposed phase shifter, SPST and SPDT switches [1]–[2].

Due to the fact that each individual component in the array is designed to transmit and receive signal, it utilises a transceiver (T/R) module as the terminating element for each channel. Typically, a T/R module consists of a transmitting path (TX) and receiving path (RX) designed in such a way as to feed the signal to the antenna at the output of the TX channel and feed the signal from the antenna to the input of the Rx channel. Fig 1.4 depicts a possible structure of a T/R module. By itself, such module usually does not occupy a large space and is not costly to implement using the MMIC technology; however, a phased-array antenna may utilise several hundred thousands of such elements. Thus, the size and performance of every sub-block of a T/R module will play a significant role in a final stage of the phased-array assembly.

Two crucial elements in the above diagram are the phase shifter and the single-pole double-throw (SPDT) switch which connects the output/input of the T/R module to

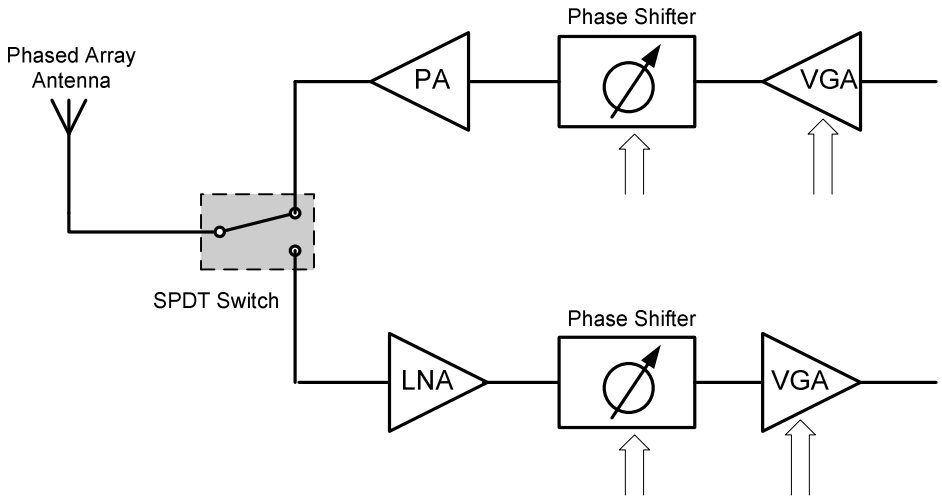


Fig 1.4 Typical structure of a T/R module

the external antenna. It is extremely important to isolate the TX and RX channels in order to prevent the signal leakage from TX channel into the RX channel during the receiving stage due to the high output power following the power amplifier (PA) in TX channel. At the same time, the SPDT switch should have a high linearity in order to accommodate the transmitted signal. Having high linearity and high isolation can be challenging task for the switch design, especially if utilising the CMOS transistors. On the other hand, the phase shifter should be accurate enough to keep the beam sharpness at a high level.

Most high performance transceiver modules used in phased-array telecommunication systems are implemented in GaAs and InP [3]-[4] semiconductor technologies; however, due to low integrative capacity and high cost of these materials, achieving fully integrated System-on-a-Chip (SoC) has been a very challenging task. Recent developments in low-cost high-integrative silicon based technologies became a feasible alternative solution for fully integrated satellite communication systems. Particularly the low-cost SiGe BiCMOS technology is currently becoming one of the leading choices for ever-expanding phased-array radio communication systems.

Utilising SiGe BiCMOS technology has its drawbacks as well. MOSFET-based switches suffer from low isolation, narrow band operational frequencies and poor linearity. Active phase shifters such as the one proposed by Dr. Rebeiz and his group also lack robust power-handling capabilities, although they minimise the DC power consumption. Recently, the ARMAG group at WSU department of electrical and electronic engineering have developed a novel PIN diode in 0.18-µm SiGe BiCMOS technology [5]. By making this diode forward biased or reverse biased, it can act as the low insertion loss high isolation highly linear SPST switch. Before, the implementation of PIN diodes was mostly done in III-V compound semiconductor technologies (i.e., GaAs and InP) which prevented it from being integrated into low-cost silicon-based technology. However, as the new PIN diode is developed in SiGe technology, it can be fully integrated into passive circuits such as SPDT switch and hybrid high-pass/low-pass phase shifter. Whilst the implementation of this PIN diode will raise the power consumption, it will improve the insertion loss, isolation and power-handling capabilities.

A. Organisation

The principles of operation of a proposed novel PIN diode as well as the effect of its geometry on the performance will be discussed in chapter 2. Chapter 3 will present an improved design of an asymmetrical PIN diode based SPDT switch, and Chapter 4 will cover the design of a passive phase shifter based on hybrid low-pass high-pass filter topology that utilises PIN diode SPST switch to shift between reference and phase delay paths. Chapter 5 will propose the future direction in the discussed topics and the possible improvement of an existing design.

CHAPTER TWO

NOVEL HIGH ISOLATION LOW INSERTION LOSS SIGE BASED PIN DIODE

A. Introduction

With the explosive growth in satellite and mobile communication markets, low cost and reconfigurable phase array communication systems have received remarkable attention. The ability to fully integrate System-on-a-Chip (SoC) and operate over a wide bandwidth is the key to the realization of wideband or multi-band satellite communication systems. Recently, silicon based technologies have become a low cost alternative solution to III-V compound semiconductor technologies, such as *GaAs* or *InP* [3]. For space applications, the radiation-tolerant and the low cost *SiGe* BiCMOS technology has emerged as technology of choice for the fast-growing phase array communication systems [4], [6].

For the T/R module in satellite communication applications, high performance switching devices are critical components for successful system integration. Geometric and process optimization has been studied to improve PIN diode insertion loss and isolation [6], [7].

This chapter presents an in-depth comparison between conventional MOSFET switch and a novel SiGe BiCMOS PIN diode. A new theoretical analysis and practical verification of PIN diode performance based on measurement, employed to enhance the performance of the PIN diode switch for microwave applications, are also presented. The reasoning behind implementation of PIN diode for use in state-of-the-art MMIC satellite communication systems is presented in terms of overall S-parameter performance, power

handling capabilities, power consumption and the level of integration in silicon-based technologies.

B. Performance characteristics of an RF switch

Telecommunication satellite systems that utilise the phased-array antennae operate at radio frequencies (RF) that range from 3 GHz to 30 GHz, but the most common frequency band for satellite communications is Ku band. According to the IEEE standard 521-2002, Ku band ranges from 12 to 18 GHz. At such frequencies, the wavelength is only around 2 cm, so the size of the chip components plays a bigger role in the overall performance of the system.

At Ku band, the performance of the switch will be evaluated using three important criteria: return loss and insertion loss for “ON” state and “OFF” state. The latter is referred to as isolation in this thesis. Considering the short wavelength of a signal, it is impossible to ignore the effect of interconnections in a circuit. Thus, the electric circuit should be modelled as the collection of transmission lines of finite lengths connecting numerous active and passive devices. Equations that describe the travelling wave in a transmission line are as follows (2.1 and 2.2) [8]:

$$V(z) = V^{+}e^{-kz} - V^{-}e^{kz} \tag{2.1}$$

$$I(z) = I^{+}e^{-kz} + I^{-}e^{kz} \tag{2.2}$$

where z is the axis of propagation, V^{+} and I^{+} are voltage and current waveforms propagating in positive z direction, V^{-} and I^{-} are the waveforms propagating in negative z direction, and k is the propagation constant for the given media.

At such high frequencies, the propagating wave will experience reflection if the

source impedance is not matched with the load impedance. Since the impedance of lumped elements such as inductor and capacitor varies with the frequency, and the operating frequency does not remain constant, it is not possible to achieve a perfect match between two circuit components. This will result in a travelling wave being partially reflected from the load back to the direction of the source. The reflection coefficient is defined as a ratio of reflected wave V^+ to incident wave V^- (2.3) [8].

$$\Gamma = \frac{V^-}{V^+} \tag{2.3}$$

The reflection of the wave will result in the reflected power P_{in}^- whose ratio to incident power P_{in}^+ will be equal to $|\Gamma|^2$. The return loss (RL) describes how much power is reflected from the load and thus is defined in terms of reflected and incident power (2.4). The return loss has the value of 0 when the wave encounters open circuit condition and is fully reflected. It would reach its maximum value of ∞ if the wave was fully transmitted [8].

$$RL = -10 \cdot \log(\frac{P_{in}^-}{P_{in}^+}) = -10 \cdot \log\left|\Gamma\right|^2 = -20 \cdot \log\left|\Gamma\right| \tag{2.4}$$

The transmitted power is the difference of incident power and reflected power, i.e., $P_t = P_{in}^+ - P_{in}^-$. The insertion loss (IL) defines the amount of transmitted power with respect to the incidental power. For passive circuits, the insertion loss (IL) can never be less than 0 because it indicates perfect matching. The insertion loss is defined as follows [8]:

$$IL = -10 \cdot \log(\frac{P_t}{P_{in}^+}) = -10 \cdot \log(\frac{P_{in}^+ - P_{in}^-}{P_{in}^+}) = -10 \cdot \log(1 - \left|\Gamma\right|^2) \tag{2.5}$$

In this work, the term *insertion loss* will be used to refer to the insertion loss when

the switch is turned on whilst the term *isolation* will be used to refer to the insertion loss of the switch which is turned off.

C. PIN and PN diodes comparison

A conventional PN diode is formed by joining P-type and N-type semiconductor materials together. Although PN diode enjoys many uses, it is most commonly used as a rectifier. Depending on the biasing conditions, the PN diode may be in one of the three regions of operations: forward, reverse and breakdown (fig 2.1). When forward biased, the diode will start conducting current when the forward voltage reaches the value $v_{d.}$ When reverse voltage is applied, the diode will have a very small amount of reverse saturation voltage. If the reverse voltage is increased past v_{br}, the diode will enter the breakdown region that is likely to destroy the PN junction [9].

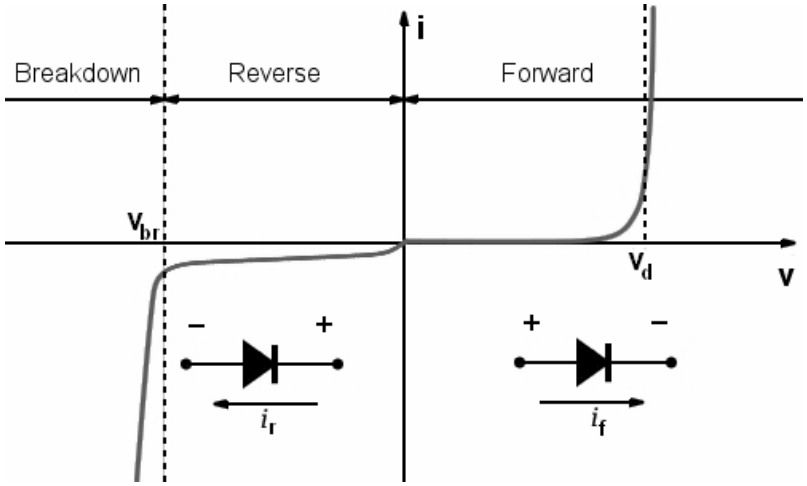


Fig. 2.1 IV curve of a conventional PN diode

Unlike PN diode, PIN diode consists of P-type, N-type and wide intrinsic semiconductor regions. The intrinsic region is situated between N-type and P-type materials. PIN diode is inferior in its rectifying properties, but it can serve as a high-

performance RF switch. The intrinsic region is filled with electrons and holes from N-type and P-type semiconductor regions, and under equilibrium condition, their number is equal. When the PIN diode becomes forward biased, the amount of injected carriers increases to a number that is several order of magnitude higher than the amount of intrinsic carriers. Thus, the intrinsic region serves as charge storage during the forward bias operation. At high frequencies, the PIN diode displays behaviour similar to that of a perfect resistor wherein resistance is inversely proportional to the DC bias current through the diode. This makes the PIN diode to display very linear behaviour even for large signals. At the same time, wide intrinsic region significantly reduces the PN junction capacitance that is formed when the diode is reversely biased which results in an improved isolation compared to a PN diode [10].

D. SiGe Based PIN Diode Structure

Due to its structure, most PIN diodes were fabricated in GaAs or InP processes; however, several students from ARMAG group, notably Le Wang and Piping Sun, were able to fabricate PIN diode in BiCMOS SiGe technology by using HBT layers. In a standard SiGe 0.18-μm BiCMOS process, PIN RF switches are realized with HBT material layers: the $P+$ base layer, *N-epi* collector layer, and buried $N+$ subcollector layer, as shown in Fig. 2.2.

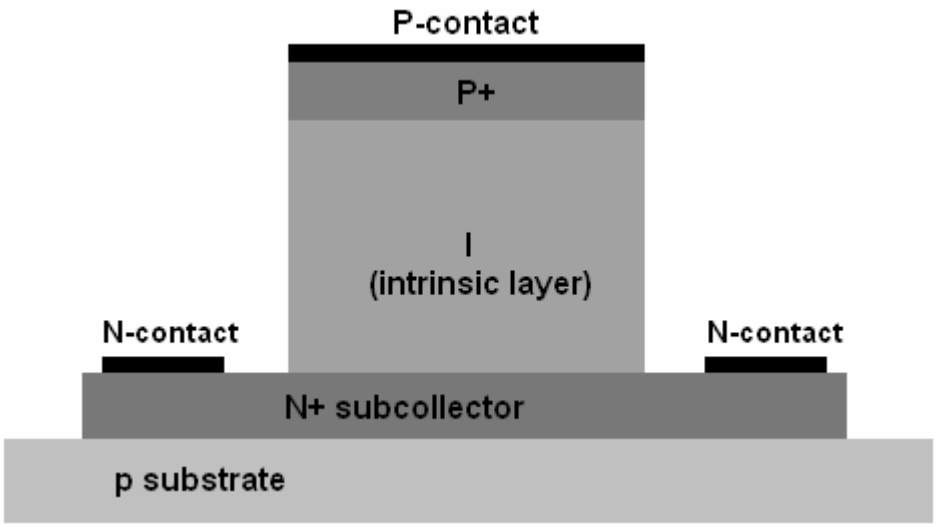


Fig 2.2. Ideal Vertical PIN diode cross-sectional view

The equivalent-circuit model from the physical geometry of the PIN RF switch is described in Fig. 2.3 [11]. C_I and C_O are the capacitances between anode and ground, and between cathode and ground, respectively. C_P is the parasitic capacitance between the anode and cathode contacts. R_C is the contact resistance, which consists of the anode contact resistance R_{CA} and the cathode contact resistance R_{CC}. R_N is the resistance from the un-etched *N-epi* layer. R_I is the variable resistance that is inversely proportional to DC bias current, C_J is the variable junction capacitance that too depends on the amount of injected carriers in the intrinsic region. R_S is the parasitic resistance in the p-substrate material. As it is clear from the figure 2.3, N+ subcollector and p-substrate form a parasitic *Psub-Nwell* diode in which N+ subcollector is cathode and p-substrate is anode. C_{PD} is the variable capacitance of this parasitic *Psub-Nwell* diode that varies with the width of the depletion region depending on the bias voltage.

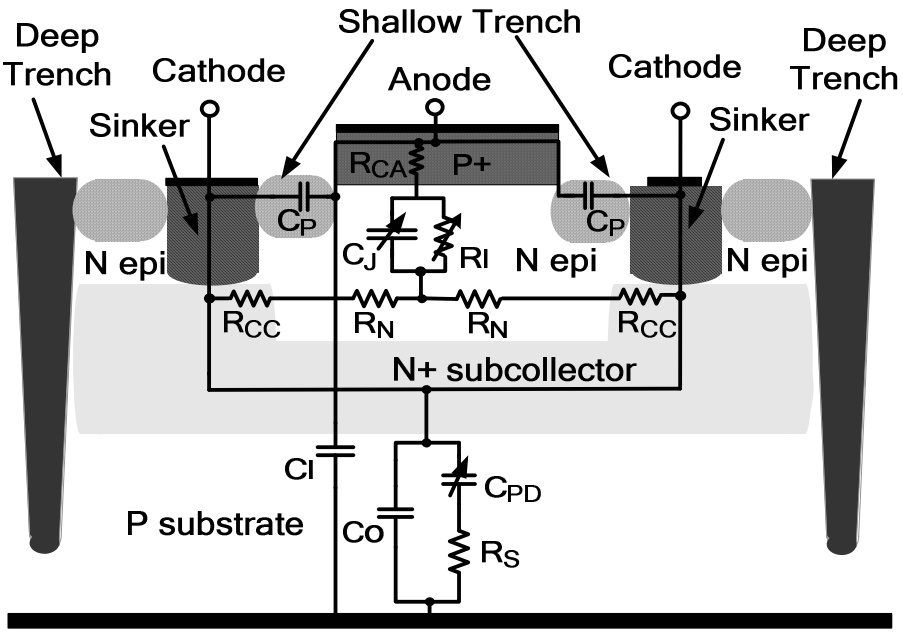


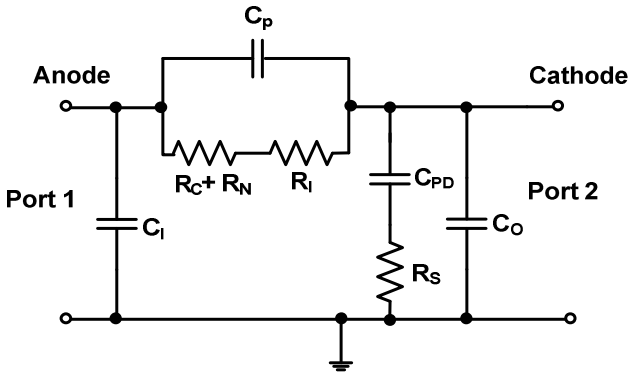
Fig. 2.3. PIN diode cross-sectional view in a standard SiGe process [11].

For the PIN RF switch, the crucial performance criteria are the forward bias insertion loss and the reverse bias isolation. Fig. 2.4 (a) and (b) show the small signal equivalent circuit models of the PIN RF switch based on the *S*-parameter computation.

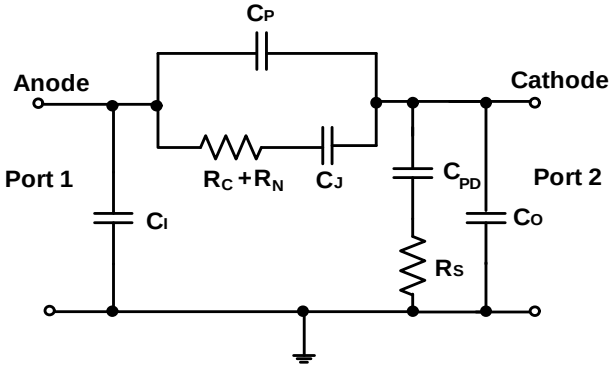
In the forward bias condition, the current-dependent resistance R_I from the intrinsic region is represented by (2.6).

$$R_I = \frac{w_0 w}{2\mu\tau_0 J_0^{1/3} A^{1/3} I_{dc}^{2/3}} \tag{2.6}$$

where, τ_0 is the effective minority carrier lifetime for a given intrinsic layer width w_0, and current density J_0, w is the width of the intrinsic layer, A is the device's anode area, μ is the average electron and hole mobility , and I_{dc} is the forward bias current [6].



(a)



(b)

Fig. 2.4. Small signal equivalent circuit models for PIN RF switch (a) Equivalent circuits for "on" state (b) for "off" state [11].

From fig. 2.4 (a) and (b), it is possible to derive an analytical expression for S-parameters, particularly for the insertion loss S_{21} and isolation S_{12} as follows [11]:

$$S_{21} = \frac{Z_0 \| \frac{1}{sC_o} \| \left(\frac{1}{sC_{PD}} + R_S \right)}{\frac{1}{sC_P} \| (R_C + R_N + R_I) + Z_0 \| \frac{1}{sC_o} \| \left(\frac{1}{sC_{PD}} + R_S \right)} \approx \frac{Z_0 \| \frac{1}{sC_o} \| \left(\frac{1}{sC_{PD}} + R_S \right)}{(R_C + R_N + R_I) + Z_0 \| \frac{1}{sC_o} \| \left(\frac{1}{sC_{PD}} + R_S \right)} \quad (2.7)$$

where, Z_0 is the characteristic impedance and $\left|\frac{1}{sC_P}\right| \geq \left|R_C + R_N + R_I\right|$, and

$$S_{12} = \frac{Z_0 \parallel \frac{1}{sC_I}}{Z_0 \parallel \frac{1}{sC_I} + \left((R_C + R_N) + \frac{1}{sC_J} \right) \parallel \frac{1}{sC_P}} \approx \frac{Z_0 \parallel \frac{1}{sC_I}}{Z_0 \parallel \frac{1}{sC_I} + \frac{1}{sC_J} \parallel \frac{1}{sC_P}} \tag{2.8}$$

where we assume that $\left|\frac{1}{sC_J}\right| \geq \left|R_C + R_N\right|$.

The forward bias current I_{dc} consists of recombination, I_{rec}, and diffusion, I_{diff}, currents [7]. I_{diff} is 10^{19} times smaller than the I_{rec}, and thus is not considered in the calculation. I_{rec} is the sum of bulk recombination current, which is proportional to the diode area, A, and the surface recombination current which is proportional to the perimeter length, P. Since the major recombination occurs at the perimeter and not the bulk, the bulk recombination current is omitted in (2).

$$I_{rec} \approx \left(\frac{qWv_{th}\sigma N_t n_i}{2} A + q\, s_p L_s n_i P\right) \exp\left(\frac{qV}{2KT}\right) \approx \left(q\, s_p L_s n_i P\right) \exp\left(\frac{qV}{2KT}\right) \tag{2.9}$$

where, v_{th} is the thermal velocity of the carriers, N_t is the trap concentration, σ is the capture cross section of the deep trap, W is the effective depletion width where the carrier recombination is significant, n_i is the intrinsic carrier concentration, s_p is the surface (perimeter) recombination velocity and L_s is the surface diffusion length.

Since $1/\tau_0 \approx v_{perim}(P/A)$ and v_{perim} is the effective surface recombination velocity, by employing equations of τ_0 and (2) in (1), we can obtain [11]:

$$R_I = \frac{w_0 w v_{perim}}{2\mu J_0^{1/3}\left[q s_p L_s \eta_i \exp\left(\frac{qV}{2KT}\right)\right]^{2/3}} \times \frac{1}{A}\left(\frac{P}{A}\right)^{1/3} \tag{2.10}$$

Eq. (3) shows that R_I is inversely proportional to the device's area. By minimizing the anode's *P/A* ratio, the current dependent resistance can be reduced and forward bias insertion loss is improved.

E. PIN and MOSFET RF switch

MOSFET (metal-oxode-semiconductor field-effect transistor) can also be used as an RF switch. A typical MOSFET (Fig 2.5) consists of poly gate, N+ type drain and source (P+ for PMOS), and p-substrate used as a body of the transistor (N-well for PMOS). The gate electrode is located above the body and between the drain and the source, and is insulated from the body by a dielectric layer. In NMOS, when a voltage is applied to the gate, the body underneath the gate dielectric will form an inversion layer (also called n-channel) which will become the electron path from source to drain. The principle of operation of PMOS transistor is similar, except that the N-well material underneath the gate dielectric will form a p-channel path that would conduct the holes between the drain and the source. P-substrate and N-well can be biased in a certain way to change the threshold voltage, which would, in turn, change the transconductance in a desired way.

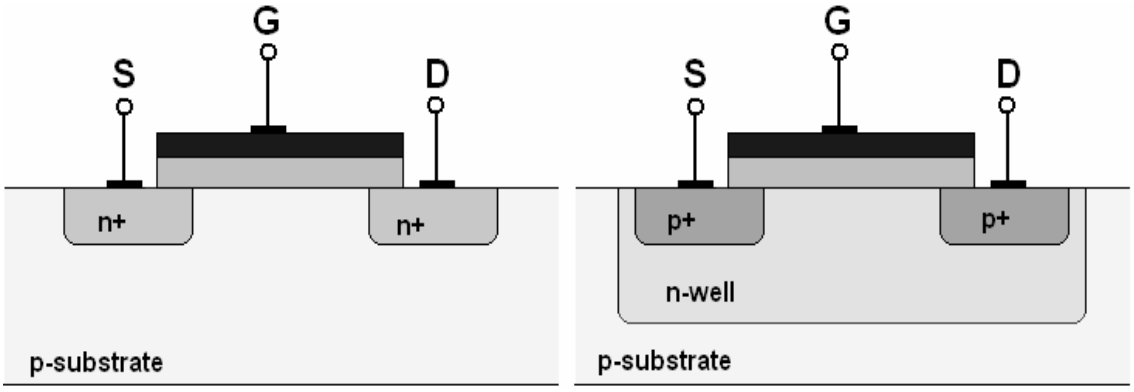


Fig. 2.5. Cross-section view of NMOS transistor (left) and PMOS transistor (right).

The resistance of the formed n- or p-channel in the "ON" state for the transistor is described as follows [12]:

$$R_S = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_T)} \tag{2.11}$$

where μ is the electron or hole mobility, C_{ox} is the gate dielectric capacitance, W/L is the ratio of channel width to channel length, V_{GS} is the voltage difference between gate and source, and V_t is the threshold voltage.

The junctions between different semiconductor materials create parasitic capacitances which will affect the performance of the MOSFET RF switch. Fig. 2.6 depicts the MOSFET in "OFF" state with parasitic capacitances between different terminals.

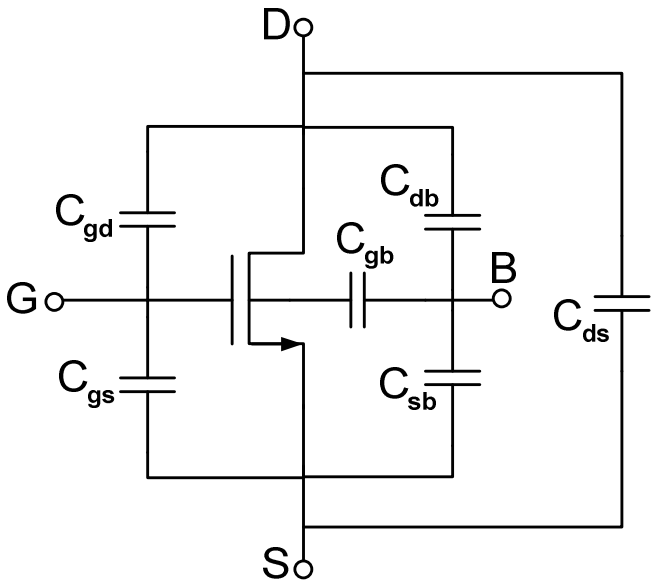


Fig. 2.6. NMOS transistor with parasitic capacitances in “OFF” state

The corresponding C_{OFF} capacitance can be found by combining parasitic capacitances from fig. 2.7 to achieve the following expression:

$$C_{OFF} = C_{ds} + \frac{C_{sb}C_{db}}{C_{sb} + C_{db}} + \frac{C_{gd}C_{gs}}{C_{gd} + C_{gs}} \tag{2.12}$$

When a MOSFET is used as the switch, the channel resistance in “ON” mode and the combined capacitance in the “OFF” mode will determine the switch performance related to the on-state power handling capability and off-state isolation, respectively. In terms of linearity, insertion loss and isolation, a novel PIN diode designed and fabricated by ARMAG group shows improved performance while enjoying the same level of integrative ability as the MOSFET device in SiGe process.

CHAPTER THREE

HIGH ISOLATION LOW INSERTION LOSS PIN DIODE BASED SPDT SWITCH DESIGN

A. Introduction

Modern communication systems utilise thousands of components in their phased-array antennae. Each component is able to transmit and receive radio signals; therefore, it works as the transceiver. In each transceiver, the transmitting path and the receiving path utilise the same antenna in order to minimise the area. Most commonly, such antenna is connected to the transceiver via a single-pole double-throw switch (SPDT), so the performance of each individual switch is crucial to the overall performance of the entire phased-array communication system.

As depicted in fig. 1.4, the transmitter generally uses a power amplifier (PA) for the final amplification of the signal before it is fed to the antenna. On the other hand, the signal that is fed to the receiver from antenna is generally attenuated due to the distance it travels from the source. Thus, the LNA is typically used at the input of the receiver to amplify the incoming signal while keeping the noise figure low. Ideal SPDT switch would completely separate transmitter from the receiver preventing any leakage between them. While reducing the insertion loss between the receiver/transmitter and the antenna is beneficial, the most crucial characteristic of the switch is the isolation between transmitter and receiver when the transceiver operates in the receiving mode. Since the transmitted signal has a large power, even a small leakage into the receiving channel will cause a significant interference with the received signal.

Due to the fact that most PIN diodes used to be fabricated in InP or GaAs, their integrative ability was insufficient to be used in system-on-a-chip (SoC) [3],[4]. Such implementation would be costly and would result in a greater chip area. This was the reason for the popularity of inexpensive and highly integrative MOSFET switches that were widely used as building blocks for SPDT switches. However, MOSFET switches developed in a standard CMOS process suffer from substrate parasitic capacitances, low breakdown voltage and low mobility. One of the biggest drawbacks of the MOSFET switches is the existence of parasitic junction diodes that would leak the negative voltage swing.

This chapter will discuss the previous PIN diode based design of a symmetrical SPDT switch proposed by an ARMAG member Pinping Sun [13] and will propose the improved version of a symmetrical as well as asymmetrical SPDT switch.

B. Conventional symmetrical PIN diode based SPDT switch design

Conventional symmetrical SPDT switch design consists of one series and one shunt PIN diode SPST switch for each arm of the transceiver (Fig. 3.1). The through path between RF IN and RF OUT1 is activated by turning on series diode D1 and turning off shunt diode D2. This is achieved by applying a DC bias voltage of 0V at the RF IN terminal and a negative bias voltage at the RF OUT1 terminal. The isolation path between RF IN and RF OUT2 exists when the series diode is reverse biased and the shunt diode is forward biased by applying bias voltage of 0V at RF IN and a positive bias voltage at RF OUT2. This topology would provide the same degree of isolation between RF OUT1 and RF OUT2 arms.

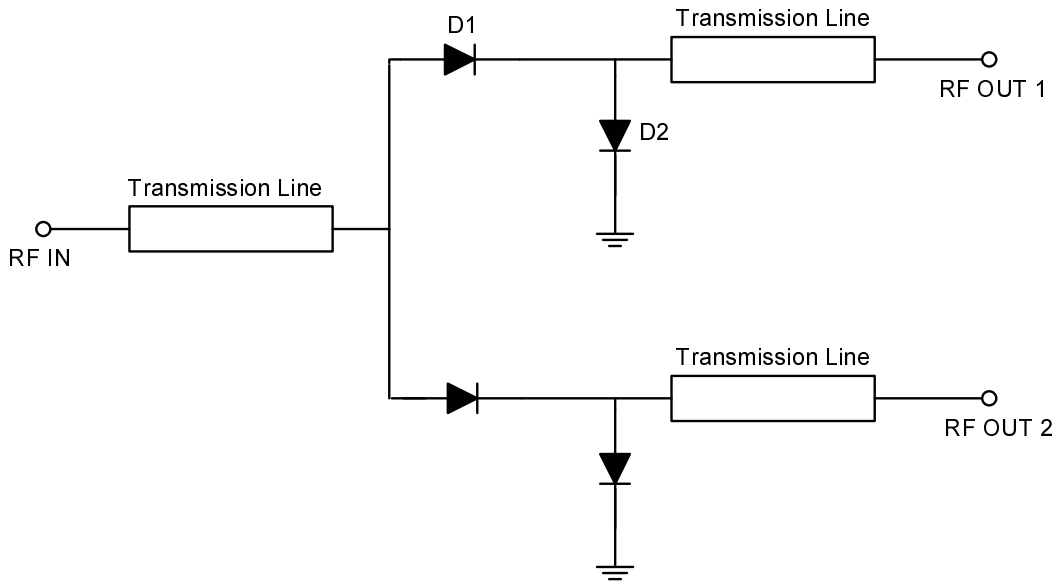


Fig. 3.1. Conventional design topology of an SPDT PIN diode switch

The main application of SPDT switch as discussed in this work is to be used in a transceiver; thus we can virtually assign the port RF IN to be the input/output of the antenna while RF OUT1 and RF OUT2 will be the output of the receiver and the input of the transmitter, respectively.

C. Degradation effect of a parasitic Psub-Nwell diode

PIN diode includes a parasitic PN diode formed by the N+ subcollector and p-substrate layers as depicted in fig. 2.3. The diode can be turned on if N+ subcollector is negatively biased compared to p-substrate. In a schematic view, it can be presented as a shunt PN junction diode whose anode is connected to ground (since p-substrate is connected to ground) and whose cathode shares the same terminal with the series PIN diode's cathode (fig. 3.2.). The shunt diode D2 also includes the parasitic Psub-Nwell diode, but it remains turned off at all times [13].

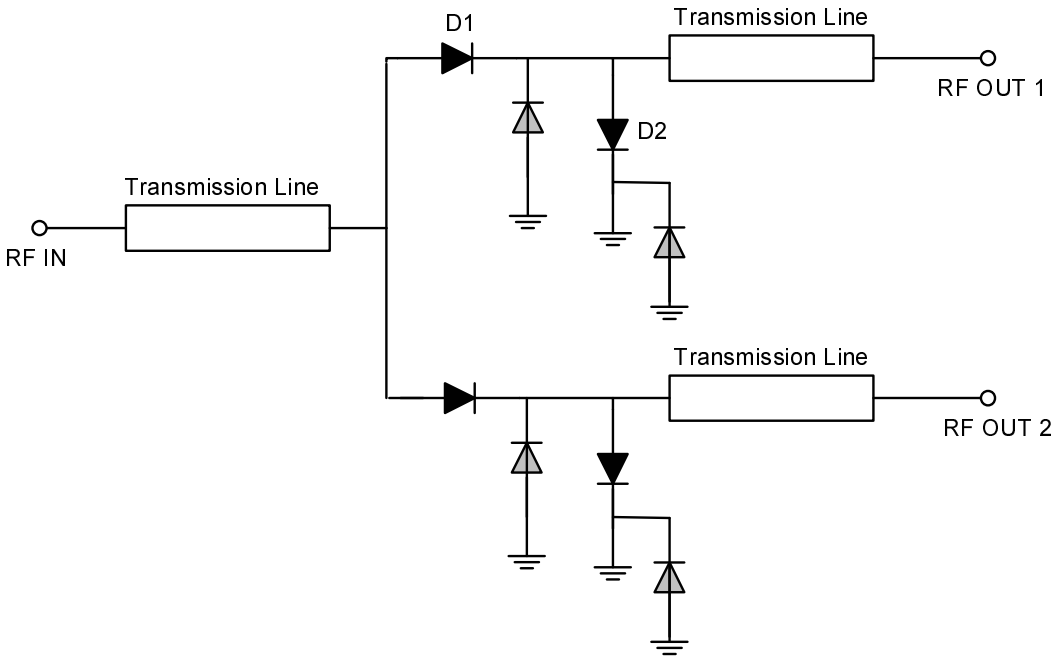


Fig. 3.2. Conventional design topology of an SPDT PIN diode switch including parasitic Psub-Nwell diodes

While the effect of a parasitic diode might be negligible for small signals, it may cause leaking when the larger voltage swings occur at the cathode of a series diode.

D. Improved design of PIN diode based SPDT switch

Whilst it is impossible to eliminate the above parasitic diode, its effect can be minimised. By reversing the polarity of PIN diodes in the circuit and reversing the biasing settings at the terminals RF OUT1 and RF OUT2, the parasitic diodes produced by series PIN diodes will be positioned in such a way that both their cathode and anode terminals will be connected to ground. The parasitic diodes produced by shunt PIN diodes will be positioned in parallel with them as described in fig. 3.4. Such topology will ensure that parasitic diodes will either not be forward biased or will have the same polarity as their “master” PIN diodes. It does not, however, fully eliminate the possibility

of a large negative voltage swing moving the cathode potential into the negative area.

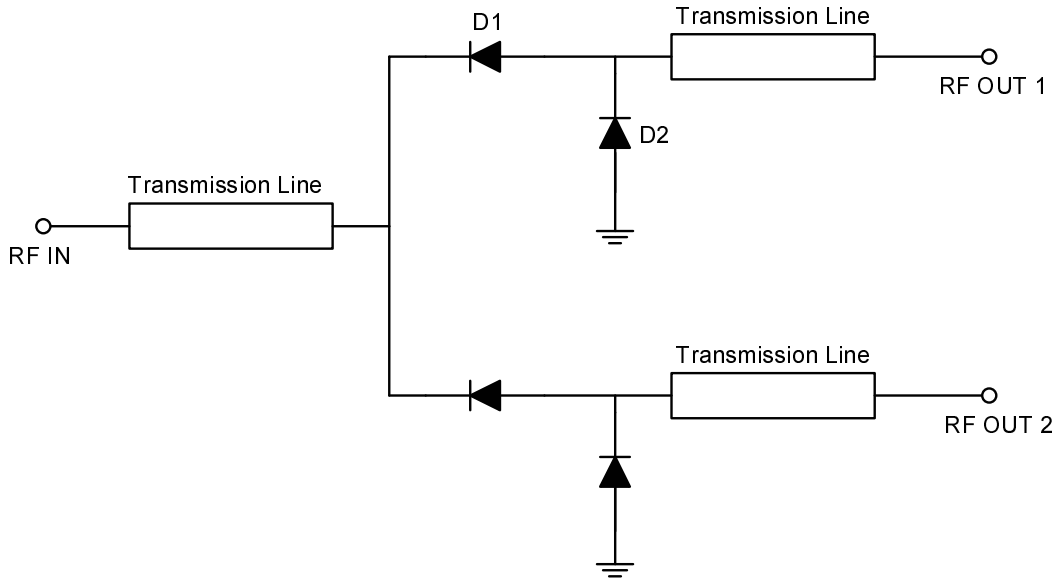


Fig. 3.3. Improved design topology of an SPDT PIN diode switch

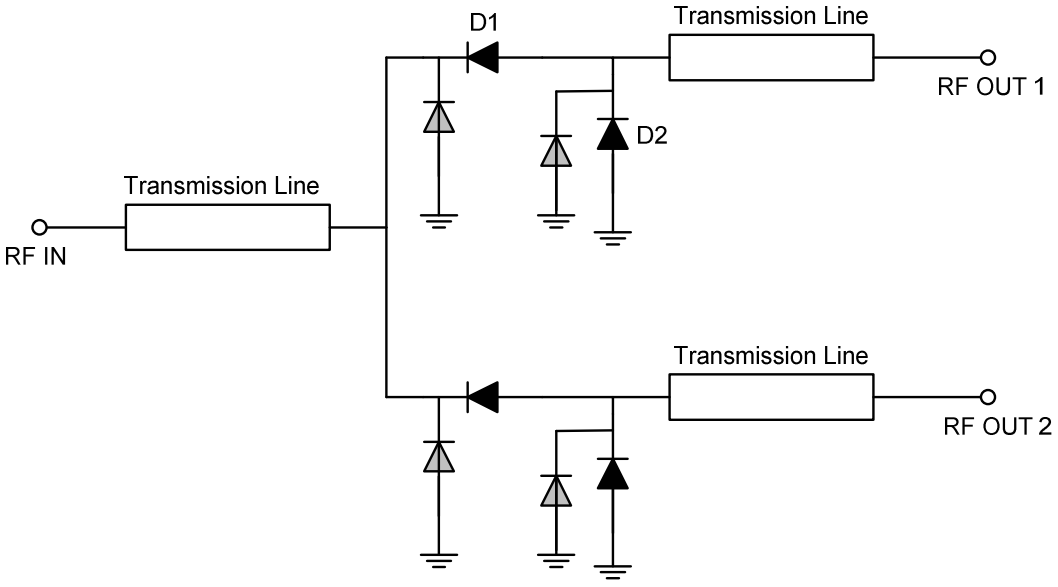


Fig. 3.4. Improved design topology of an SPDT PIN diode switch including parasitic Psub-Nwell diodes

Each arm of the switch implements a series-shunt diode combination. This is a

most common topology used for SPDT switch whether it is based on MOSFET SPST switches or PIN diode SPST switches. ARMAG group produced three PIN diodes with different anode area: 6.25 μm^2, 25 μm^2 and 50 μm^2. PIN diode with the smallest anode area would increase the isolation due to reduced PN capacitance but would increase the insertion loss due to the smaller contact area. On the other hand, PIN diode with the largest anode area would decrease the insertion loss but also decrease isolation. It was experimentally determined that 25 μm^2 – 50 μm^2 series-shunt diode combination would result in the best balance between lowering insertion loss and increasing isolation.

E. Asymmetrical design of PIN diode SPDT switch optimised for use in transceiver applications

Symmetrical topology of SPDT switches discussed in parts B, C, and D provide for identical insertion loss and isolation between RF IN and RF OUT1 and between RF IN and RF OUT2. However, in case of transceiver application, such symmetry may not yield the optimum results. The balance between insertion loss and isolation for the transmitter is not the same as the balance for the receiver. Since the incoming signal at the receiver's input is very small, it is important to minimise the insertion loss in order to prevent the incoming signal from further attenuation. For the transmitter, on the other hand, it is not very critical to maintain very minimal insertion loss because the transmitted signal already carries large power. It is of crucial importance to instead minimise the leakage from the TX channel into the RX channel during the receiving mode. In light of these requirements, an improved asymmetrical topology is proposed in which the transmitter arm of the switch will utilise series-shunt-shunt diode combination.

Such combination will increase the insertion loss due to leakage from two shunt diodes, but most importantly, it will increase isolation between antenna and TX path when the transceiver is operating in RX mode. The proposed topology is presented in fig. 3.5.

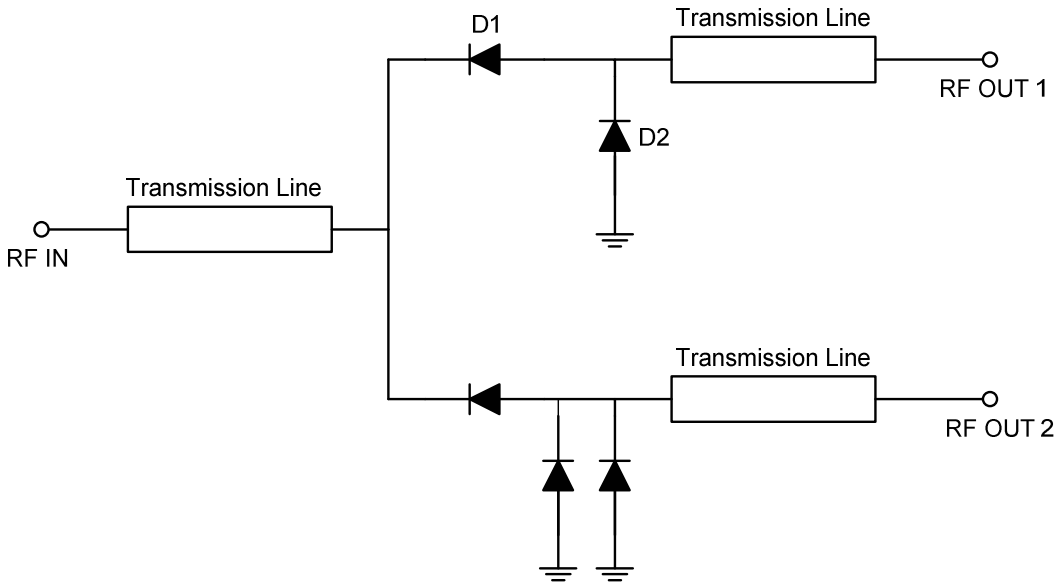


Fig. 3.5. Asymmetrical topology of an SPDT PIN diode switch for improved isolation

This design too features reversed polarities of the PIN diodes to minimise the effect of parasitic diodes. Fig. 3.6 depicts the schematic view of the asymmetrical topology including the parasitic diodes. The drawback of this design is 25% increase in DC power consumption when the transceiver is in the RX mode.

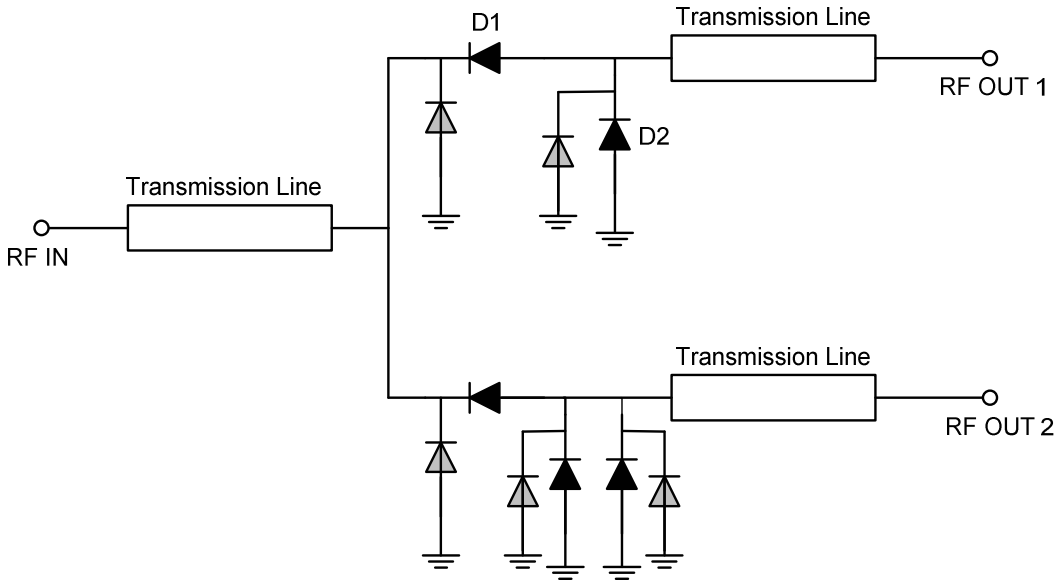


Fig. 3.6. Asymmetrical topology of an SPDT PIN diode switch for improved isolation including parasitic Psub-Nwell diodes

F. Asymmetrical SPDT switch performance and implementation

The simulation results for RX arm and TX arm of the asymmetrical SPDT switch are presented in fig. 3.7 and fig. 3.8, respectively. The operating frequency range is from 6 GHz to 18 GHz which fully covers X and Ku bands used for communication satellites. The post-layout simulations were performed with the parasitics extracted from the final layout utilising ADS Momentum tool and the BiCMOS SiGe 0.18-µm substrate data provided by Jazz Semiconductor. For RX arm of the switch, the insertion loss varies from 0.72 dB at 6 GHz to 1.15 dB at 18 GHz, the isolation varies from 48 dB at 6 GHz to 40.5 dB at 18 GHz, and the return losses are all above 11 dB. For TX arm, the insertion loss is slightly higher ranging from 0.74 dB to 1.4 dB over the range of 6 – 18 GHz, the isolation is improved compared to RX by about 5 dB ranging from 53.7 dB at 6 GHz to 45.5 dB at 18 GHz. The return losses are above 9.5 dB. The average current being drawn from 2 V source is 2-3 mA, depending on whether the switch is in RX or TX mode.

Table I presents the comparison between the proposed asymmetrical switch and the MOSFET SPDT switch in [15] and [14] with impedance transformation network (ITN). Due to superior insertion loss and isolation of PIN diode SPST switch, SPDT switch presented in this work shows lower insertion loss and significantly improved isolation compared to CMOS switches in [15] and [14].

TABLE I
PERFORMANCE COMPARISON OF PROPOSED SPDT SWITCH

	This work RX	**This work TX**	[15]	[14]
Insertion Loss (dB) @ 15 GHz	**0.72**	**0.74**	1.8	3.5
Isolation (dB) @ 15 GHz	**42.1**	**47.3**	17.3	40.5
Return Loss (dB) when the switch is on (S11/S22) @ 15 GHz	**13/13.5**	**11/12**	24/12.5	19.5
Power Supply (V)	**2**		3	1.8
Power Consumption (mW)	**4-6**		0	~0

The fabricated series-shunt and series-shunt-shunt PIN diode SPDT switches measure 673 µm by 385 µm each (Fig. 3.9 and 3.10).

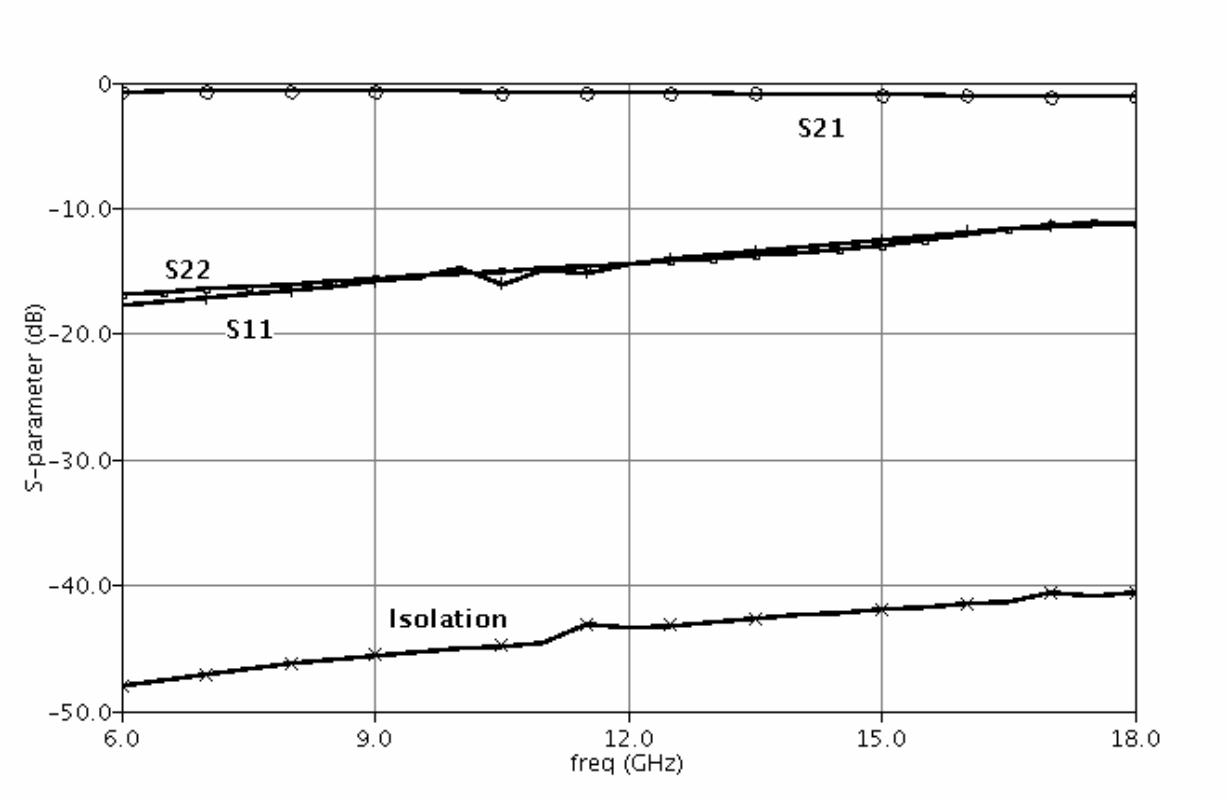


Fig. 3.7. Simulated S-parameters of RX arm of the switch

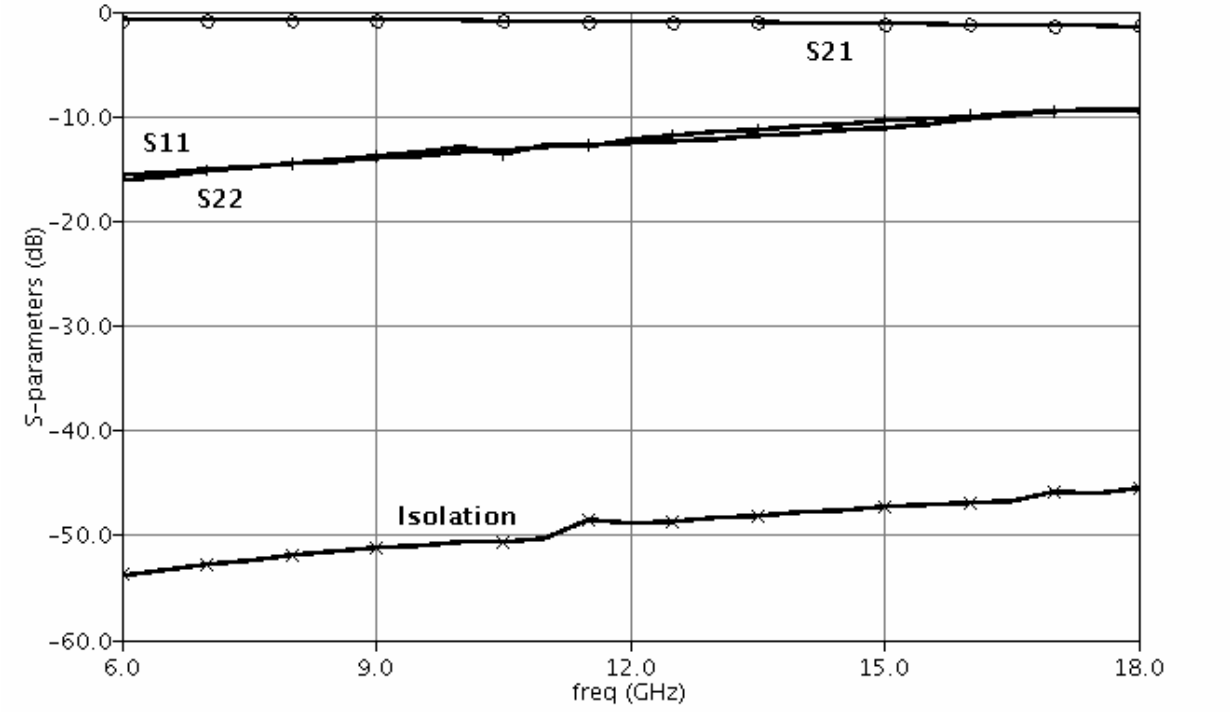


Fig. 3.8. Simulated S-parameters of TX arm of the switch

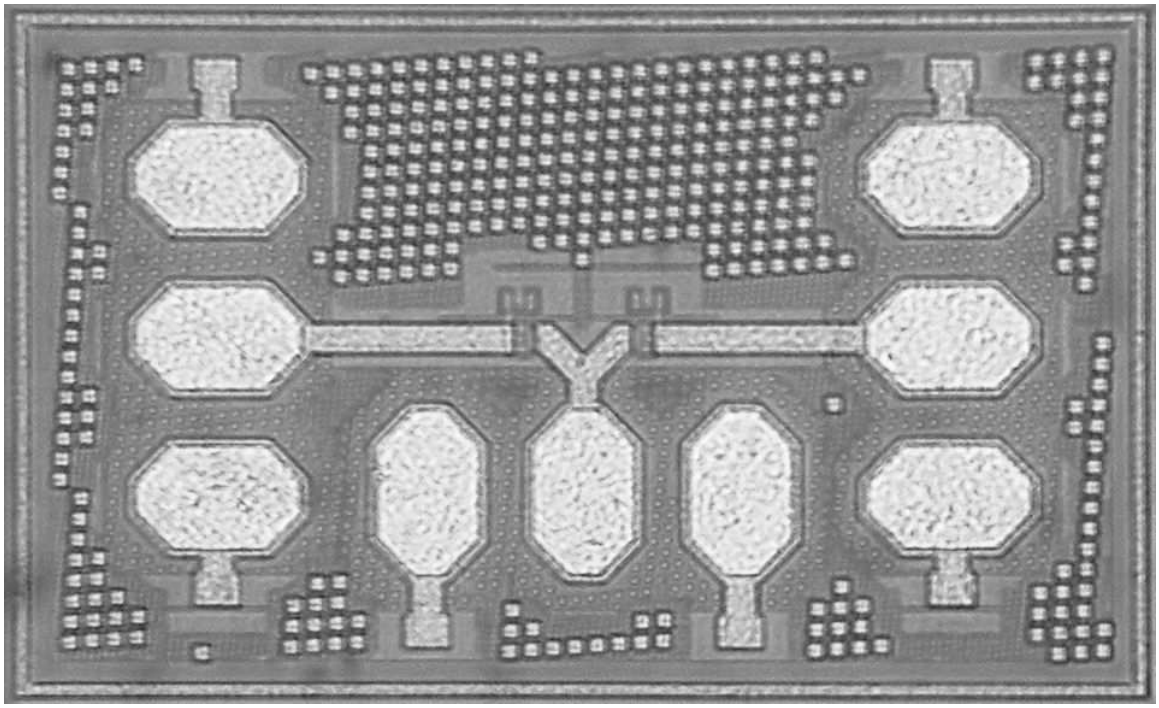


Fig. 3.9. Microphotograph of a series-shunt symmetrical SPDT switch

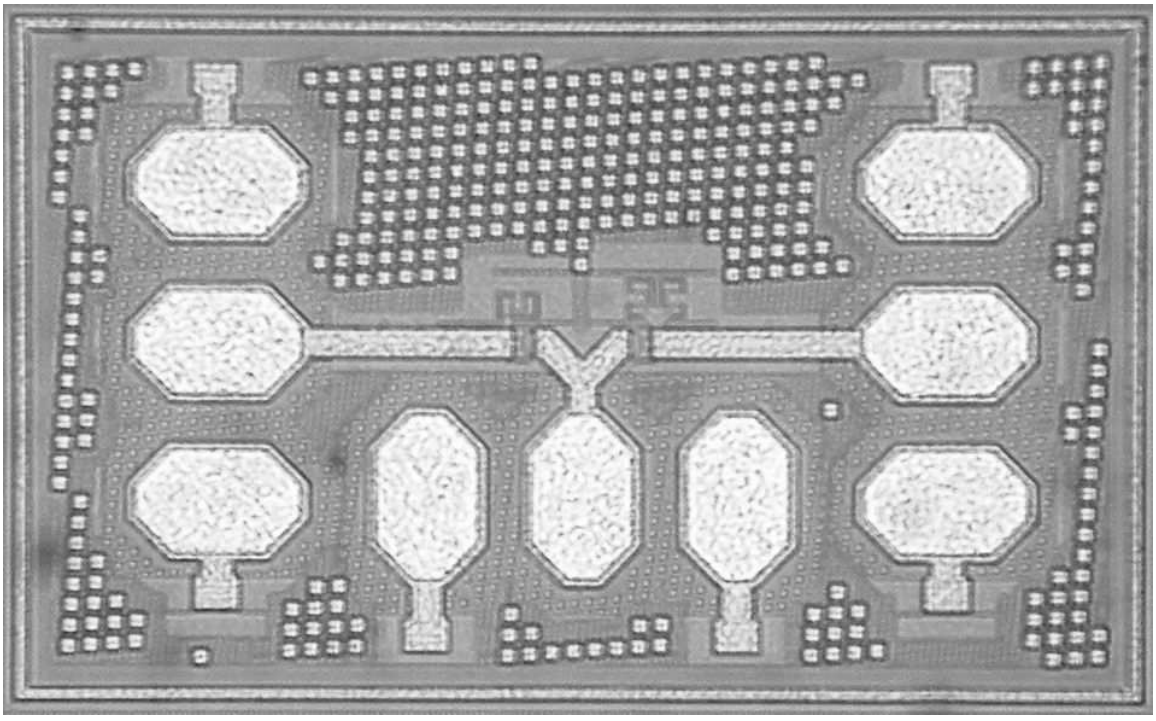


Fig. 3.10. Microphotograph of a series-shunt-shunt asymmetrical SPDT switch

CHAPTER FOUR
3-BIT PIN DIODE BASED ATTENUATOR

A. Introduction

State-of-the-art satellite communication systems utilise phased-array antennae to produce a beam in a desired direction. In turn, each element in the phased-array antennae utilise phase shifter and amplifiers in order to set the correct phase delay and the magnitude of the signal waveform. At times, variable gain amplifiers (VGA) are deployed to vary the signal magnitude, but as every other active device, VGA may produce distortion and contribute to noise degradation. In addition, CMOS VGA do not typically operate over the wide frequency bands. In certain applications, it might be crucially important to produce accurate attenuation steps rather than to maintain the overall gain.

If the primary concern for the signal attenuation is power handling capabilities, wide frequency band and accurate attenuation steps, a passive PIN diode based attenuator might be considered. This chapter will present the 3-bit passive PIN diode attenuator that is operated with discrete switching control.

B. Π- and T-network attenuation design

Single cell attenuator can be represented as a two-port network that can be described in terms of Z parameters. The most common attenuation topologies are Π-type and T-type, ash shown in fig. 4.1 and 4.2. Based on the desired attenuation, input and output impedance, it is possible to calculate the values of the resistive components. The resistive topology was chosen for maximising the frequency band and reducing the

effective area of the chip. Equations (4.1)-(4.3) and (4.4)-(4.6) allow for calculating the values of R1, R2, and R3 for Π-type and T-type networks, respectively [8].

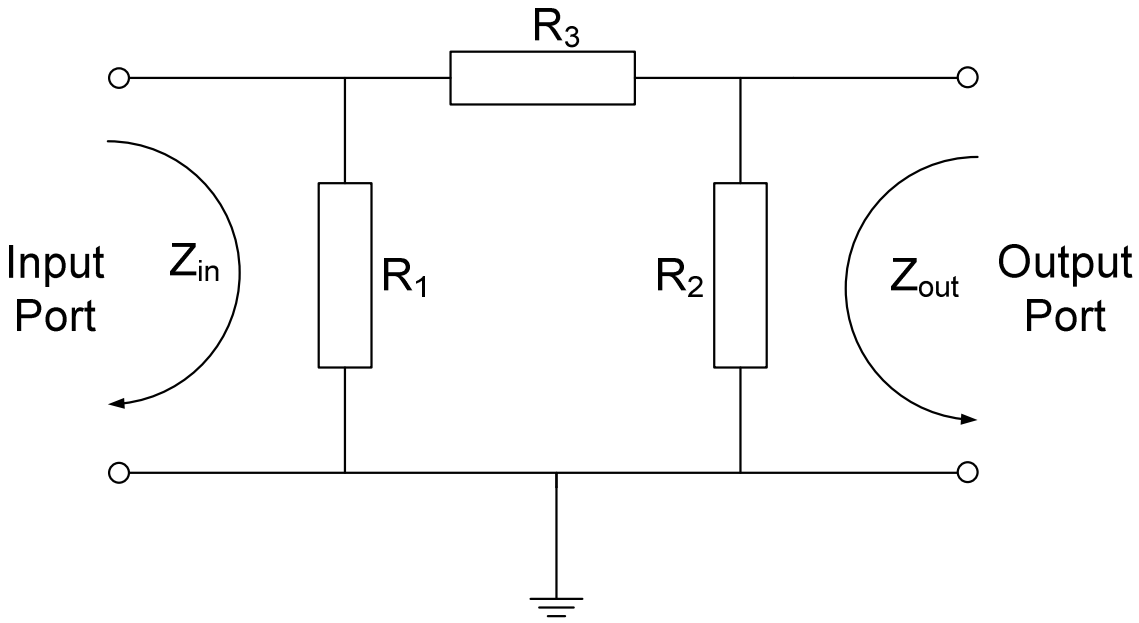


Fig. 4.1. Π-type network attenuation topology

$$R_3 = \frac{1}{2}(10^{L/10} - 1)\sqrt{\frac{Z_{in} \cdot Z_{out}}{10^{L/10}}} \tag{4.1}$$

$$R_1 = \frac{1}{\frac{10^{L/10}+1}{Z_{in}(10^{L/10}-1)} - \frac{1}{R_3}} \tag{4.2}$$

$$R_2 = \frac{1}{\frac{10^{L/10}+1}{Z_{out}(10^{L/10}-1)} - \frac{1}{R_3}} \tag{4.3}$$

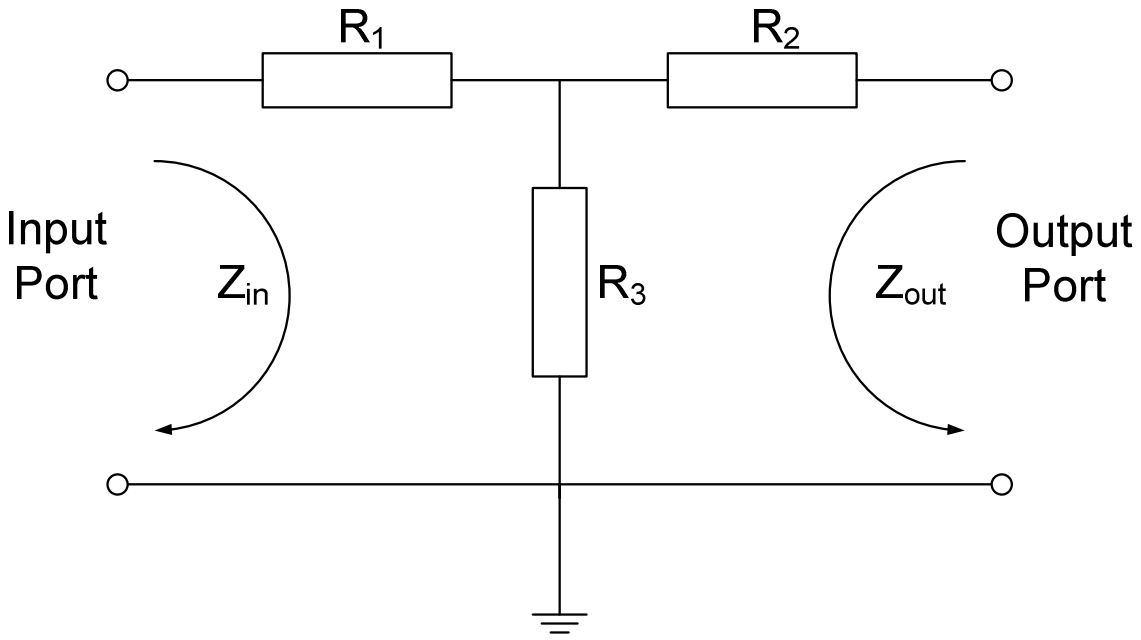


Fig. 4.2. T-type network topology of an attenuator

$$R_3 = 2\frac{\sqrt{Z_{in} \cdot Z_{out} \cdot 10^{L/10}}}{10^{L/10} - 1} \tag{4.4}$$

$$R_1 = \frac{10^{L/10} + 1}{10^{L/10} - 1} \cdot Z_{in} - R_3 \tag{4.5}$$

$$R_2 = \frac{10^{L/10} + 1}{10^{L/10} - 1} \cdot Z_{out} - R_3 \tag{4.6}$$

C. Proposed topology of PIN diode based attenuator

As shown in previous chapters, a novel PIN diode designed and fabricated by ARMAG group achieves low insertion loss, high isolation and high power handling capabilities. This diode is used as a SPST switch in the proposed attenuator design to switch the signal between reference path and attenuation path. Fig. 4.3 presents a single

cell of the attenuator. Two 50 μm^2 PIN diodes (D1 and D2) are included in the reference

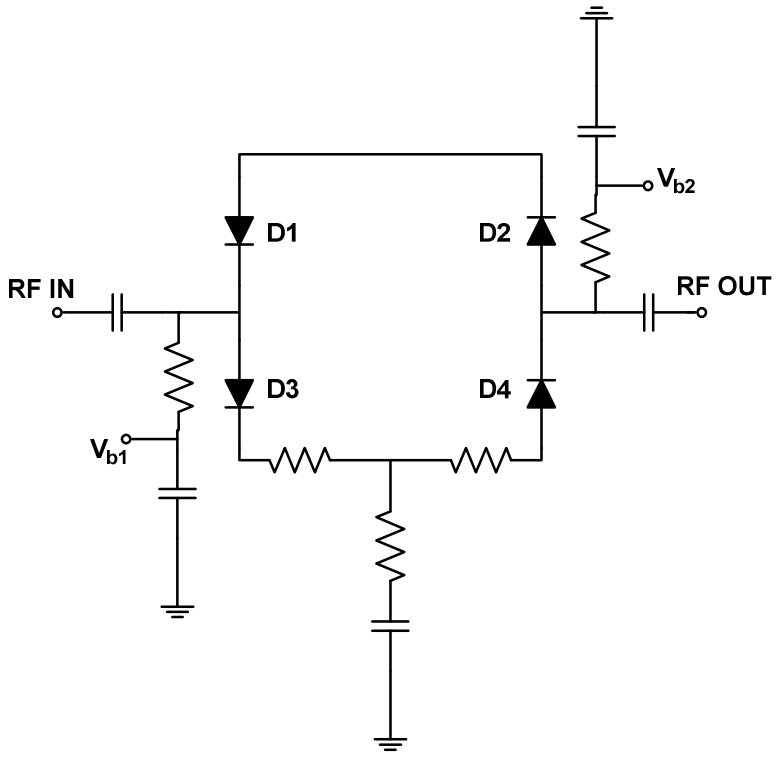


Fig. 4.3. Single cell of the PIN diode based attenuator

path (path that provides the least attenuation) and two 50 μm^2 PIN diodes (D3 and D4) are used in the attenuation path. The size of 50 μm^2 was chosen for each series diode due to its low insertion loss. At the same time, series-series topology would ensure improved isolation. The insertion loss due to series-series configuration for reference and attenuation path would be the same, so the relative attenuation would only depend on the resistive attenuation network. By biasing diodes to make them forward biased or reversed biased, we can enable reference path while disabling the attenuation path, and vice verse. For the attenuation path, a resistive T-network topology was chosen over Π-network topology in order to reduce the chip area. Since the PIN SPST switches are controlled

with the bias DC current, the design needs to utilise the DC blocking capacitors that would prevent DC current from leaking to the ground and at the same time ensure the broadband performance of the attenuator. Thus, T-network topology would utilise one DC blocking capacitor whilst Π-network topology would need to utilise two. Depending on the operational frequency, the size of such DC blocking capacitor would vary ranging from ~7 pF at 6 GHz to ~2.5 pF at 18 GHz. The area size reduction becomes even more significant if several attenuation cells are used in the attenuator.

The switching between reference and attenuation paths occurs in the following way: when V_{b1} = 0 V and V_{b2} = 3.3 V, diodes D1 and D2 are forward biased while diodes D3 and D4 are reverse biased which results in reference path being the pass-through path for the RF signal while attenuation path is isolated. When V_{b1} = 3.3 V and V_{b2} = 0 V, diodes D3 and D4 will be forward biased while diodes D1 and D2 will be reverse biased which will turn on the attenuation path and turn off the reference path for the RF signal.

As it can be recalled from chapter three, the N+ subcollector layer and p-substrate layer of a PIN diode will form a parasitic Psub-Nwell diode. The cathode of such parasitic diode shares the same terminal with the PIN diode's cathode, and its anode is connected to ground. Since this anode has the constant bias potential, the parasitic diode may enter into forward bias region if there is a large negative voltage swing at its cathode. This would produce signal leakage, and as a consequence, degradation in linearity. By setting bias voltage to zero or positive value, we ensure that DC voltage will not drop below zero and will not turn on the parasitic Psub-Nwell diode.

D. Proposed topology of 3-bit PIN diode based attenuator

The proposed 3-bit attenuator is composed of three attenuation cells from fig. 4.3 connected in series. Adjusting the values of T-network resistors, we can set the desired attenuation relative to the reference path. DC blocking capacitors will ensure the separation of different DC bias currents. Fig. 4.4 depicts the proposed 3-bit attenuator. The attenuation steps are produced by switching between the attenuation path and the reference path for each individual cell.

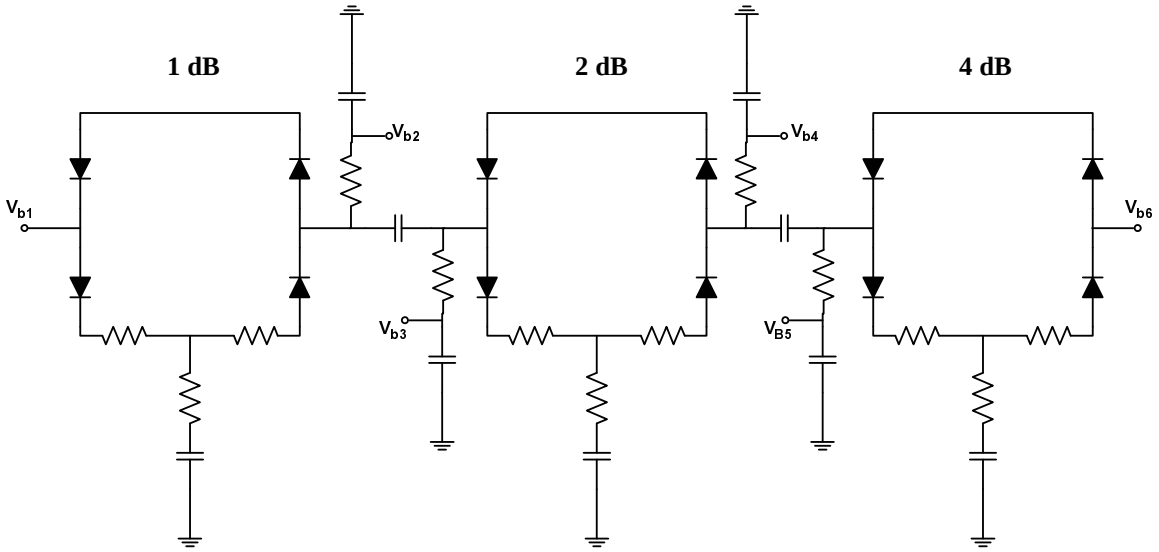


Fig. 4.4. 3-bit PIN diode based attenuator

E. Implementation and Simulation Results

The post-layout simulation results were performed on the circuit using the extracted RLC interconnections parasitics that were obtained utilising ADS Momentum and the substrate data provided by Jazz Semiconductor for BiCMOS 0.18-µm SiGe process. Simulation results show quite accurate broadband performance over the frequency range from 6 GHz to 16 GHz (Fig. 4.5). For the 3-bit attenuator, each individual bit would provide 1 dB, 2 dB and 4 dB attenuation; thus, the resolution is 1 dB

and the maximum possible attenuation is 7 dB. As expected, the error is accumulated with every enabled attenuation cell. The largest deviation occurs for the maximum relative attenuation of 7 dB and constitutes 0.65 dB.

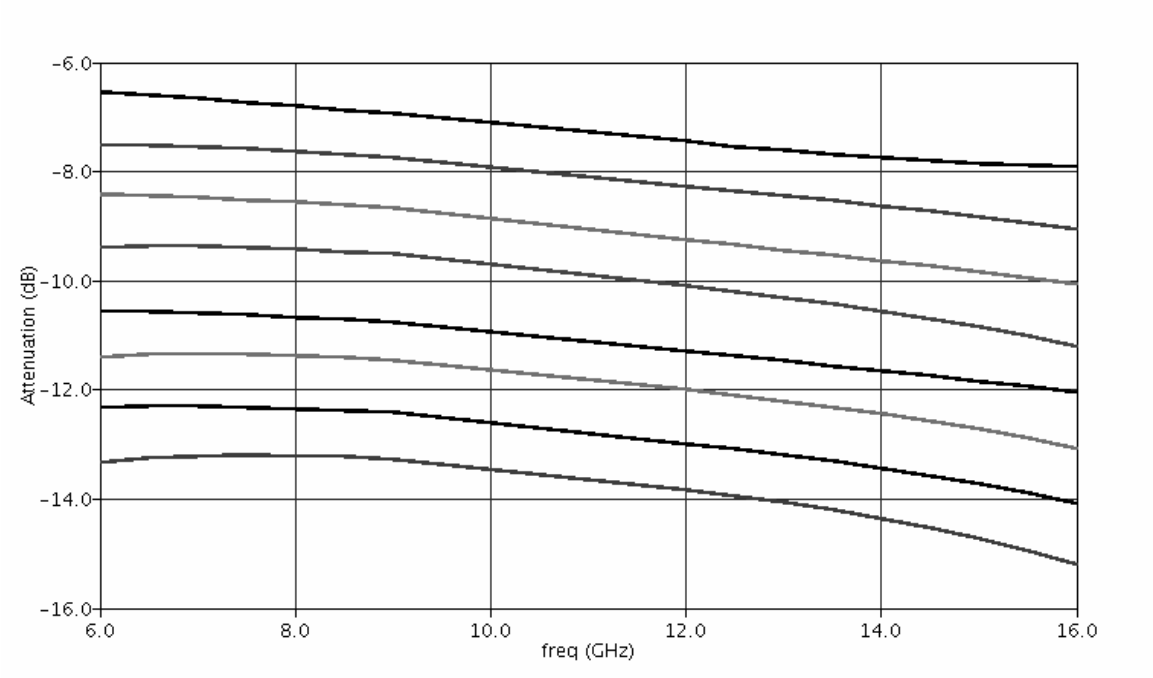


Fig. 4.5. Simulated S-parameters performance of the 3-bit attenuator

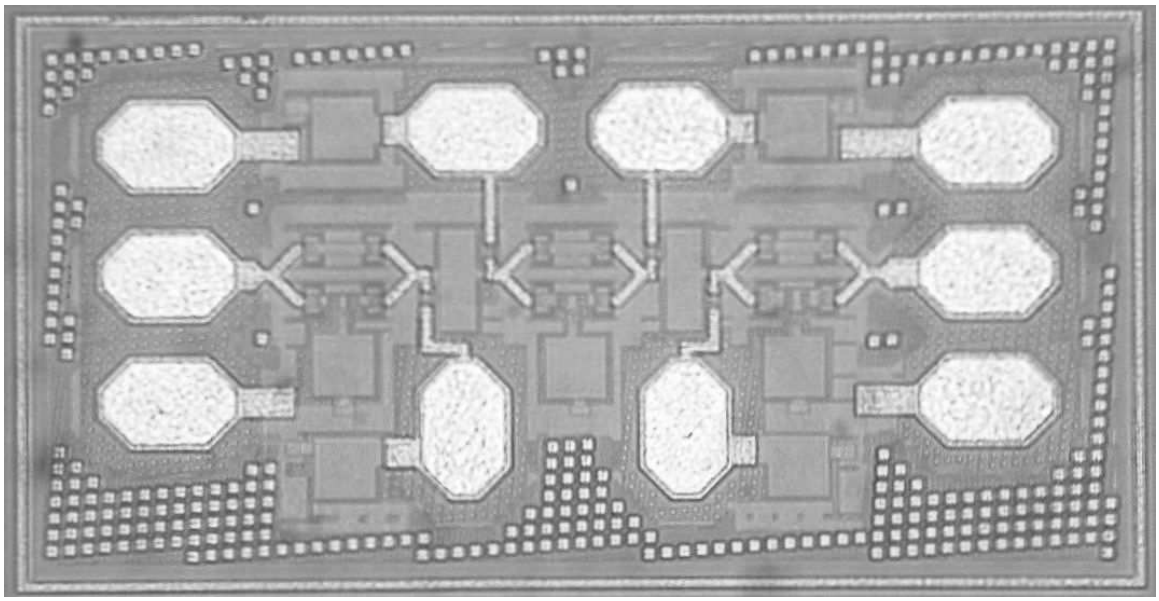


Fig. 4.6. Microphotograph of a 3-bit attenuator

The fabricated PIN diode based 3-bit attenuator measures 850 µm by 412 µm (Fig. 4.6). The performance measurements are in the initial stage and are expected to closely match the post-layout simulated results presented in fig. 4.5.

Table II presents the comparison of the PIN diode based attenuator discussed in this thesis with [16] and [17]. From table II, the proposed 3-bit SiGe PIN diode attenuator has the comparable frequency range, insertion loss and return loss; however, the biggest advantage is the small chip size and the fabrication cost. The attenuator proposed in this work can be easily integrated in the SoC satellite communication systems which would result in significant cost savings.

TABLE II
PERFORMANCE COMPARISON OF PROPOSED 3-BIT PIN DIODE ATTENUATOR

	[16]	[17]	**This work**
Device Technology	GaAs pHEMT	InGaAs PIN	**SiGe PIN**
Freq (GHz)	DC – 40	6 – 20	**6 – 16**
Number of bit	5	3	**3**
Attenuation Range (dB)	23	28	**7**
Insertion Loss (dB)	6.0 – 8.0	4.0 – 4.5	**6.0 – 8.0**
Return Loss (dB)	14	10.0	**12**
Size/bit (mm^2/bit)	0.89	0.49	**0.069**

CHAPTER FIVE

HIGH LINEARITY LOW POWER PIN DIODE PHASE SHIFTER DESIGN

A. Introduction

Phase shifters enjoy a wide variety of applications, especially as an integrative part of beam-steering devices in phased-array antenna systems to electronically control the radiation pattern by reinforcing it in a desired direction and suppressing it in undesired direction. The traditional implementation of phase shifter was that of GaAs IC technology or micro-electromechanical systems (MEMS) for high-end military and commercial applications. However, due to low integrative capabilities such implementations result in high cost. MOSFET-based active phase shifters can also be utilized in beam-forming applications, but the off-state capacitance of a MOSFET negatively impacts the performance by limiting the bandwidth. In addition, because of the active nature of MOSFET-based phase shifters, the linearity tends to degrade as well.

Recently, phase shifters have been implemented in CMOS or silicon germanium (SiGe) BiCMOS processes for high-end applications [18], [19]. Development in SiGe BiCMOS technology offers microwave performance with high integration levels that makes it possible to design low cost, compact, high performance phase shifters. This chapter describes an MMIC phase shifter developed in a standard six-level metal SiGe BiCMOS process that offers high performance transistors with peak cutoff frequency (f_t) of 155 GHz and high quality passive components. A variety of circuit topologies has been proposed for the implementation of MMIC phase shifters [19]-[21]. The high-pass/low-pass filter topology is widely used due to excellent power-handling capability [22]-[23]. This technique will be used to implement the 4-bit phase shifter.

B. Phase Shifter High-Pass/Low-Pass Filter Topology

MMIC phase shifter was designed in a 6-level metal 0.18-µm SiGe BiCMOS process taking advantage of high-frequency transistors' cut-off frequency of 155 GHz as well as high-quality passive components. Figure 5.1 presents topologies for the 180° and 90° bits of the phase shifter.

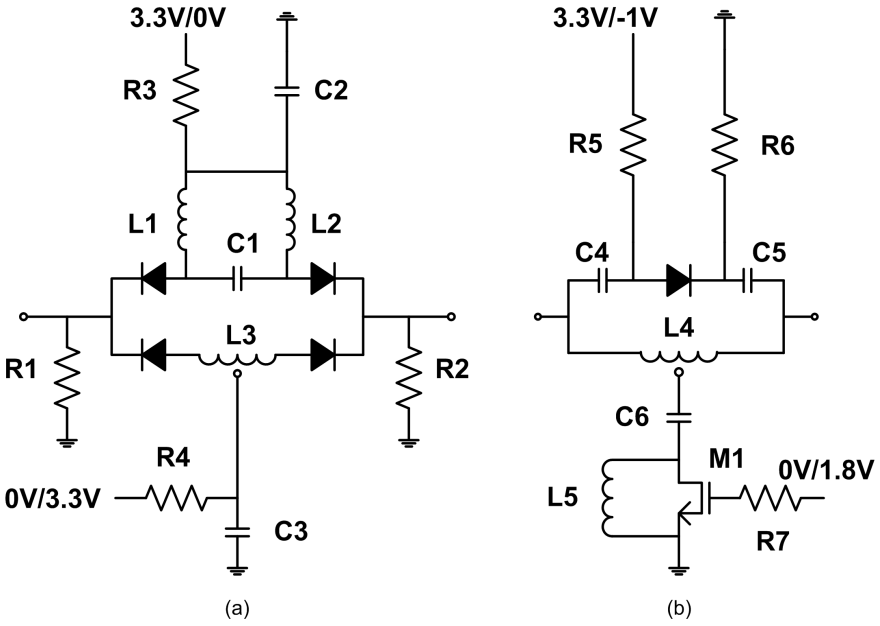


Fig. 5.1. Circuit topologies for each bit with differential inductor (L3 and L4) and high performance SiGe PIN diodes for 180^o, 90^o, 45^o, and 22.5^o phase shifter bits: (a) 180^o phase shifter bit; (b) 90^o, 45^o, and 22.5^o phase shifter bits [26]

The 180^o phase shifter bit is based on hybrid topology that uses high-pass/low-pass filters utilizing SiGe PIN diode switches. High pass π-shape filter (HPF) has the least negative phase delay, which serves as a reference path. The 90^o, 45^o, and 22.5^o phase shifter bits use bridged-T type filter utilizing both PIN diode and MOSFET switches to improve linearity and insertion loss, and DC power consumption, respectively. A low pass T-shape filter (LPF) has the most negative phase delay which

serves as delay path.

The linearity performance of a SiGe phase shifter with an integrated LNA was characterized in [20]. High linearity of phase shifter is one of important requirements for the beam former applications in jamming environments. In this dissertation, improved linearity performance of a silicon PIN diode-based phase shifter will be demonstrated. The PIN diode switch is inherently more linear because its off-state capacitance is mainly determined by the width of the intrinsic region and can be treated as a fixed value; thus mitigating the large-signal distortion effect. For a miniature design, differential inductors are used to replace the long transmission lines. Also, hybrid switched-filter topology is implemented with two different switches: SiGe PIN diodes [25] are used on an RF signal path for high linearity and low insertion loss, and MOSFET switches are used for parallel resonance to achieve low insertion loss with reduced power dissipation.

C. Phase Shifter Design Calculations

As shown in Fig. 5.1, the 180^{o} bit employs a high-pass/low-pass filter because this structure can achieve a large phase shift over a wide frequency range. The high-pass - shape filter (HPF) has the least negative phase delay and serves as the reference path. The low-pass T-shape filter (LPF) has the most negative phase delay. First-order formulae for the component values in high-pass/low-pass filters are modified from [23]:

$$L_1 = L_2 = \frac{Z_0 \sin(\theta_1)}{\omega(1-\cos(\theta_1)} \tag{5.1}$$

$$C_1 = \frac{1}{\omega Z_0 \sin(\theta_1)} \tag{5.2}$$

$$\frac{L_3}{2} = Z_0 \frac{1-\cos(\theta_2)}{\omega \sin(\theta_2)} \tag{5.3}$$

$$C_3 = \frac{\sin(\theta_2)}{\omega Z_0} \tag{5.4}$$

Z_0 is 50 Ω characteristic impedance. In (5.3), L_3 represents two inductances for either side of the LPF. θ_1 and θ_2 are frequency-dependent phase delays for the high-pass and low-pass filters, respectively. Eq. (5.5)-(5.7) shows the relative phase shift (θ_1- θ_2) between high-pass and low-pass filters. The derivative of the argument inside the inverse cosine function in (5.5) over frequency is zero at ω_0, which implies that the relative phase flattens out around the centre frequency.

$$\theta_1 - \theta_2 = \cos^{-1}\left(K - \left(\frac{L_3 C_3}{2}\omega^2 + \frac{1}{L_1 C_1 \omega^2} \right) \right) \tag{5.5}$$

$$K = 1 + \frac{L_3 C_3}{2 L_1 C_1} + \frac{C_3}{C_1} \tag{5.6}$$

$$\omega_0 = \frac{1}{\sqrt[4]{L_3 C_3 L_1 C_1 / 2}} \tag{5.7}$$

Customized octagonal shape 25 μm^2 PIN diodes (insertion loss ≈ 1 dB) are used on the HPF path, and 50 μm^2 PIN diodes (insertion loss ≈ 0.8 dB) are used on the LPF path as single-pole-double-throw (SPDT) switches [25]. The use of two different PIN diodes is applied to achieve a balance of insertion losses between the two paths. Larger PIN diodes have lower insertion loss but worse isolation, while smaller PIN diodes gives better isolation but higher insertion loss. In all phase shifter bits, a PIN diode switch is used in a series fashion because it generates less distortion than a shunt PIN diode switch.

The 90^o, 45^o, and 22.5^o bits use a bridged-T filter since it has lower insertion loss

and provides medium phase shift. As can be seen in Fig. 5.1(b), a differential inductor is used instead of two single-ended transmission lines to minimize chip area. The 50 μm^2 PIN diodes are used as single-pole-single-throw (SPST) switches for low insertion loss. When the PIN diode is turned on, the reference path dominates the signal route. L_5 resonates with the parasitic capacitance C_p from M_1 at 15 GHz to float the LPF. When the PIN diode is reverse biased, L_5 is grounded by M_1, and the LPF routes the signal. L_4 and C_6 are based on Eq. (5.3)-(5.4). L_5 can be derived from Eq. (5.8).

$$L_5 = \frac{1}{\omega^2 C_p} \tag{5.8}$$

D. Implementation and Measurement Results

Fig. 5.2 shows a photograph of a fabricated 4 bit phase shifter. The die size is only 1.6 mm × 0.37 mm, excluding the testing pads. All four phase shifter bits are cascaded in a row so that they provide digitally controlled 16 phase states between 0^o and 360^o with 22.5^o granularity.

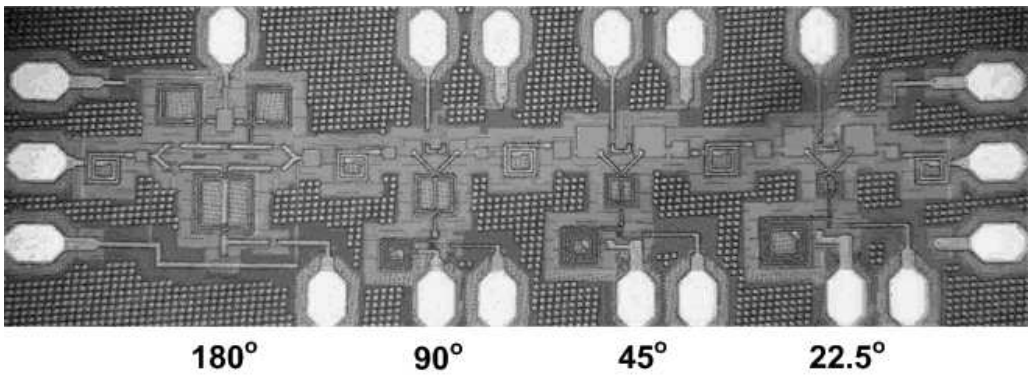


Fig. 5.2. Chip photograph of the 4-bit phase shifter in standard 0.18 um SiGe BiCMOS process (1.6 mm × 0.37 mm excluding the testing pads) [26].

Fig. 5.3 shows the measured 16 phase states from 14.5 GHz to 15.5 GHz with on-wafer probing. This phase shifter has a maximum phase error of 18.6^{o} at the nominal 180^{o} phase state because of the inaccurate isolation model of the 25 μm^2 PIN diode used in the HPF path at the prototype circuit design phase, which also causes the joining between the 180^{o} and 157.5^{o} phase states at around 15.5 GHz. This phase error can be corrected with a modified isolation model of 25 μm^2 PIN diodes. For most phase states, relative phase variation is less than ±1.8^{o} over the 1 GHz frequency range. The 157.5^{o} phase state has a relative phase variation of ± 3.8^{o} from 14.5 to 15.5 GHz.

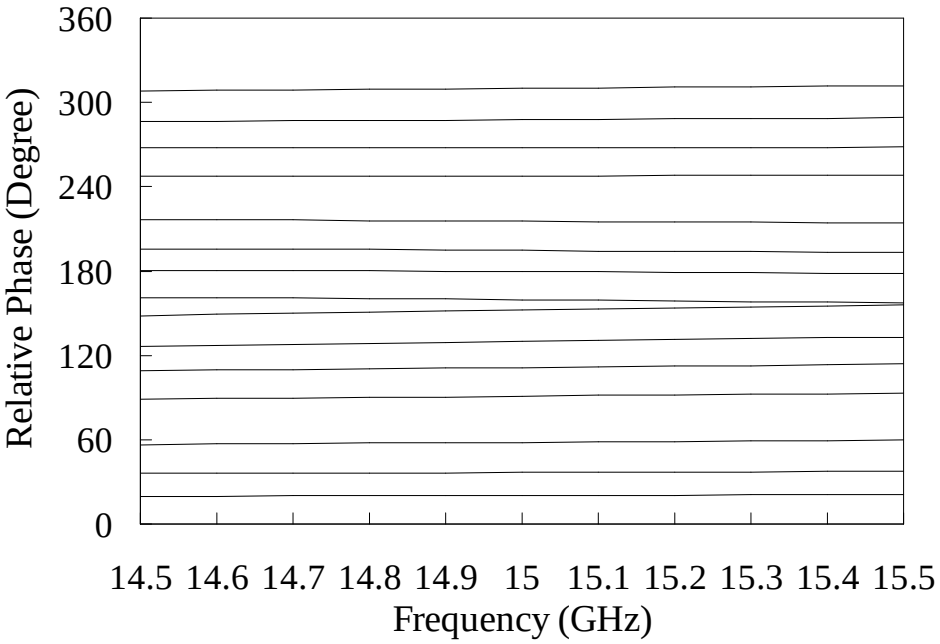


Fig. 5.3. Measured relative phase shifts for all 16 phase states [26].

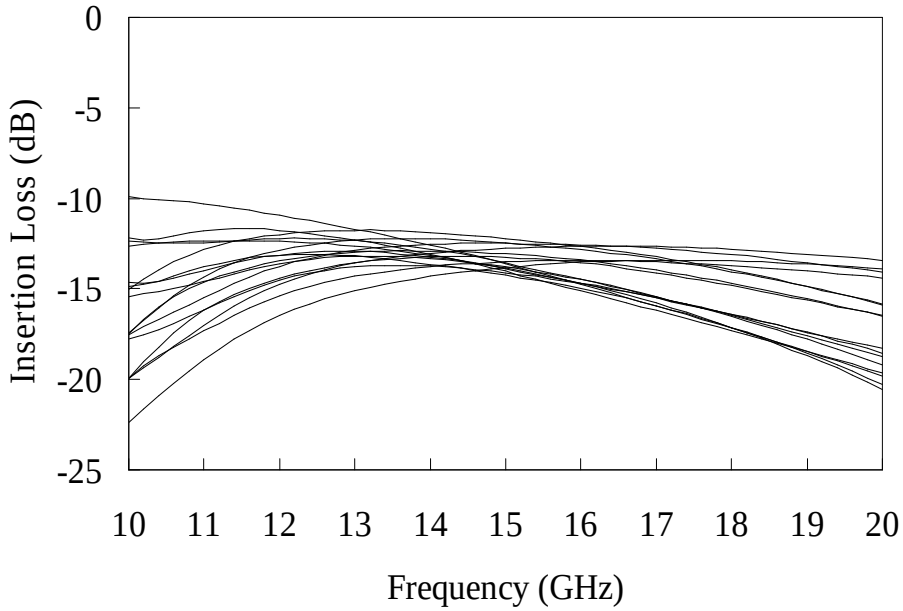


Fig. 5.4. Measured insertion losses for all 16 phase states [26].

Fig. 5.4 shows measured insertion losses from 10 to 20 GHz. At the 14.5 ~ 15.5 GHz frequency range, the insertion loss is 13.2 dB ± 1 dB, caused by PIN diode switches and passive components along the signal path. Fig. 5.5 and 5.6 show 20 dB ± 5 dB return loss for both the input and output ports.

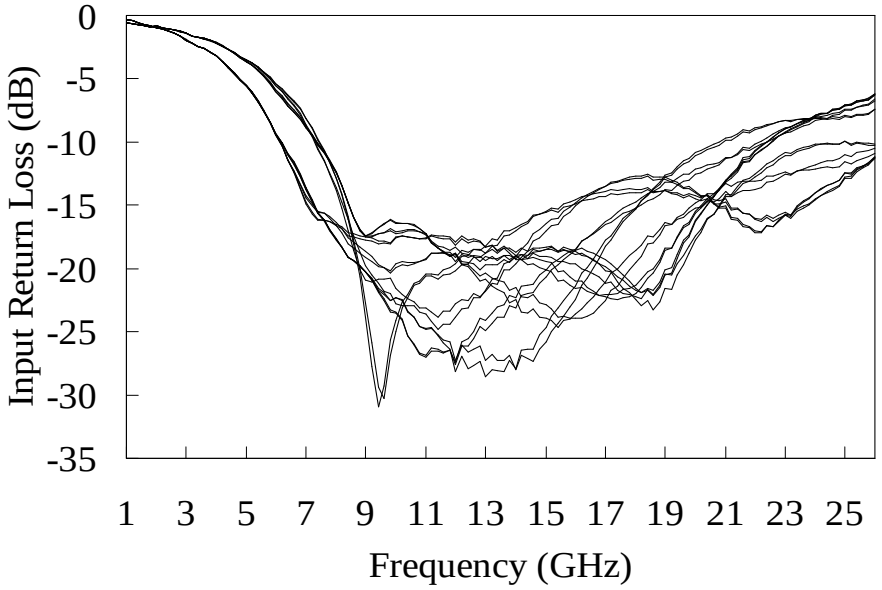


Fig. 5.5. Measured input return losses for all 16 phase states [26].

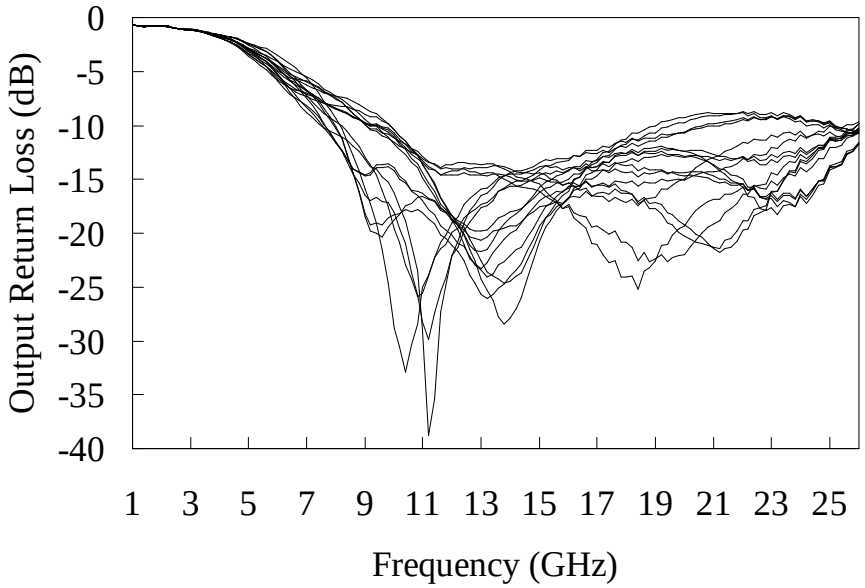


Fig. 5.6. Measured output return losses for all 16 phase states [26].

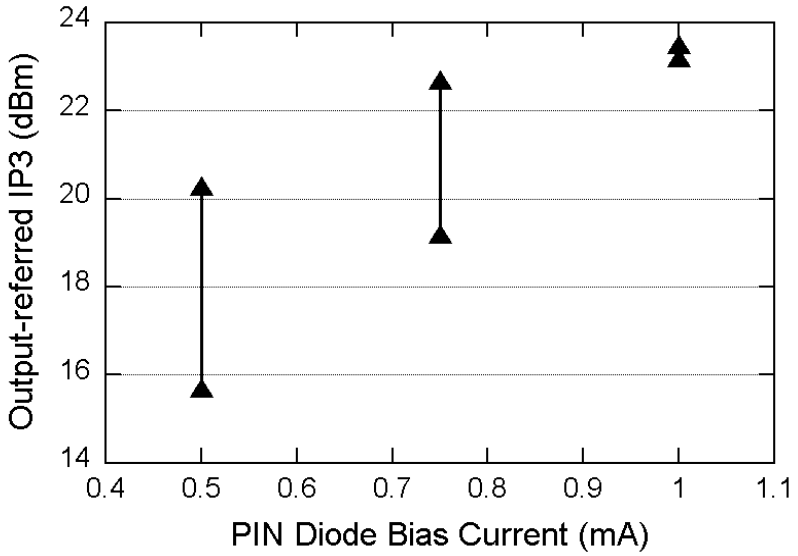


Fig. 5.7. Measured minimum and maximum output-referred IP3 of the phase shifter for different phase delay and bias current for each PIN diode [26].

Fig. 5.7 shows measured output-referred IP3 of the phase shifter at various DC bias currents for each turned-on PIN diode. Maximum input-referred and output-referred IP3 are 37 dBm and 23.2 dBm, respectively, at 1 mA biasing current for forward-biased

PIN diode and 10 MHz tone spacing. At 1 mA diode biasing current, the entire phase shifter draws 2 mA ~ 5 mA DC current from a 3.3 V power supply, depending on the phase state setting.

Table III summarizes and compares the performance of this phase shifter with other recently published X and K-band silicon-based phase shifters in terms of various aspects [26]. To the author's best knowledge, this 4-bit phase shifter achieves the highest linearity at Ku-band in standard SiGe BiCMOS process, due to the use of high performance PIN diode switches and passive components in each phase shifter bit. The phase error performance can be improved with more accurate isolation models of the 25 μm^2 PIN diode switch.

TABLE III. PHASE SHIFTER PERFORMANCE COMPARISON

	[19]	[20]	[21]	[24]	**This work**
Bits	5	4	4	6	**4**
Freq (GHz)	8 ~12	11 ~ 12	6 ~ 18	7 ~ 11	**14.5 ~ 15.5**
Insertion Loss (dB)	< 25	Gain 3.7 ±0.5	0.2 ~ 2.1	11	**12.2 ~ 14.2**
Phase Error	< 13^o	18^o	2.7 ~ 10^o	N/A	**< 18.6^o**
IIP3 or P_{1dB} (dBm)	N/A	-17.3 (IIP3)	-5.4 (input P_{1dB})	3 (output P_{1dB})	**37 (IIP3)**
Power Dissipation (mW)	< 1	53.5	8.7	45	**11.6**
Die Size (mm^2)	4.87 (with pads)	1.1 (without pads)	0.14 (without pads)	14.4 (with pads)	**0.6 (without pads)**
Process	SiGe BiCMOS	SiGe BiCMOS	CMOS	SiGe BiCMOS	**SiGe BiCMOS**

CHAPTER SIX

CONCLUSION

In today's market, telecommunication satellite systems play a very large role. The use of phased-array antennae in modern communication systems created a high demand for compact, high performance and highly integrative components for use in beam forming applications. Due to a high number of transceiver devices in each phased-array system, individual performance of TX and RX channels as well as their sub-components is of high importance for the overall performance of the entire system.

This thesis have concentrated on the applications of a novel octagonal SiGe PIN diode, and how it can improve the linearity, insertion and isolation of different sub-components in T/R modules that are used in satellite communication systems.

This work started with the overview of a novel octagonal PIN diode designed and fabricated by the members of ARMAG group. The PIN diode can works as a high performing SPST switch, thus it can be used in various applications that require low insertion, high isolation and high linearity switching devices. Until recently PIN diodes were fabricated in GaAs and InP processes, and, therefore, they could not be effectively integrated in a cheaper silicon-based technology. Instead, MOSFET devices were used in MMIC RF switches even though they suffer from poor linearity, low isolation and higher insertion loss. Custom designed SiGe BiCMOS PIN diode provided for new possibilities in designing high performance wide band switching devices while maintaining the same cost as with the use of MOSFET devices.

Several important components of T/R modules have been presented. New high

performance asymmetrical SPDT switch was optimised for the performance of individual TX and RX arms. Over the frequency range of 6 GHz to 18 GHz, it maintains low insertion loss of 0.95 to 1.15 dB for RX and an isolation of 53.7 dB to 45.5 dB for TX in order to minimise the signal leakage from TX channel into RX channel. Due to its wide band nature, this SPDT switch can be used in X-band and Ku-band applications alike, making it very attractive for low-cost satellite communication systems. The possible use of PIN diode in passive attenuator topology has been discussed. The attenuator is expected to show accurate attenuation steps and maintain high linearity while keeping the power consumption low.

The new 4-bit PIN diode based phase shifter has also been presented in this thesis. It uses a hybrid high-pass/low-pass filter and bridged-T filter technology to steer the signal through phase delay path to achieve a desired shift. This phase shifter covers the entire 360° spectrum and has a resolution of 22.5°. While maintaining high linearity, the phase shifter has a current consumption of only 3.5 mA from 3.3 V source. The use of differential inductors in T-network topology results in reduced chip area which is critical for its incorporation into phased-array systems that use thousands of elements.

The presented SPDT switch, attenuator and phase shifter can be integrated with other sub-components of T/R modules and would provide for low-cost high-performing RF communication systems.

The future research in this field may be concentrated on the further improvements in isolation and insertion loss of custom designed PIN diode switch by studying the effects of device geometry. With the developments in fabrication technology, PIN diode should continue to provide for an easy integration in new low-voltage SoC applications.

BIBLIOGRAPHY

[1] X.Guan, “Microwave integrated phase array receivers in silicon”, Ph.D. Thesis, Caltech, 2005

[2] K. Koh, G. M. Rebeiz, “An X- and Ku-Band 8-Element Phased-Array Receiver in 0.18-um SiGe BiCMOS Technology,” IEEE J. Solid-state Circuits, vol. 43, no. 6, pp.1360 -1371, June. 2008

.

[3] D. Hoag, J. Brogle, T. Boles, D. Curcio and D. Russell, “Heterojunction PIN diode switch,” in IEEE MTT-S Int. Microwave Symp. Dig., Long Beach, CA, pp. 255- 258, 2003. Xiang Guan

.

[4] J. A. Torres and J. C. Freire, “Monolithic transistors SPST switch for L-band,” IEEE Trans. Microwave Theory Tech., vol. 50, no.1, pp. 51-56, Jan. 2002.

[5] P. Sun, P. Upadhyaya, D. Jeong, D. Heo and G. S. La Rue, “ A novel SiGe PIN diode SPST switch for broadband T/R module,” Microwave Wireless Compon. Lett., vol. 17, no.5, pp.352-354, May 2007.

[6] J. Li and K. K. O, “15-GHz Fully Integrated NMOS switches in 0.13-μm CMOS process,” IEEE J. Solid-State Circuits, vol.40, no. 11, pp. 2323-2328, Nov. 2005

.

[7] Y. Jin and C. Nguyen, “ Ultra-compact high-Linearity high- power fully integrated DC-20 GHz 0.18-μm CMOS T/R switch,” IEEE Trans. Microwave Theory and Tech., vol.55, no.1, pp.30- 36, Jan. 2007

.

[8] R. Ludwig, P. Bretchko. *RF Circuit Design-Theory and Applications.* Upper Saddle River, NJ, Prentice-Hall, Inc., 2000

[9] R. C. Jaeger, T. N. Blalock. *Microelectronic Circuit Design.* New York, McGraw-Hill, Inc., 2004

[10] W. E. Doherty, R. D. Joos. *The PIN Diode Circuit Designers' Handbook.* Watertown, MA, Microsemi Co., 1998

[11] P. Sun, P. Upadhyaya, A. Mikul, Y. You, D. Jeong, D. Heo, “Silicon-Based Low-Insertion Loss PIN SPST RF Switches,” submitted to International Symposium on Circuits and Systems.

[12] P. E. Allen, D. R. Holberg. *CMOS Analog Circuit Design, 2nd Ed.* New York, Oxford University Press, 2002

[13] P. Sun, “High Speed SiGe MMICs for Phased Array Communications”, Ph.D. Dissertation, WSU, 2008.

[14] L. Wang, P. Sun, M. Rajashekharaian, D. Heo, C. Champion, G. Lame, “A 15-GHz single-pole double-throw annular MOSFET switch for space application,” IEEE Workshop on Microelectronics and Electron Devices, pp. 103-106, Apr. 2005.

[15] Z. Li, K. Kenneth, “A 15-GHz Integrated CMOS Switch with 21.5-dBm P1dB and 1.8-dB Insertion Loss,” IEEE Symposium on VLSI Circuits, pp. 366-367, June 2004.

[16] I. Ju, Y. S. Noh, I. B. Yom, “Ultra Broadband DC to 40 GHz 5-bit pHEMT MMIC Digital Attenuator,” European Microwave Conference, vol. 2, Oct. 2005.

[17] H. Eom, K. Yang, “A 6-20 GHz compact multi-bit digital attenuator using InP/InGaAs PIN Diodes,” International Conference on InP and Related Materials, pp. 1-3, May 2008.

[18] C. F. Campbell and S. A. Brown, “A compact 5-bit phase-shifter MMIC for *K*-band satellite communication systems,” IEEE Trans. Microwave Theory Tech., vol. 48, no. 12, pp. 2652-2656, Dec. 2000.

[19] M. A. Morton, J. Papapolymerou, “5 bit, silicon-based, X-band phase shifter using a hybrid pi/t high-pass/low-pass topology,” IET Microw. Antennas Propag., vol. 2, issue. 1, pp. 19-22, Feb. 2008.

[20] T. M. Hancock and G. M. Rebeiz, “A 12-GHz SiGe Phase Shifter with Integrated LNA,” IEEE Tran. Microwave Theory and Tech., vol. 53, no. 3, pp. 977-983, March 2005.

[21] K. J. Koh and G. M. Rebeiz, “0.13-μm CMOS Phase Shifters for X-, Ku-, and K-Band Phased Arrays,” IEEE J. Solid-State Circuit., vol. 42, no. 11, pp. 2535-2546, Nov. 2007.

[22] J. P. Comeau, J. D. Cressler, M. Mitchell, J. Papapolymerou, “Sources of Phase Error and Design Considerations for Silicon-Based Monolithic High-Pass/Low-Pass Microwave Phase Shifters,” IEEE Trans. Microwave Theory and Tech., vol. 54, pp. 4032-4040, Dec. 2006.

[23] D.W. Kang and S. Hong, “A 4-bit CMOS Phase Shifter Using Distributed Active Switches,” IEEE Trans. Microwave Theory and Tech., vol. 55, no. 7, pp. 1476-1483, July 2007.

[24] R. Tayrani, M. A. Teshiba, G. M. Sakamoto, Q. Chaudhry, R. Alidio, Y. Kang, I. S. Ahmad, T. C. Cisco, M. Hauhe, “Broad-band SiGe MMICs for phased-array radar applications,” IEEE J. Solid-State Circuits, vol. 38, no. 9, pp. 1462-1470, Sep. 2003.

[25] P. Sun, P. Upadhyaya, D. Jeong, D. Heo, G. S. La Rue, “A Novel Monolithic SiGe PIN Diode SPST Switch for Broadband T/R Module,” IEEE Microwave and Wireless Components Letters, vol. 17, no. 5, pp. 352-354, May 2007.

[26] L. Wang, P. Sun, Y. You, A. Mikul, R. Bonebright, G. A. Kromholtz, and D. Heo, “Highly Linear Ku-band SiGe PIN Diode Phase Shifter in Standard SiGe BiCMOS Process”, accepted by IEEE Microwave and Wireless Components Letters.

[27] Spliced. “BMEWS solid-state phased-array radar at RAF Fylindales.” Online image. 1 October 2005. Wikimedia Commons. 2 October 2009. <http://commons.wikimedia.org>