A LOW NOISE LOW POWER DC-COUPLED SENSOR AMPLIFIER WITH OFFSET CANCELLATION

By

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To the Faculty of Washington State University:

The members of the Committee appointed to examine the thesis of HARI KRISHNAMURTHY find it satisfactory and recommend that it be accepted.

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ABSTRACT

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Modern research on studying animal behavior has a need for a variety of systems to record and analyze neural activities. This thesis involves the design of a DC-coupled low noise, low power sensor amplifier IC with DC offset cancellation. This chip consists of 16 independent channels which will be connected to multiple electrodes or an electrode array probing parts of the brain of the animal under study. Our application is mainly towards monitoring the neurological signals from mice without use of tether. This requires a wireless telemetry system with low mass and size. Each channel has amplification with programmable gain ranging from 20 to 2000 along with a filter. The power required per channel is about 1mW with a power supply of +/- 1 V. The bandwidth of each channel is 7kHz and has an input referred noise of about 0.495uV. A DC offset of up to +/- . 3 V can be canceled independently on each of the channels by adjusting the bulk voltages of the first stage amplifier.

The amplification is obtained across two stages, the first stage with a programmable gain from 10 to 50 and the second stage with a gain of 2, 16 or 40. These stages are followed by buffers which deliver the differential signals to the A/D converter.

An 8-bit resistor string DAC is used to control the bulk voltages of the input pair on the first stage amplifier to cancel the DC offset voltage. The DAC requires a bandgap reference of 1.5 V which is stable across temperature variations. The bandgap needs a higher voltage for its operation that is supplied by a charge pump PLL. The charge pump delivers a voltage of 3V which is sufficient to drive the bandgap. The chip was designed in the Jazz 0.18u CMOS process. Further improvement of the circuit to increase the offset cancellation to +/- 0.8 V would be helpful in some applications. One approach to accomplish this is to use voltages of 0, 0.5 and -0.5 in the feedback loop of the first stage amplifier.

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Dedicated to the memory of my grand parents and my family

who I love dearly.

CHAPTER ONE

1.1 BACKGROUND

Any electronic system to study real world phenomenon has an analog front end. Though most of the signal processing over the years has moved to the digital domain, the world at large is still analog and always will be. Analog circuits will therefore perform the vital role of interfacing electronic circuitry with the real world.

Biomedical research over the years has always had a need for multi-channel amplifiers to amplify the weak signals that are observed in different areas of research. Previous systems used for this purpose had many cables which burden small animal subjects, and have high power dissipation and/or high noise. This thesis project involves the development of a multi-channel integrated sensor IC with low noise, low power and DC cancellation to be used to detect and study the neural signals from the brain of mice.

Several other CMOS multi-channel integrated circuits have been used for the above stated purpose. These circuits either have very high power consumption or a high noise level[2] which will severely affect the accuracy of the signal being detected. High distortion[4] and large layout area[4] are also some disadvantages of comparable systems. Noise and power dissipation of some designs[3][4] are low but they lack programmable gain and use AC coupling which filters out low frequency components

The sensor amplifier design has a noise of 0.495uV with a gain of up to 2000. The DC offset at the input is 510.9uV for the first stage op-amp. This is without bulk adjustment with both the bulks of the input differential pair connected to the 1.5 volt supply from the DAC. The amplifier has a gain in the range of 20 to 2000. This is programmable and is split across the first two stages of the amplifier. The first stage has gains of 10, 25 and 50 while the second stage has positive and negative gains of 1, 8 and 20. The power consumption of the channel is about 900uW. The amplifier has DC offset cancellation upto +/- .3 volts. This is achieved by adjusting the bulk voltages of the input pair of transistors on the first stage of the amplifier. The bandwidth of the amplifier is from 0 to 7kHz. A charge pump was also designed to provide higher voltage supply to a bandgap reference. The bandgap reference voltage is required to allow the voltage reference for the resistor string DAC's to be 1.5V which is higher than the power supply voltage.

1.2 ORGANISATION

The thesis is split into six chapters. A general background of the project is discussed in chapter 1. Chapter 2 describes the previous version of the sensor amplifier followed by chapter 3 which explains the system architecture of the present design of the IC. The channel architecture is elaborated in chapter 4 followed by the simulation results in chapter 5. The final chapter talks about the future work and the layout complications involved in the design of the Integrated circuit.

CHAPTER TWO

2.1 SENSOR AMPLIFIER

The present version of the amplifier design is an improvement on the previous version designed and fabricated in the TSMC 0.25u process. The system level architecture of the previous version of the chip is shown below[9].

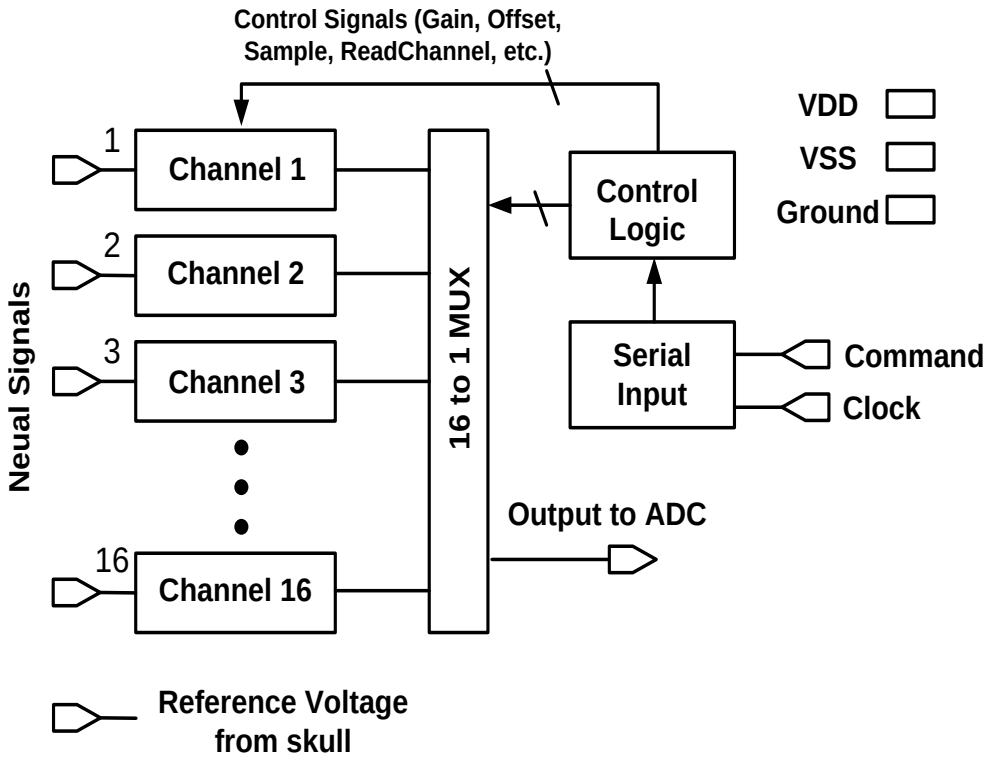

Figure 1 System architecture of sensor amplifier I

There are 16 channels in this design and each channel is used to amplify, filter and sample the signals. A multiplexer(MUX) is used to select the channel to be output to the analog to digital converter (ADC). A digital control circuit based on a state machine was used to setup each channel's mode of operation and also control the MUX to select the channel that was to be read by the ADC.

The amplifier component of the above architecture consisted of 3 stages of gain as shown below. This was followed by a filter and a track-and-hold circuit whose output goes to the MUX.

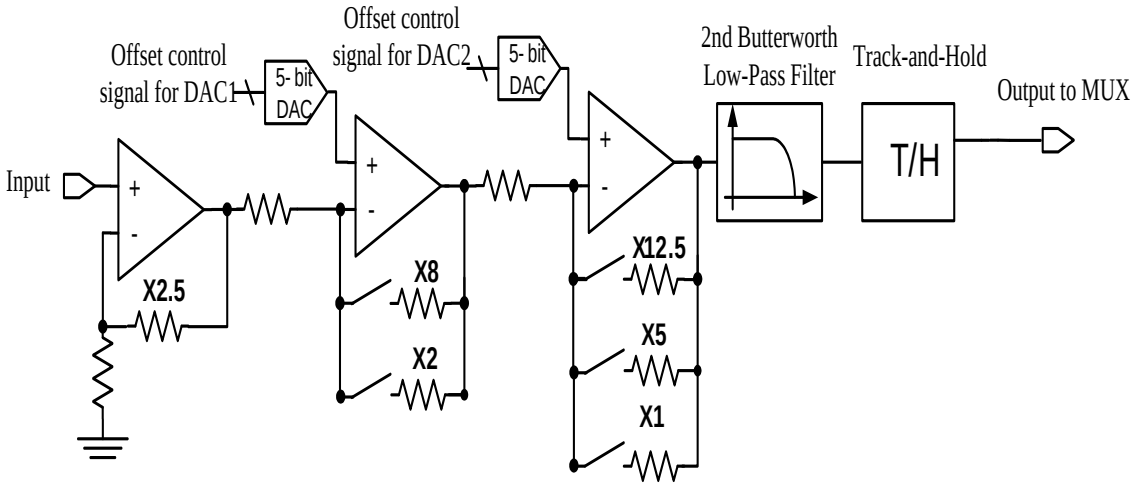

Figure 2 Channel architecture of sensor amplifier I

The disadvantage of the above design was the use of 3 stages to achieve a gain of 250. Also the DAC's used for the DC offset cancellation are at the input of the second and third stages and changing the gain of the second stage changes the offset voltage. Also, since the

gain of the first stage is only 2.5, the DAC noise must be kept low. The programmable gain is achieved by connecting different resistors to the feedback loops of the op-amps. The signal is passed through a low pass filter and the track-and-hold before proceeding to the MUX which selected the channel to be output to an ADC.

2.2 CHOPPER AMPLIFIER TECHNIQUE

An improvement suggested to the previous design was the use of a chopper amplifier[9]. The chopping amplifier was employed to reduce the flicker noise of the circuit. The chopper stabilization technique uses the basic idea of modulating the signals to higher frequencies where there is much less flicker noise. This signal is then amplified and demodulated by an output chopper to lower frequencies. The output chopper will raise the DC offset and the flicker noise to higher frequencies. A filter can then be used to remove the unwanted components of noise and offset. The chopper amplifier architecture is shown below.

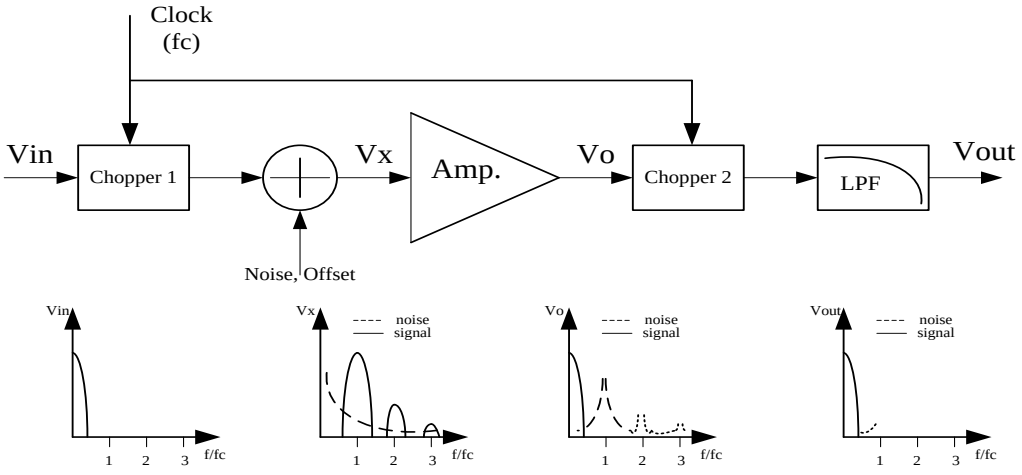

Figure 3 Chopper Amplification Technique

One major advantage of this design was having DC cancellation in the first stage. This allows a higher minimum gain on the first stage, which reduces the contributions of noise from subsequent stages. The schematic of the chopper amplifier is shown below. The chopping of the signals takes place at the drains of the transistors and the output is single ended. Conventional choppers chop at differential inputs and outputs unlike the one used in this design. The chopping frequency chosen must meet the Nyquist criterion ie the chopping frequency should be at least twice the frequency of the highest frequency component in the signal being sampled.

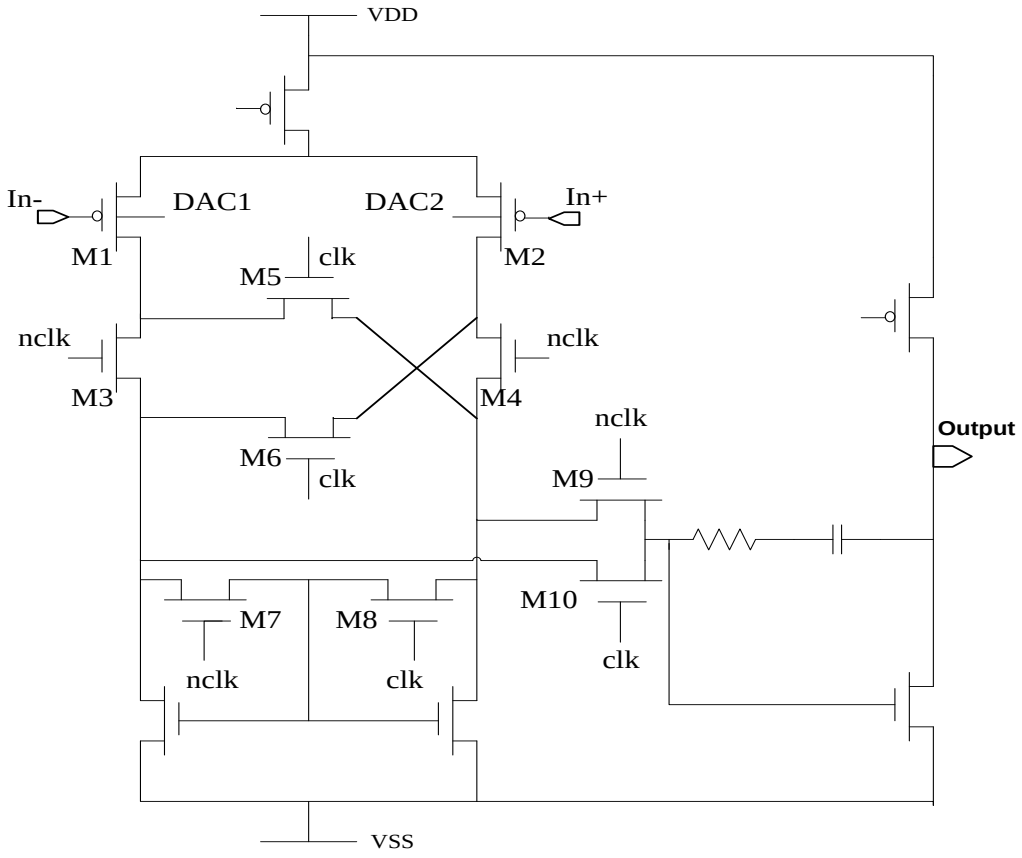

Figure 4 Chopper Amplifier

The bulk nodes of the input pairs are connected to DAC's which are used to set the voltages at these nodes. By varying the bulk voltages the DC offset of the incoming signal can be adjusted up to +/- .3V

The chopper amplifier was designed and simulated. Instead of a chopping amplifier a source degenerated load on the first stage gave similar noise figures and hence the chopper amplifier technique was shelved. The new design using source degeneration is discussed in the next chapter.

CHAPTER THREE

3.1 SENSOR AMPLIFIER II

Several requirements were to be met for the design of the latest version multi-channel sensor amplifier used to study neurological signals in the brain of mice. The key features of this design include :

1. Bulk adjusted DC offset cancellation.
2. High-linearity DAC's
3. Use of source degeneration instead of chopping.
4. Design of the analog filter
5. Design of bandgap reference
6. Design of Charge Pump

The sensor amplifier system architecture is shown below.

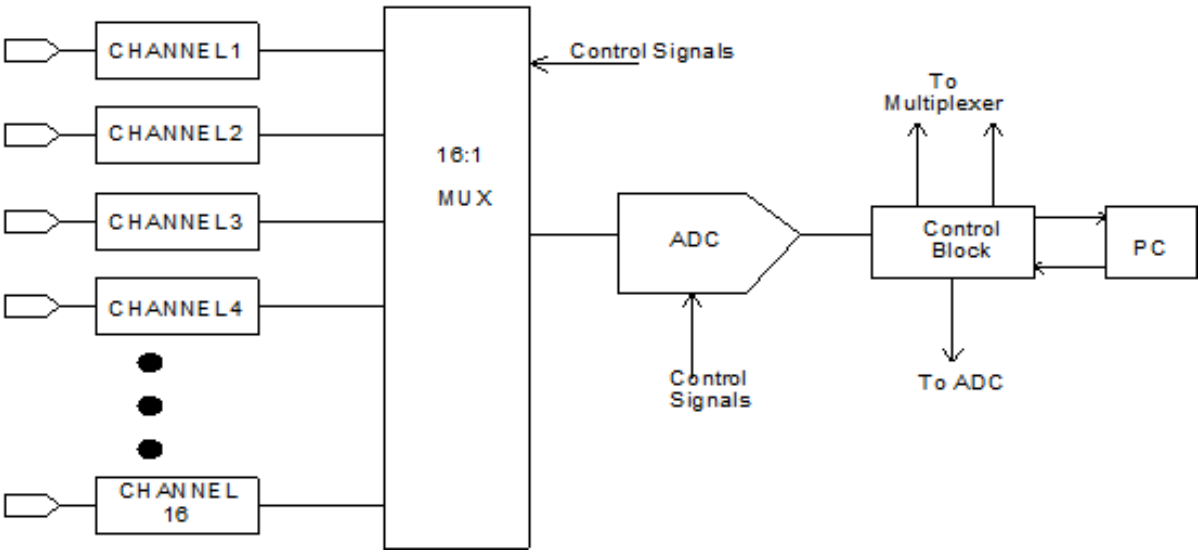

Figure 5 System architecture of sensor amplifier II

Op-Amp Characterization And Design Issues

3.1.1 DC Offset Cancellation

The multiple electrode arrays used to study the neural signals use the skull as a reference site. This leads to DC offset errors upto +/- 0.3volts in the signal. Most of the multichannel IC's in the market employ AC coupling to get rid of the DC offset. However this technique usually leads to the use of large off-chip capacitors to provide a low enough cut-off frequency besides leading to filtering out of certain low frequency components. The current design described in this thesis uses a bulk adjustment technique to remove the DC offset.

The input pair of transistors on the first stage op-amps have bulks which are connected to a resistor string DAC. By setting the voltages at the bulks of the input pairs we can remove the DC Offset associated with the incoming signal. The voltages at both the bulks are adjusted to remove the DC Offset. Course adjustment of DC cancellation is met at one of the transistors bulk while the bulk of the other transistor is used to make fine adjustments. The bulk adjustments and the design of the resistor string DAC's are explained in detail later. Since the DC Offset is removed in the first stage Op Amp it is possible to have a higher minimum gain of 10 on this stage. This aids in reducing the total number of stages from three in the previous design to two in the current design.

3.1.2 Programmable Gain

The total gain required from the channel is from 20 to 2000. To achieve this the gain is

split across the first two stages of the channel. The first stage has programmable gains of 10, 25 and 50. The second stage has programmable gains of 2, 16 and 40. The different gains are achieved by transmission gate switches to change the feedback resistors that are connected to the output of the Op Amp. The DC offset cancellation allows the gain of the first stage to be increased to minimize noise contributions from other stages.

3.1.3 Noise Contribution

The Noise contribution of the first stage Op Amp is shown below. The design of the first stage Op Amp with low noise was critical due to the high gain of this stage. The interface between silicon and gate oxide in MOS transistors has several incomplete bonds which 'trap' charge carriers and later release them leading to flicker noise. Flicker noise is commonly referred to as 1/f noise since it inversely proportional to the frequency of operation of a circuit. The flicker noise is given by $K/(\mathrm{Cox} \bullet WLf)$, where K is the process-dependent constant, W and L are channel width and length respectively[1]. Flicker noise can be reduced by having a larger active area. Since the first stage is the main noise contributor it is required that the flicker noise from the input pair is small at the expense of a larger active area. Hence the input pairs of transistors are made large to make the channel low noise. PMOS devices have holes as the majority charge carriers in a buried channel at a further distance from the oxide-silicon interface. This results in PMOS devices exhibiting lower flicker noise which is the reason they were selected as the input pair of the first stage op-amp.

Another important contributor to the noise of the circuit are the resistors in the DAC used for bulk adjustment. The previous version of the sensor amplifier had a DAC connected to one of the inputs of the op-amp and hence the noise from the DAC was amplified along with the signal. However in the present design the DACs are connected to the bulk and do not experience as much gain as the previously design. The current through the DACs was increased and lower value resistor's were used to implement the DAC in order to lower their noise contribution.

The 2^{nd} order Butterworth filter was removed and a simple RC filter was used to bring down the power. This helped to lower the power of the system since there was one less op-amp in the channel. Using source degeneration also helped to lower the noise from the active loads in the first stage of the primary stage op-amp.

The noise requirement for the latest design was to have an input-referred noise from 1Hz to 7KHz of .5μV. This is much lower than previous designs which had requirements of 2μV and 1.4μV . Since the power dissipation of this design was lower than the previous designs, the current of the first stage could be increased and still have power dissipation of less than 1mW per channel. The integrated input referred noise of this design was simulated at 0.49uV at the input with zero offset and a channel gain of 2000.

3.1.4 Power Consumption

The sensor amplifier is a part of the system that is to be used to study the brain of mice.

Though the current version of the system is powered by a tether, the final goal is to power the system remotely with no tether.

It is therefore very important to have a low power sensor amplifier to reduce the overall power of the system. In addition power dissipation should be low enough so as not to bother the mouse. However since there is a low noise requirement a trade-off has to be made with the power consumption.

Techniques like sharing of bias circuits and use of a single bandgap generator to power all the DAC's are used to reduce the power consumption.

3.1.5 Power Supplies

The power supplies used in the Jazz 0.18um CMOS process are +/-1 volts. This presents a problem since the bulks of the input transistors need to be higher than the power supply rails with a maximum DAC voltage of 1.5 volts. A charge pump was designed to provide a supply for the bandgap which generates the reference voltage of 1.5 volts instead of using an external regulator and using an extra pin on the chip package. The design of the charge pump is explained in later sections.

3.1.6 Linearity

Linearity is one of the important requirements of the sensor amplifier. The resistors, capacitors, switches and Op amp's all contribute to the non-linearity of the system. The Op

Amp's should be designed with very high open loop gain to have high linearity. The linearity of the Op Amp is essential for proper gain linearity and hence good performance of the circuit. Other components for the design are chosen based on their linearity characteristics. For instance poly resistors and MIM capacitors which offer good linearity are used in the layout. The linearity of the channel is characterized by the total harmonic distortion (THD) shown in the simulations section.

CHAPTER FOUR

4.1 CHANNEL ARCHITECTURE

The channel design of the sensor amplifier was optimized after the trade offs between several designs were met. The components of the channel are :

1. First gain stage with offset cancellation
2. Second Gain Stage comprising of inverting and non-inverting stages
3. Analog Filter.
4. Bandgap Reference
5. Charge Pump
6. Resistor String DAC

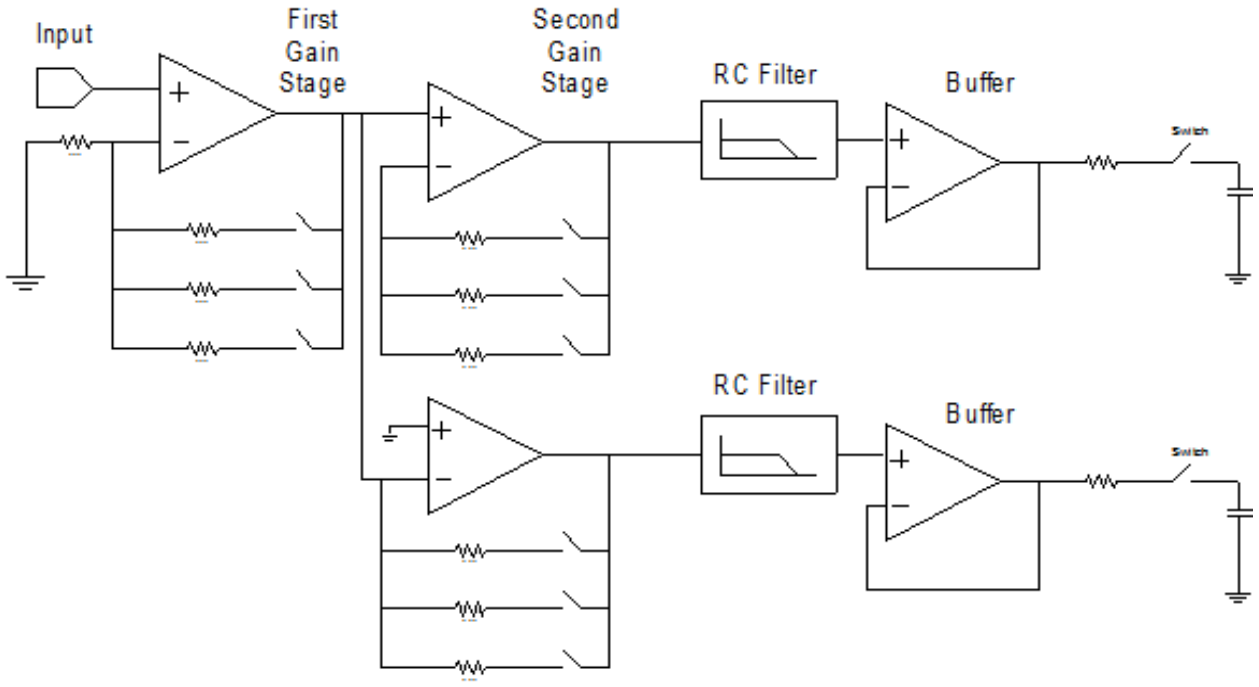

Figure 6 Channel Architecture of Sensor Amplifier II

4.1.1 First Gain Stage with Offset Cancellation

The first gain stage of the Op Amp has the DC Offset cancellation and programmable gain of 10,25 and 50. The DC Offset cancellation was achieved by controlling the bulk voltages of the input pair of transistors. The voltage of the bulk's of the input pair were varied using a 5 bit decoder and resistor string DAC. A switching matrix is used with the decoder to set the appropriate voltage to each of the bulk terminals. The programmable gain is achieved by connecting different resistors to the feedback loop using FET switches.

The input pair of the first stage Op Amp is a set of PFET's with isolated bulks. Since the DC Offset cancellation is moved to the first stage of the Op Amp the minimum gain on the first stage is increased to 10 which will hence make the noise of this stage dominate the noise of the channel. The flicker noise from the input pair dominates the noise of the first stage and therefore of the entire channel. To reduce the flicker noise the input pair of transistors are made as large as possible. The trade-off with area of the chip determines the size of the input pair. Care should also be taken when the input pair of transistors are laid out. Since they are very large they should be laid out in common centroid so that they have proper matching and do not have inherent offsets. The layout of the input pair will be discussed later.

The DAC consists of course adjustment resistors as well as fine adjustment resistors. A single resistor string is used to obtain the voltages required to bias both the bulks. A set of switches along with a decoder are used to obtain these DAC voltages. The architecture of

the DAC and the decoders will be discussed subsequently. Depending on whether the DC offset is positive or negative the fine resistor string voltage and the coarse resistor string voltage will be applied to the respective bulks.

The first gain stage Op Amp is shown in Figure 7.

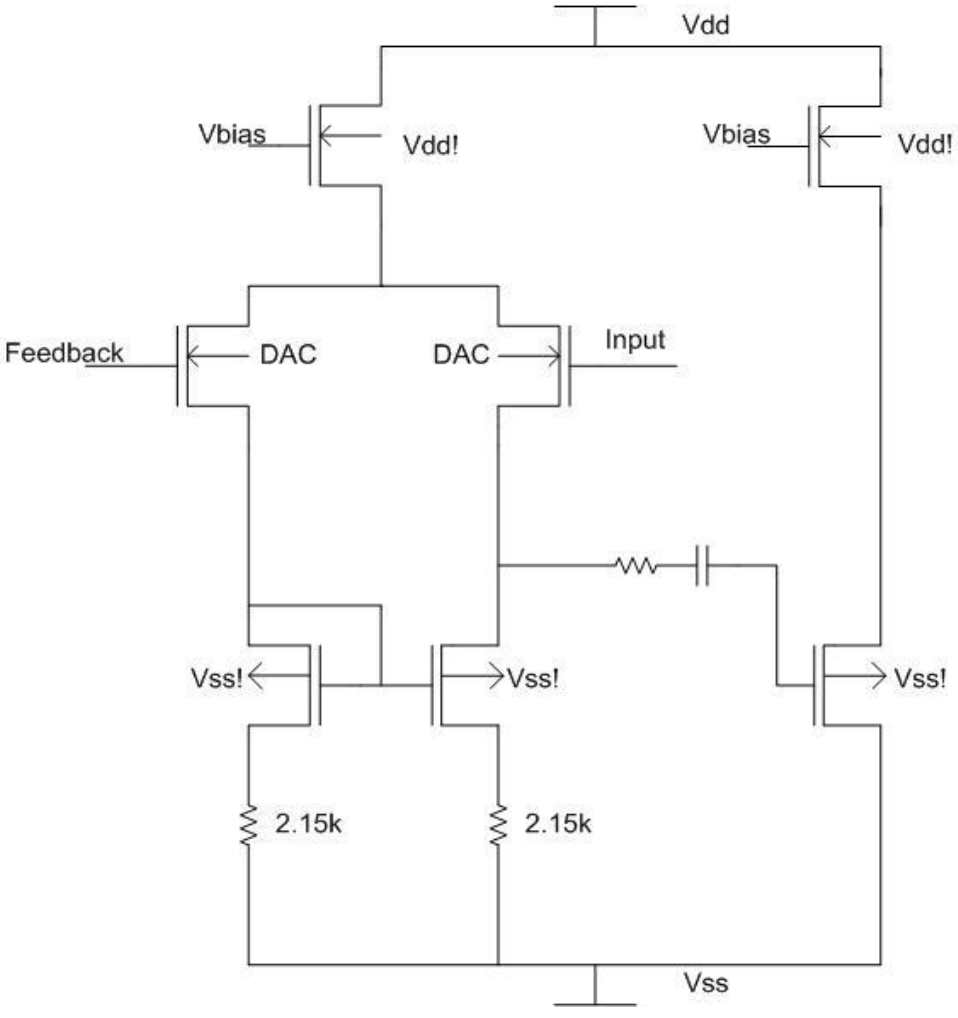

Figure 7 First Gain Stage Op-Amp with DC Cancellation

Linearity of the Op Amp is essential for any good amplifier. In order to have very high linearity the DC gain of the Op Amp is made very high. The DC gain of the Op Amp in the first stage is above 100dB. Adequate phase compensation is provided using a resistor and a capacitor to provide a phase margin of atleast 60 degrees on the first stage. The simulation results for the phase margin, gain margin, DC gain of the first stage Op Amp are shown in the simulation results.

4.1.2 Second Gain Stage

The second gain stage of the channel is essentially for amplification. The first gain stage branches off into two amplifiers in closed loop configuration with positive and negative gains, providing an additional gain of 2. Each of them has gains of 1, 8 and 20. Combined with the programmable gain of 10, 25 and 50 of the first stage, the differential channel gain is variable from 20 up to a 2000. Since the gain of the first stage is at least 10 and the noise contribution of the second stage is not critical the second stage op-amp power can be low and hence help in maintaining a low overall power for the entire channel.

The Op Amp's used in this stage have NFET's as input pairs. The PFET's are used in the first stage to reduce the flicker noise however in the second stage a higher input common mode range is needed. The residual offset which is not entirely canceled by the bulk voltage mismatches and results in a common mode voltage being applied to the second op-amp. Thus an NFET input stage was chosen.

In the previous design the first stage of the Op Amp had a gain of just 2.5 and the overall gain requirement was 250, since the gain of a 100 could not be achieved in the second stage alone the previous design had 3 gain stages. This resulted in the use of 3 Op Amps for the gain stage and higher power dissipation. The present design has offset cancellation on the first stage and the gain requirement of the channel is met in the first two stages removing the need for a third gain stage. The Op Amp used in the second gain is shown in Figure 8.

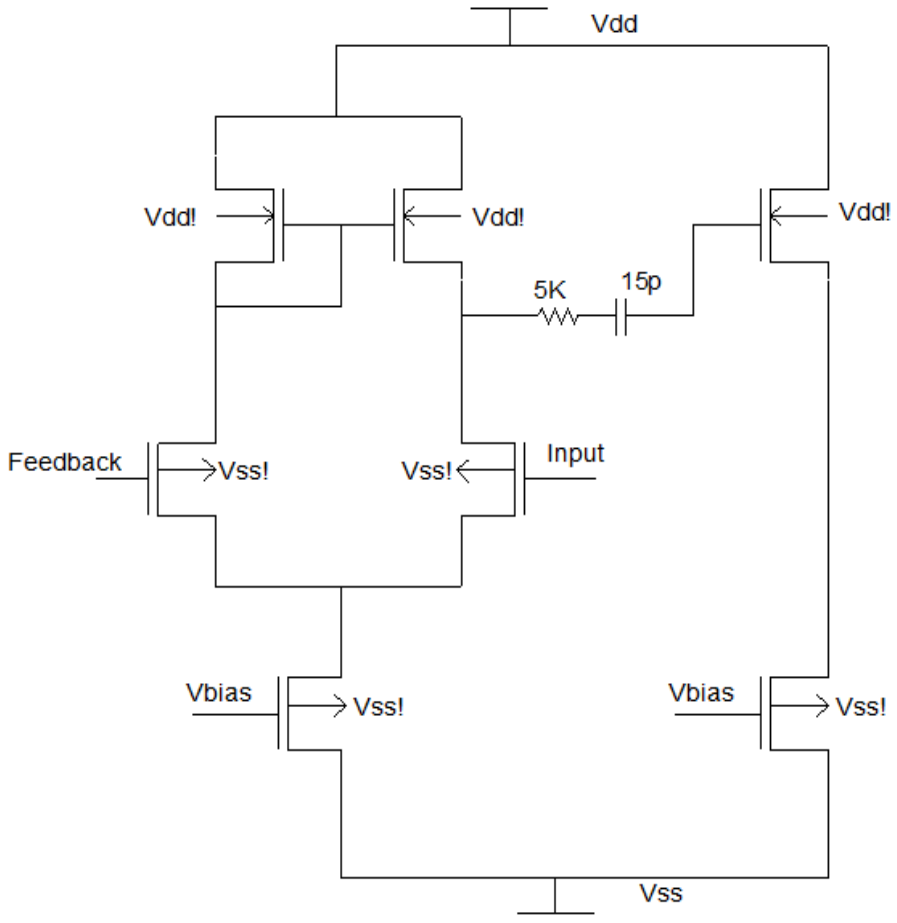

Figure 8 Second Gain Stage Op-Amp

Linearity is important for the Op Amp in the second amplification stage as well. Hence the Op Amp is designed with a very high DC gain of over 90dB. Adequate phase compensation is provided to have a phase margin over 55 degrees. The simulation section shows the DC gain, phase and gain margin of the second stage Op Amp.

4.1.3 Low Pass Filter design

The signal which are to be processed by the system has a maximum frequency of 7Khz. A low pass analog filter with a cutoff frequency of 7KHz is used. The signals after amplification are passed through low pass filter's to reduce the wide band noise and remove other spurious signals that are present in the individual channels. Initially a 2^{nd} order Butterworth filter was designed and implemented. The block diagram of the filter is shown in Figure 9.

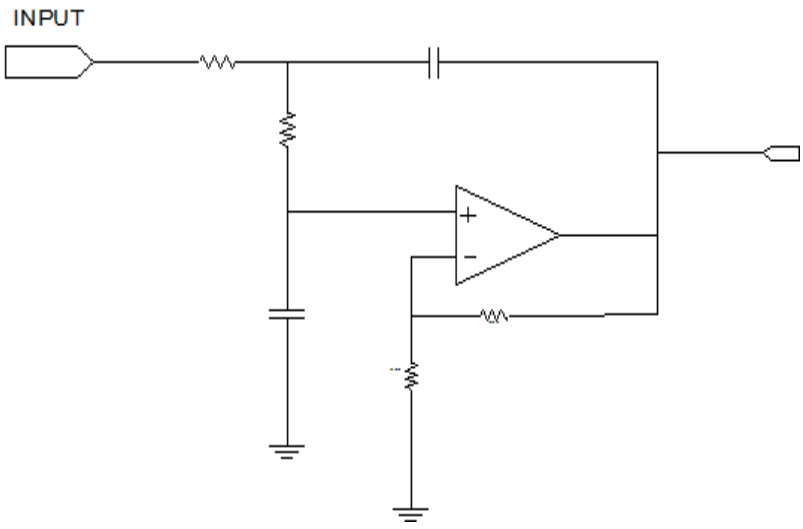

Figure 9 Butterworth Filter

The Butterworth filter had a gain of 10 and positive and negative inverting buffers were used to produce the differential signals after passing through the Butterworth filter. This proposed design had a gain of 50 on the first stage and a constant gain of 10 on the Butterworth filter which acted as the second gain stage in addition to filtering the incoming signals. Changes in the design requirements pushing the total gain of the channel to a maximum of 2000 resulted in removing the 2^{nd} order Butterworth filter from the channel and replacing it with a simple RC filter. The second stage was now replaced with two Op Amp's with positive and negative programmable gains.

The Butterworth filter was replaced with a simple RC filter. The RC filter has a cut off frequency of $1/(2\pi RC)$. The value of the capacitor is picked and then depending on the cut off frequency required the value of the resistor is chosen. For the cut off frequency of 7KHz a value of 100p was chosen for the capacitor and the value of resistor was hence calculated to be approximately 227K. A simple RC filter is shown in Figure 10.

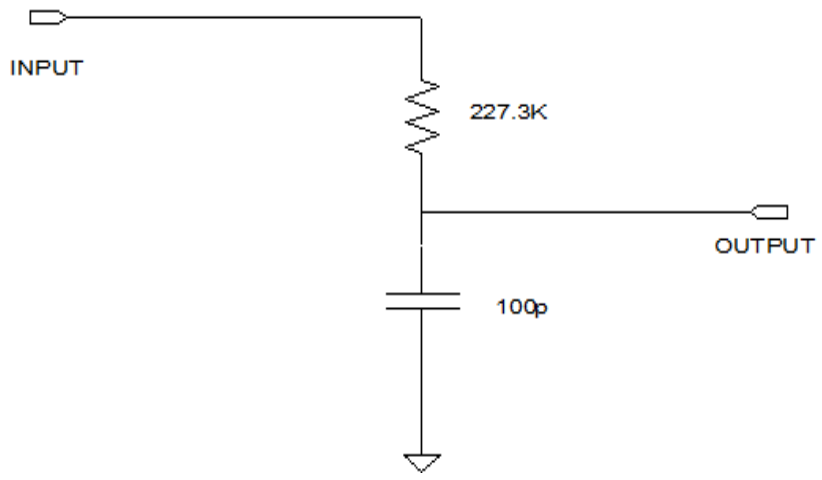

Figure 10 RC Filter

4.1.4 Resistor String DAC's

The resistor string DAC's are used to set the voltages at the bulk terminals of the input pair on the first gain stage of the channel. A pseudo 10 bit resistor string DAC is implemented by connecting 32 fine adjustment resistors to 32 coarse adjustment resistors in series. A five bit decoder connected to 32 switches is then used to obtain a specific voltage level from the fine resistor string and coarse resistor string separately. Depending on the offset being positive or negative, the coarse and the fine resistor string voltages will be connected to the bulks of the input pair of the Op Amp.

The resistors in the DAC make a significant contribution to the noise of the entire channel. The values of the resistors are chosen so as to maintain a good trade off between the noise contribution and power consumption due to the resistor string.

Resistor string DAC's are easy to implement and are high speed which make them suitable for our implementation. Switches used to deliver the DAC voltage are made sufficiently large to reduce their noise contribution. The block diagram of the DAC is shown in Figure 11.

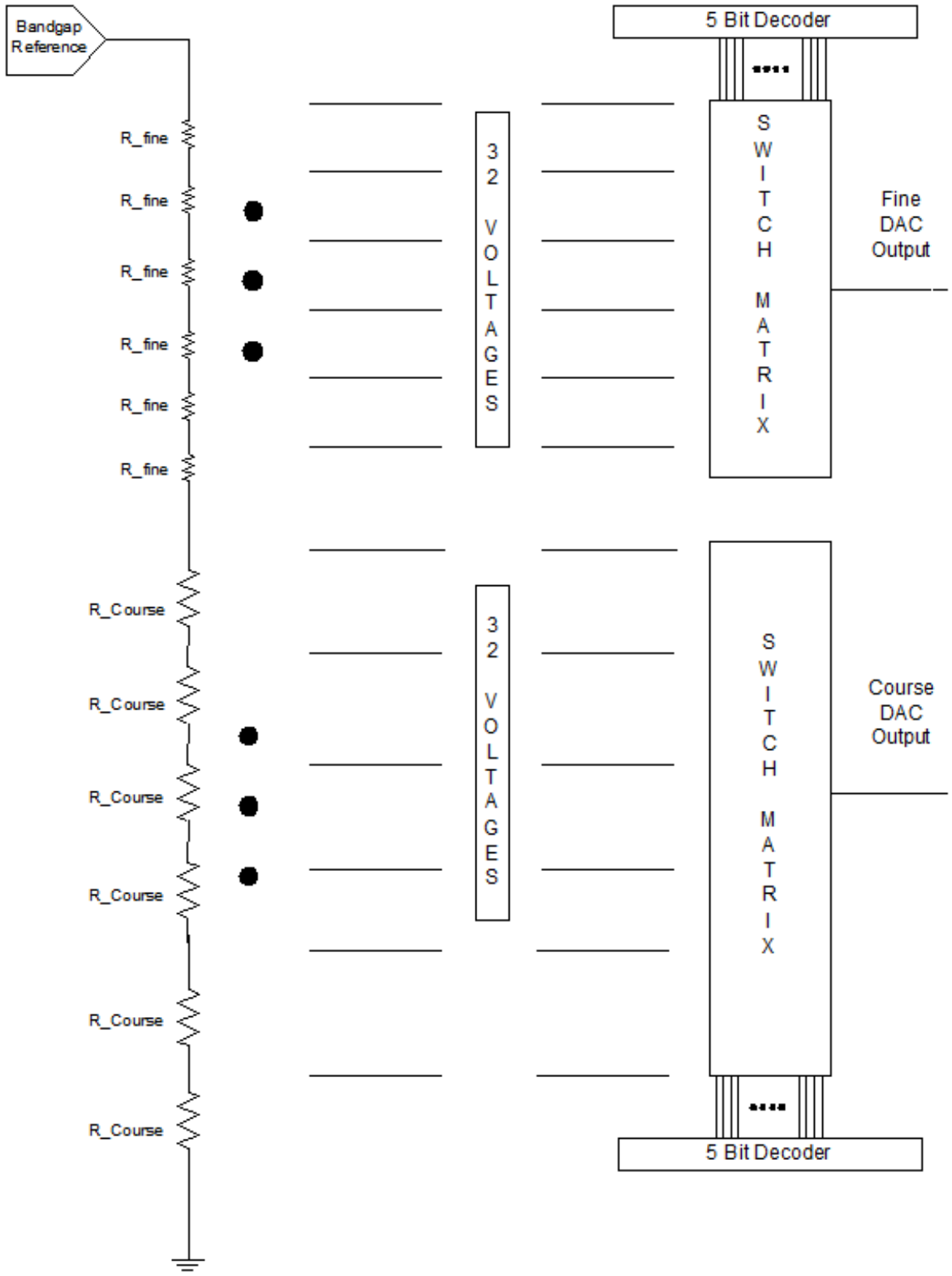

Figure 11 Resistor String DAC and 5-Bit Decoder's

4.1.5 Bandgap Reference

A bandgap voltage reference is used to provide a constant reference voltage to the resistor string DAC used to bias the bulk nodes of the input pair. A Bandgap voltage reference is often used when there is a need for biasing circuits or to provide a reference to which other voltages are compared.

The main criterion for implementation of a Bandgap is that it exhibits little dependence on temperature and power supply voltages. This is achieved by balancing the positive temperature co-efficient of the differences in the base-emitter voltages of the Bi-polar FET's and the forward bias voltage of the individual BJT's which have a negative temperature co-efficient. The PSR of the bandgap is more than 60dB, this would dampen any fluctuation in the power supply by a factor of 1000 before affecting the output of the bandgap. The PSR of the bandgap is shown in the simulations section.

The reference voltage required for our design is 1.5 V. The supply voltage Vdd required for the operation of the Bandgap is provided using a charge pump. A single Bandgap reference is used to provide the voltage with the required current to drive all the resistor string DAC's used in the 16 channels. Since a charge pump is used to power the Bandgap reference it must be designed so as to provide sufficient current to the Bandgap to drive a very low resistance. This resistance would be equivalent resistance of 16 resistor string DAC's in parallel.

The design of the charge pump is explained in the following section. The temperature independent output of the Bandgap is simulated and included in the simulation section. The architecture of the Bandgap reference is shown in Figure 12. A start-up circuit was also implemented to prevent any lock up conditions that might prevent the Bandgap from producing the required reference voltage.

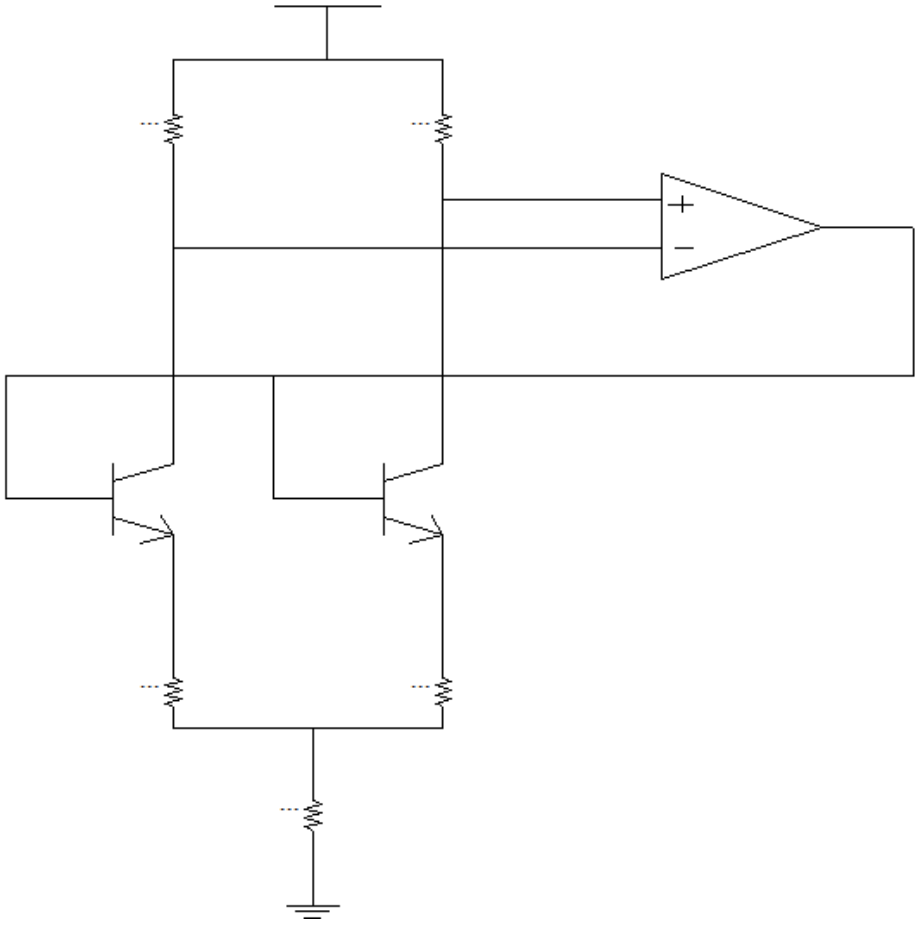

Figure 12 Bandgap Reference Genarator

4.1.6 Charge Pump

A voltage higher than the upper supply was needed. A charge pump voltage doubler was chosen to power the Bandgap reference. A switched capacitor topology was used to realize the charge pump. A simplified diagram of the charge pump is shown in Figure 13.

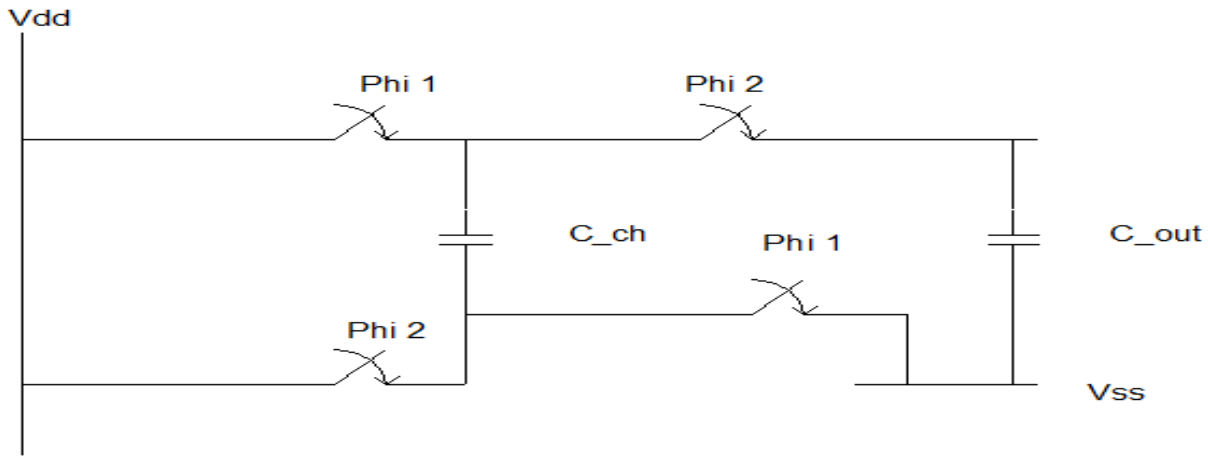

Figure 13 Model of Charge Pump

During the initial clock phase phi1 the capacitor C_ch is charged between Vdd and Vss. During the clock phase of phi 2 the bottom plate of C_ch is moved to Vss from Vdd and hence the charge on the top plate increases to 2Vdd-Vss. The difference between the plates is then passed on to C_out. After several clock cycles the required voltage output across the capacitor C_out is obtained.

The actual realization of the circuit is shown in Figure 14. The clock voltages required for the top two transistors must be higher since they drive higher voltages. Those clocks are generated using the clock generation circuit that is depicted in the Figure 15. The simulation results indicating the functioning of the charge pump is shown in the

simulations section.

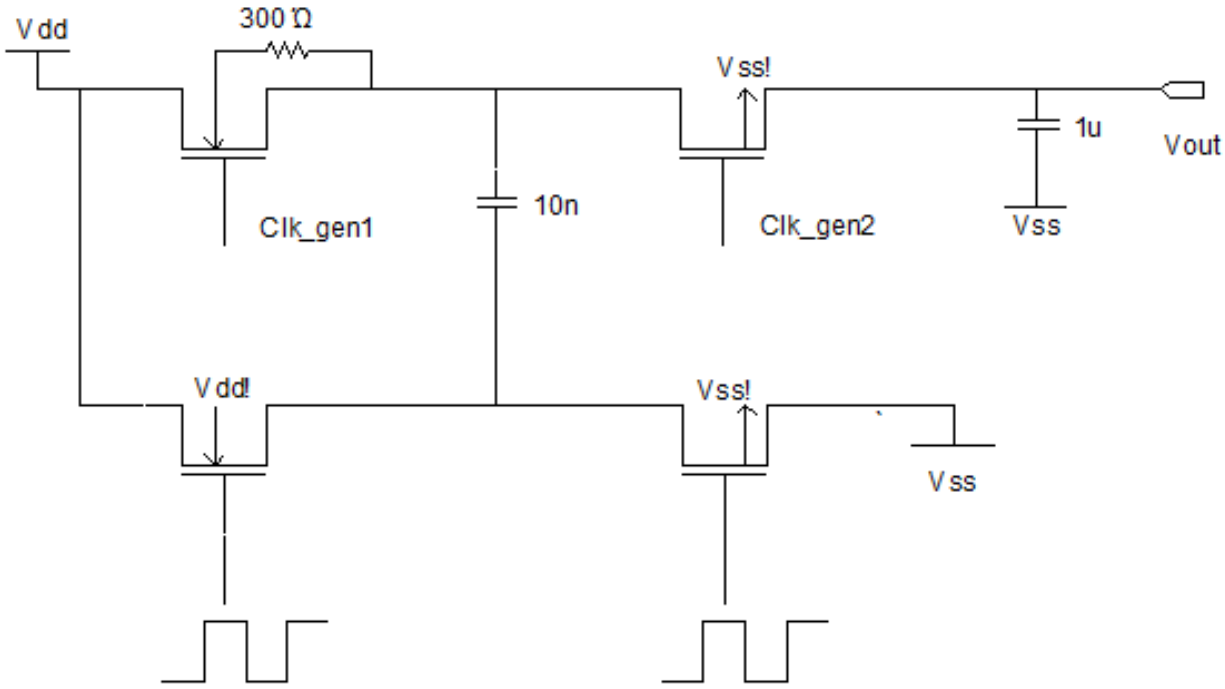

Figure 14 Charge Pump Schematic

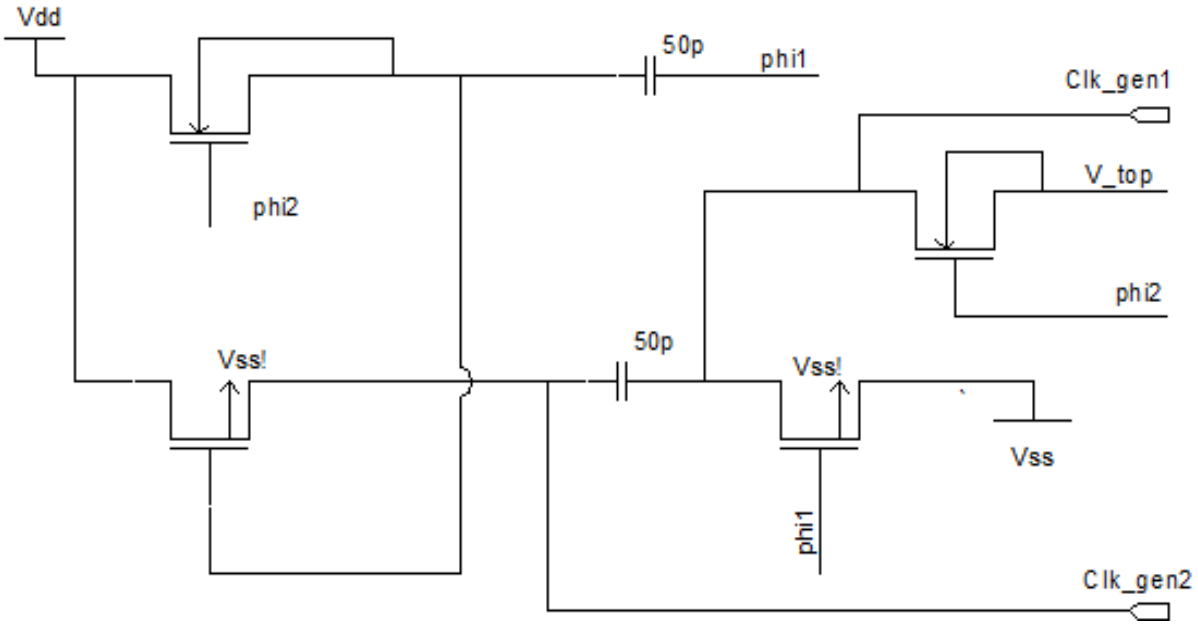

Figure 15 High Voltage Clock Genarator

CHAPTER FIVE

SIMULATIONS

5.1 Op Amp Characteristics

The DC gain plot and the phase margin of the Op Amp used in the first gain stage are shown in Figure 16. The Op Amp is in the open loop configuration. An AC source is placed at the input to the Op Amp and the gain at the output is measured using AC analysis. The offset voltage of the Op Amp is applied as a DC voltage along with the AC source.

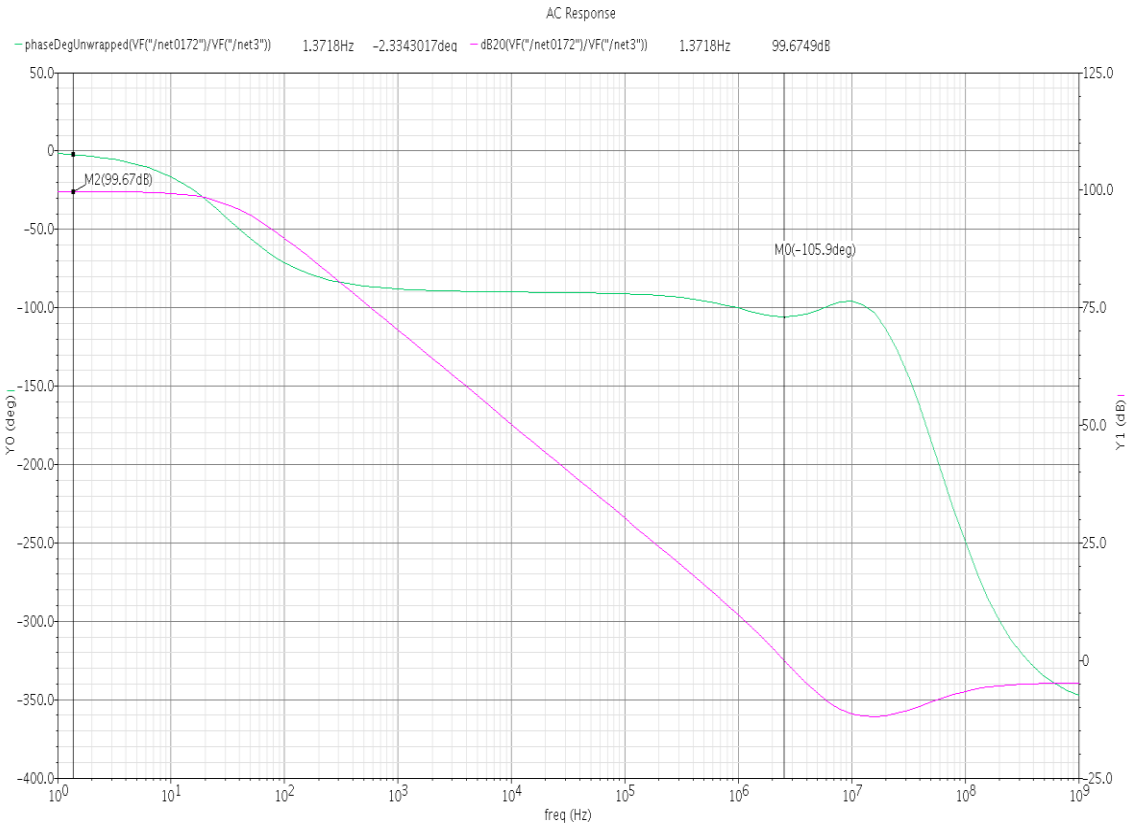

Figure 16 AC Response of First Gain Stage Op-Amp

The power supply rejection ratio(PSRR) is an important parameter to gauge the noise rejection of the Op Amp (supply noise).

The PSRR is defined as the difference between the gain from the input to the output and the gain from the supply to the output with the gain being in dB. It is important to have an high PSRR because the supply lines are generally noisy and it is essential that the Op Amp rejects this noise. The PSRR of the Op Amp used in the first gain stage is shown in Figure 17. The DC gain plots from the input to the output and from the supply to the output are first made and then their difference taken to obtain the PSRR+ plot.

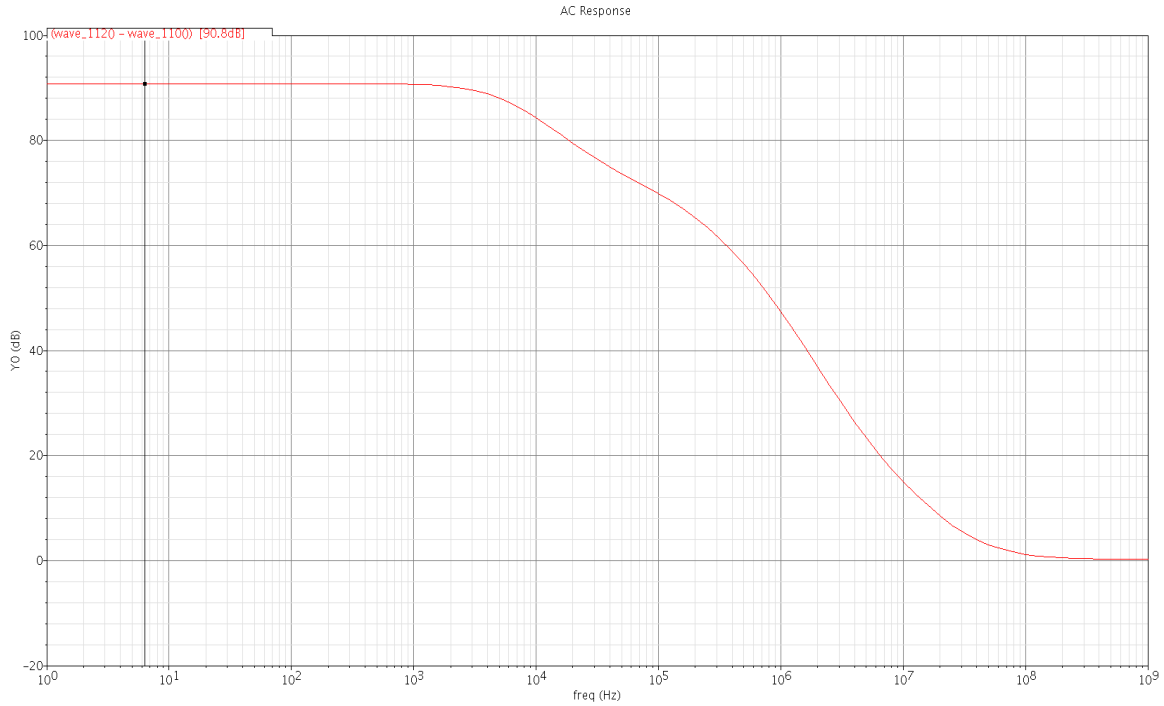

Figure 17 PSRR+ of First Gain Stage Op-Amp

The Op Amp gain from input to output and vdd to output are shown in Figure 18.

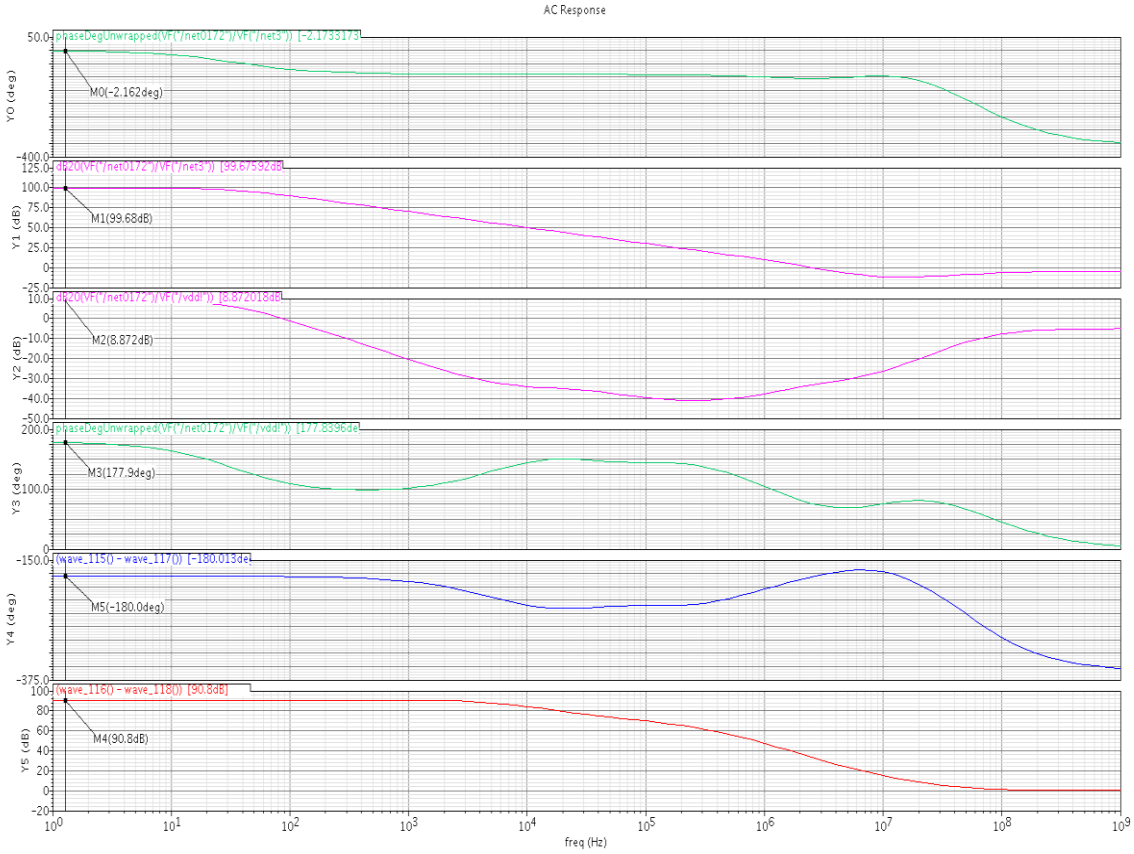

Figure 18 Gain and PSRR Computation

The PSRR+ is the power supply rejection from Vdd. In a method similar to the above the PSRR- which represents the power supply rejection from the terminal VSS is found. The plot of the PSRR- is shown in Figure 19.

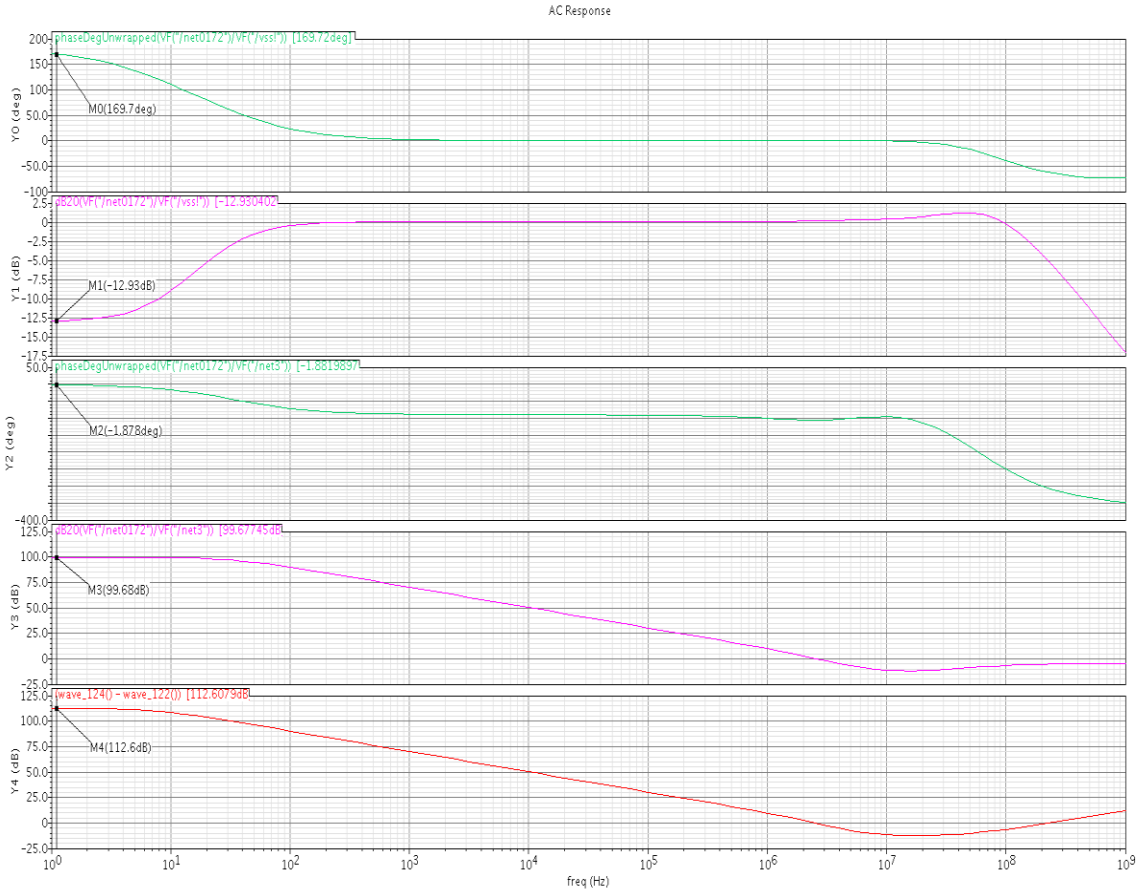

Figure 19 PSRR- of the First Stage Op-Amp

The Characteristics of the second stage Op Amp are also shown in Figure 20. The simulation setup is similar to that of the first Op Amp. The second Op Amp has a high DC gain of 90 dB and has high linearity. High power supply rejection in the first stage was realised with PSRR+ above 90dB and PSRR- above 110dB. This ensures the op-amp works optimally in the event of power supply fluctuations.

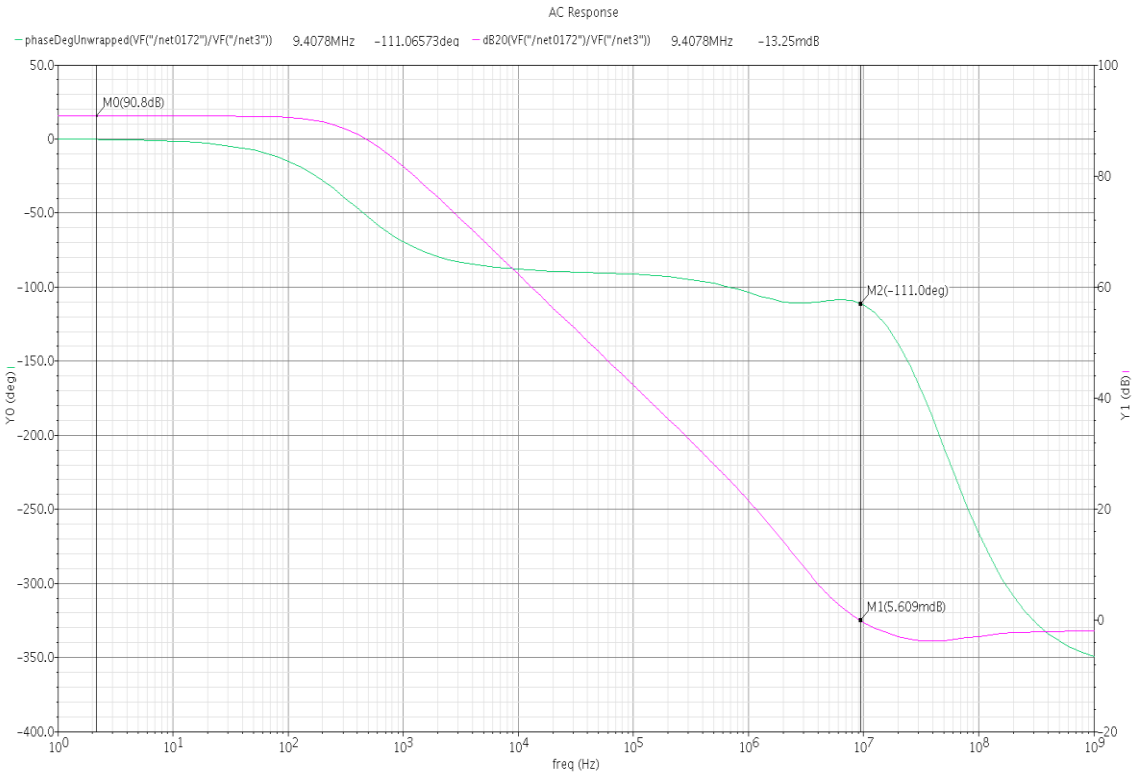

Figure 20 AC Response of Second Stage Op-Amp

5.2 Noise Characteristics

The noise performance of the channel is analyzed with varying gain and varying offsets. The analysis with varying gain is presented first. The input offset was set to zero and Vos was applied to the input of the Op Amp. The input offset voltage(Vos) is the voltage required at the input of an op-amp to obtain a zero output. The table below shows the total noise and the integrated input referred noise of the channel from 1Hz to 1GHz varying with the different programmable gains.

The main noise contributors are the input pair of transistors, the resistors in the DAC and the bandgap that is used to provide the reference for the DAC's. The input referred noise is obtained by dividing the total noise at the output by the gain of the channel. It can be

observed that the input referred noise is decreasing with increasing gain, the noise is the least for the highest gain of the channel.

Table 1 Noise Vs Programmable gain

Gain	Noise(in uV)	Input Referred Noise(in uV)
20	21.6	1.079
50	32.2	0.6434
100	53.5	0.5346
160	102.6	0.6412
400	252.6	0.6316
800	399.3	0.4990
1000	533.2	0.5332
2000	991.1	0.4955

To achieve a high dynamic range and good accuracy a lower input referred noise is required. Several techniques are discussed to lower the noise in the channel in the previous sections.

The input frequency to the amplifier is low so flicker noise dominates. The noise plot of the channel is shown in Figure 21. The integrated noise of the channel is measured from 1Hz to 1 GHz. The general upper limit to integrate the noise is 1.2 times the corner frequency.

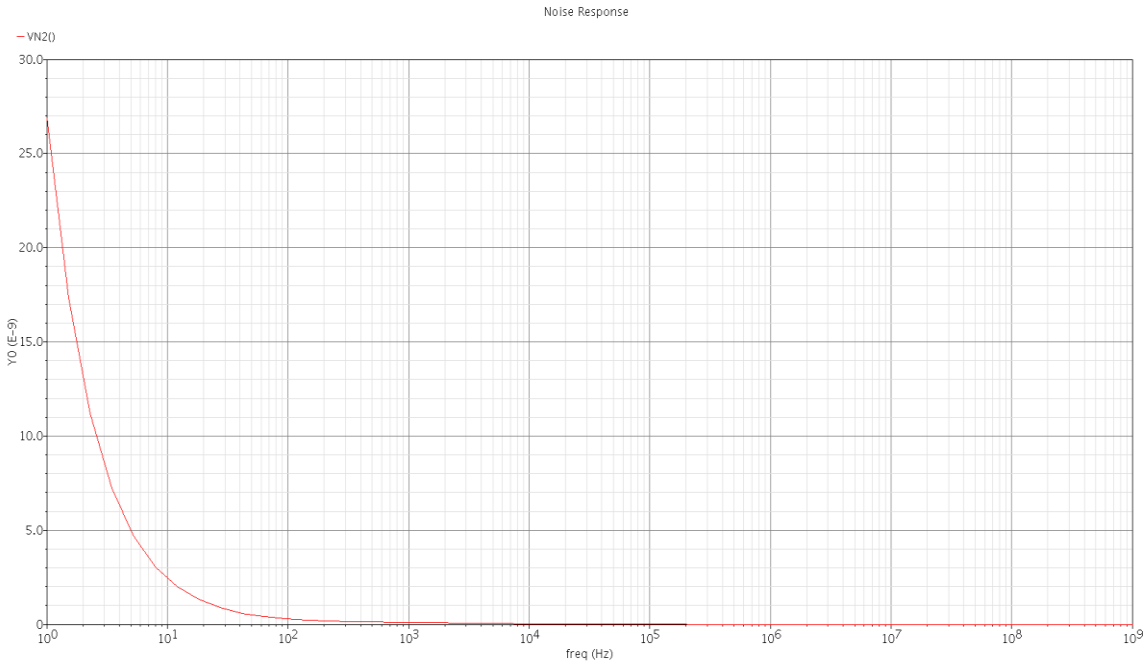

Figure 21 Noise Response

The following table (in Figure 22) is the integrated noise of the channel from 1 Hz to 1GHz. The top 20 parameters contributing to the noise of the channel are listed. This table represents the noise for a gain of 2000 across the channel. It can be observed that the first 4 highest components of noise are the flicker and thermal noises of the input pair of transistors. The resistor in the feedback loop of the first stage and the resistors from the DAC's are also seen to be significant noise contributors.

Device	Param	Noise Contribution	% Of Total
I2.M7.mds	id	0.000522037	27 .75
I2.M8.mds	id	0.000521766	27 .72
I2.M8.mds	fn	0.00029856	9 .08
I2.M7.mds	fn	0.000297862	9 .03
/R8	rn	0.000286446	8 .35
/I2/R12	rn	0.000226921	5 .24
/I2/R10	rn	0.000223638	5 .09
I21.M59.mds	id	0.000136018	1 .88
I21.M0.mds	id	0.000135992	1 .88
I2.M22.mds	id	8.40188e-05	0 .72
I2.M21.mds	id	8.27141e-05	0 .70
I2.M32.mds	id	6.76228e-05	0 .47
I2.M32.mds	fn	6.51961e-05	0 .43
/I2/R13	rn	4.66064e-05	0 .22
/R1	rn	3.91683e-05	0 .16
/R16	rn	3.63716e-05	0 .13
I2.M22.mds	fn	3.55961e-05	0 .13
I2.M21.mds	fn	3.49478e-05	0 .12
/R2	rn	3.46977e-05	0 .12
I2.M28.mds	id	3.30577e-05	0 .11

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000991034
Total Input Referred Noise = 4491.52
The above noise summary info is for noise data

Figure 22 Noise Summary (Integrated Noise)

The input referred noise varies according to the input DC offset that needs to be canceled. The DAC needs to be adjusted to obtain the required voltage bias to the bulks of the input pair. This is done by switching different resistor's to obtain the voltages. The resistors

contribute to the noise of the channel and this leads to the variations in the input referred noise for different offsets that are canceled by the channel. The table below shows the top 20 parameters contributing to the channel noise with a DC offset of .1 being canceled by adjusting the bulk voltages.

Device	Param	Noise Contribution	% Of Total
I2.M8.mds	id	0.000524473	14 .35
I2.M7.mds	id	0.00051876	14 .04
I2.M8.mds	fn	0.000299799	4 .69
I2.M7.mds	fn	0.000292675	4 .47
/R8	rn	0.000287939	4 .33
/I2/R12	rn	0.00022552	2 .65
/I2/R10	rn	0.000222221	2 .58
I2.M32.mds	id	0.000200205	2 .09
I2.M32.mds	fn	0.000194384	1 .97
I21.R6.r2	fn	0.000188029	1 .84
I21.R8.r2	fn	0.000188029	1 .84
I21.R7.r2	fn	0.000188029	1 .84
I21.R5.r2	fn	0.000188029	1 .84
I21.R4.r2	fn	0.000188029	1 .84
I21.R3.r2	fn	0.000188029	1 .84
I21.R2.r2	fn	0.000188028	1 .84
I21.M36.mds	id	0.000173225	1 .57
/I2/R13	rn	0.000137983	0 .99
I21.M0.mds	id	0.000136711	0 .98
I21.R6.r3	fn	0.000108558	0 .61

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.00138429
Total Input Referred Noise = 4129.04
The above noise summary info is for noise data

Figure 23 Noise Summary with DC Offset of 0.1V

The table below shows the variation of the input referred noise with different DC Offset levels. The gain of the channel was set to 2000 while the offset was varied.

The offset voltages of the input are varied from +.3 to -.3 and the noise performance of the system tabulated.

Table 2 Noise Vs Offset

Offset	Noise (in V)	Input Referred Noise (in uV)
0.1	.00138	0.69
0.2	.00166	0.83
0.3	.00184	0.92
-0.1	.00129	0.65
-0.2	.00176	0.88
-0.3	.00181	0.91

For positive offsets the fine DAC string output is reduced to raise the level of the output of the channel. This can also be done by rising the level of the output from the coarse resistor string. The coarse string is used for larger changes in the output voltage levels compared to the fine string. The combination of both the coarse and the fine DAC string outputs are used to adjust the output level to cancel the DC offset that is present in the incoming signal.

5.3 Charge Pump

The charge pump is used to provide a higher supply voltage to the bandgap reference. The

plot below shows the value of 2VDD-VSS which is obtained at the top plate of the output capacitor. The input voltages to the charge pump are the supplies +1 and -1 volt. The output obtained from the charge pump is 2(VDD-VSS) relative to VSS. Hence effectively there is a doubling of the voltage that was given as the charge pump input. The top plate settles at 2.97 volts and the small drop from 3 volts is due to the transistor switches which have small resistive drops.

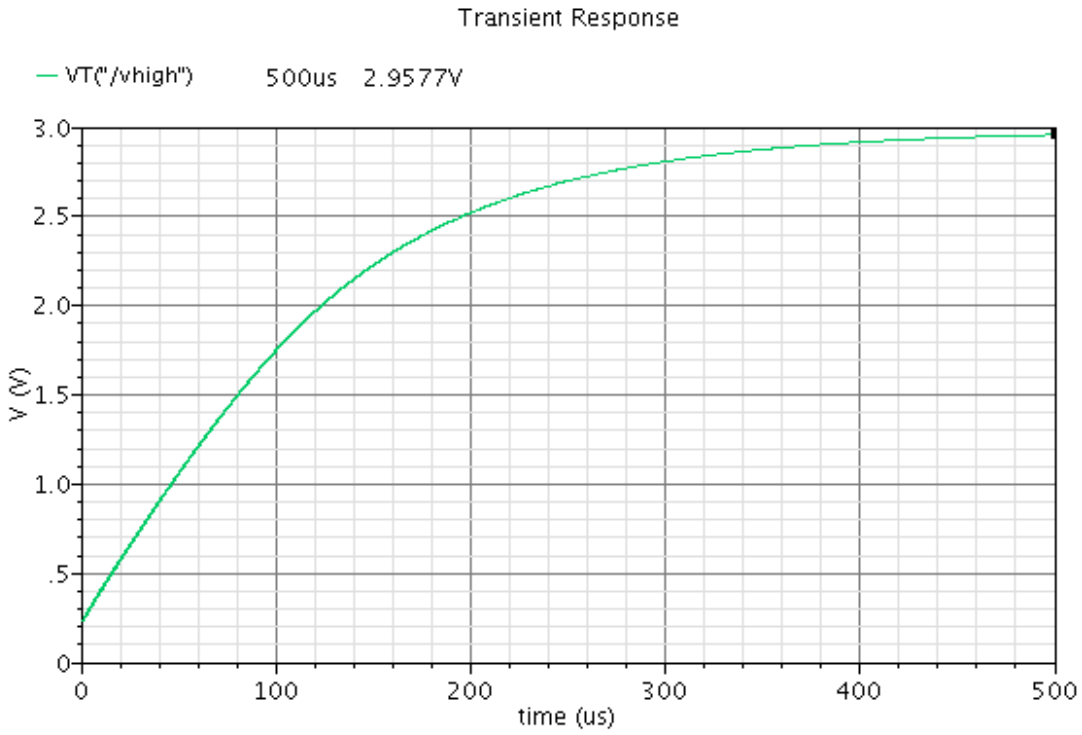

Figure 24 Output of Charge Pump

The signal plot below shows the high voltage clocks that are generated to toggle the switches handling the high voltage. The clocks phi1 and phi2 set the charging and

discharging rates of the capacitors. Their frequency can be increased to meet higher current requirements.

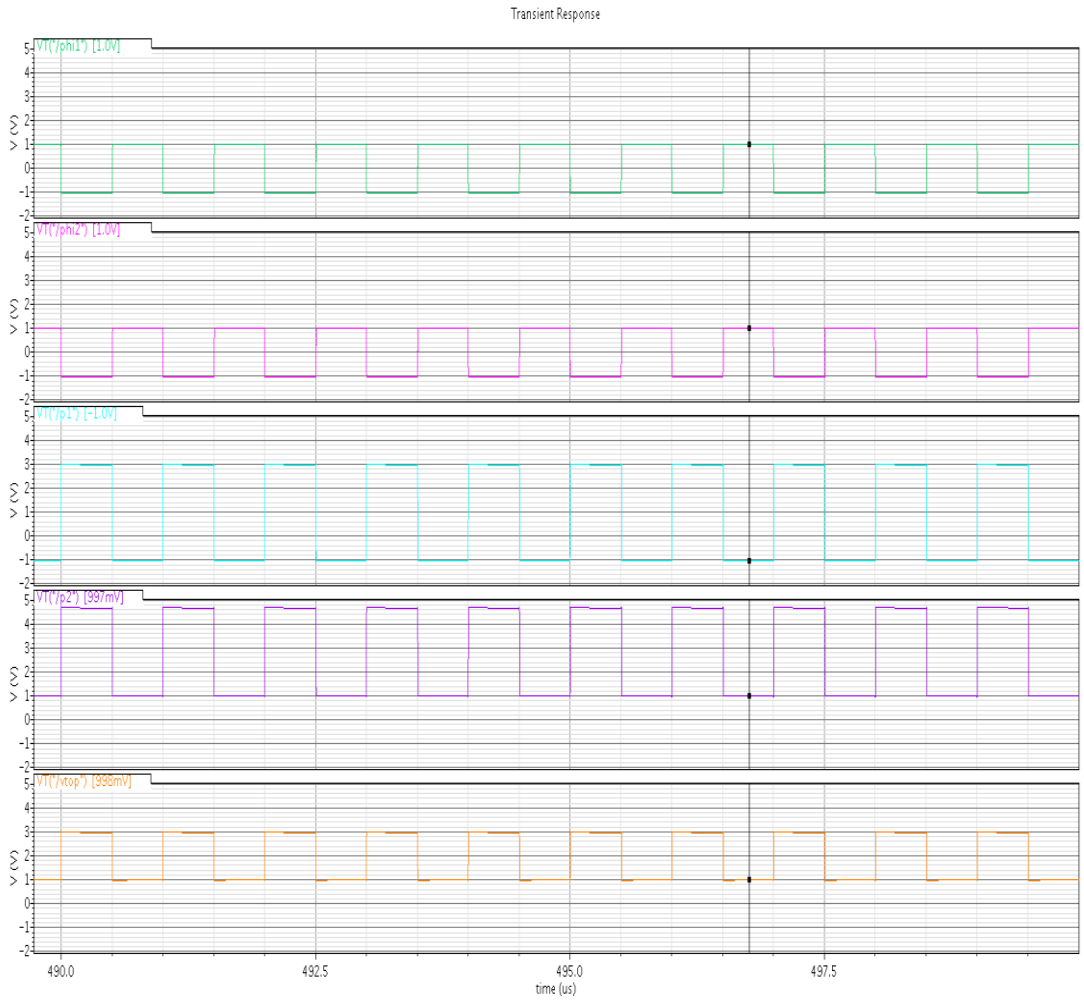

Figure 25 High Voltage Clocks

5.4 Offset Cancellation

The DC Offset cancellation is achieved in the first stage of the channel. The following plot shows the cancellation of a DC Offset of 0.3 volts. The decoder switches are set to provide the required voltages to the bulks of the input pair of transistors on the first stage.

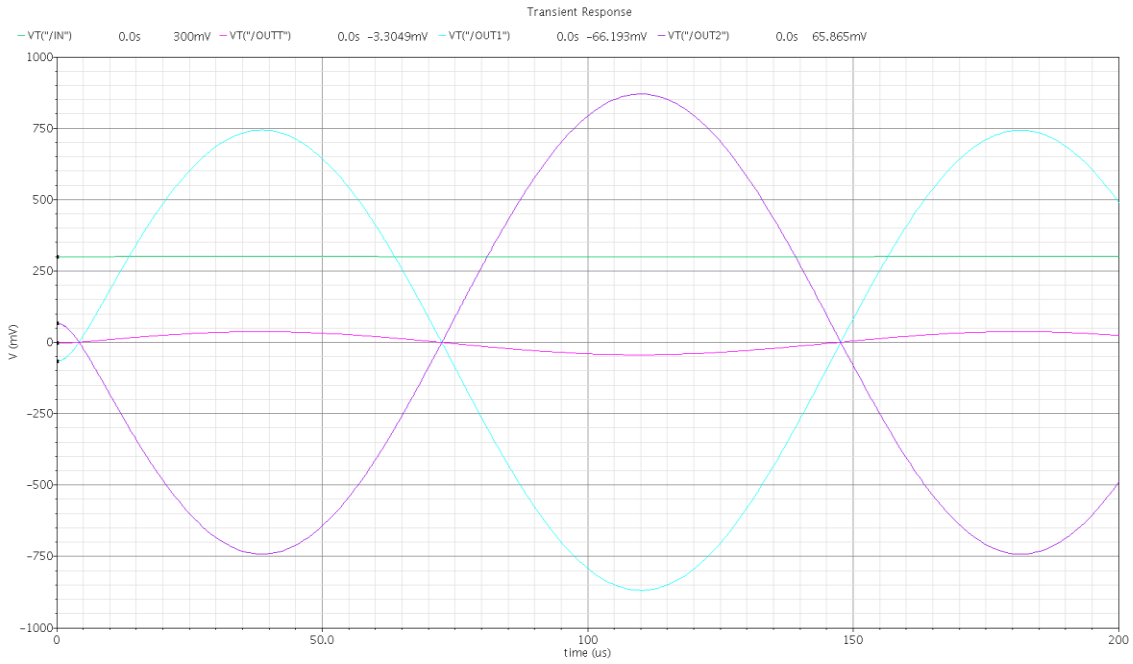

Figure 26 DC Offset Cancellation

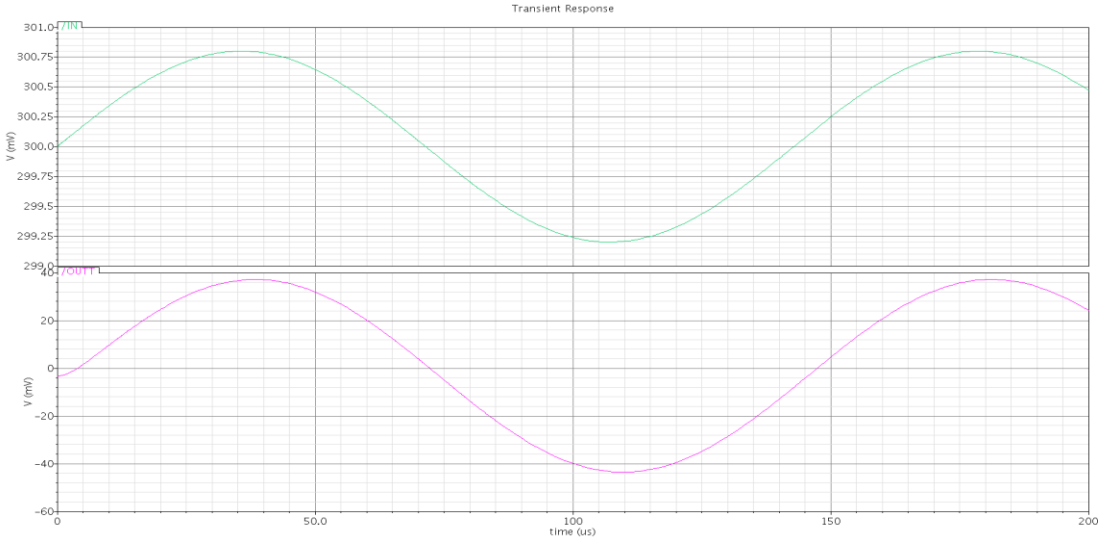

Figure 27 Offset at Output of First Stage

Figure 26 shows the input with an offset of .3 volts, the output of the first stage with a gain of 50 and offset cancellation, the second stage Op Amp's each amplifying the signal 20 and -20 respectively. Figure 27 shows the input with a DC Offset and the DC offset canceled output of the first stage separately for clarity.

5.5 Filter Response

The 2nd order Butterworth was designed using the Analog Filter design tool of ANALOG DEVICES. Subsequent design changes led to the replacement of the Butterworth filter with an RC filter. The filter responses of both the filter's are shown in Figure 28 and 29. The Butterworth filter as expected has a sharper fall as compared to the RC Filter after the cut-off frequency in the frequency response graph.

The butterworth filter has a slope of -40dB per decade compared to the -20dB per decade of the RC filter.

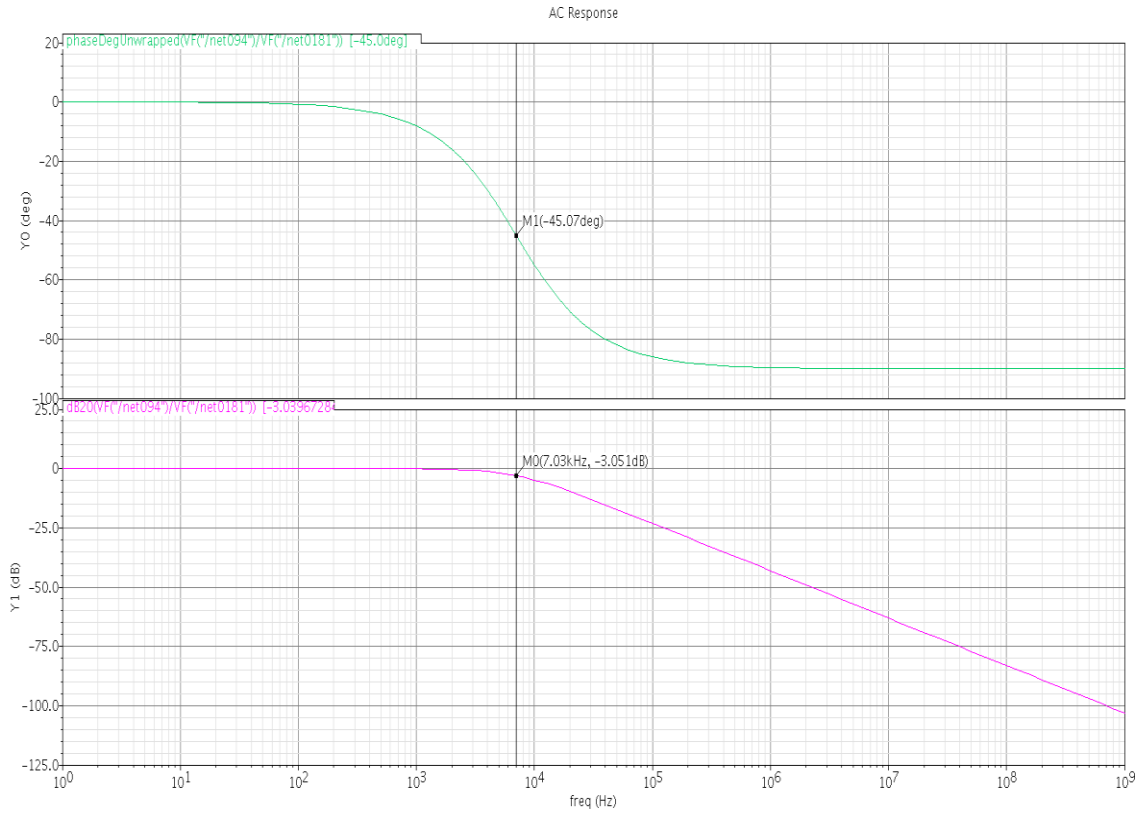

Figure 28 AC Analysis of RC Filter

The cut off frequency of the RC filter is 7KHz. This is the bandwidth of the signal that can pass through the filter. For a capacitor value of 100p the value of the resistor is 227.36K Ohms.

The response of the Butterworth filter is shown in Figure 29. The Butterworth filter used in the preliminary design had a gain of 10 and a cut off frequency of 7KHz. The filter was designed using the Analog Filter Design tool of Analog Devices.

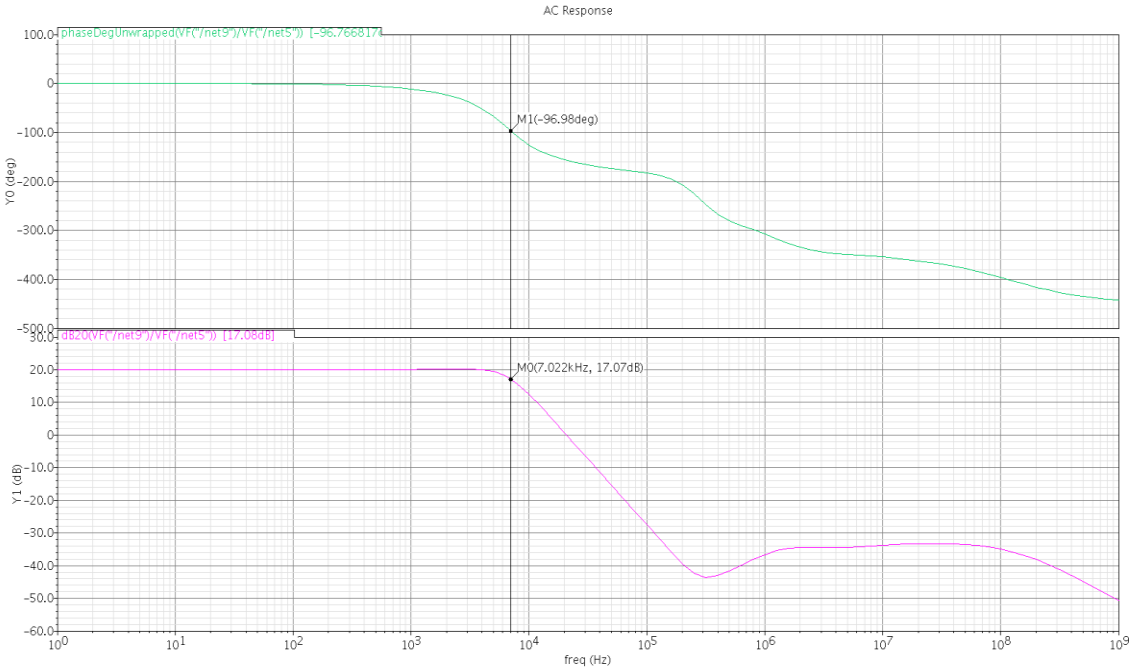

Figure 29 AC Analysis of Butterworth Filter

5.6 Resistor String DAC's

The resistor string DAC's provide the voltage levels used to bias the bulks of the input pair for DC offset cancellation. A single resistor string is used to bias both the bulks. The reference voltage for the DAC is 1.5 volts which is provided by a bandgap reference. The DAC consists of 32 fine resistors in series with 32 coarse resistors. One of the 32 levels produced by each of the coarse and fine resistor strings are used to bias the bulks of the first stage Op Amp.

By using a clocking scheme for the 5 bit decoder all the 32 voltage levels that will be produced by the fine and the coarse string's are obtained.

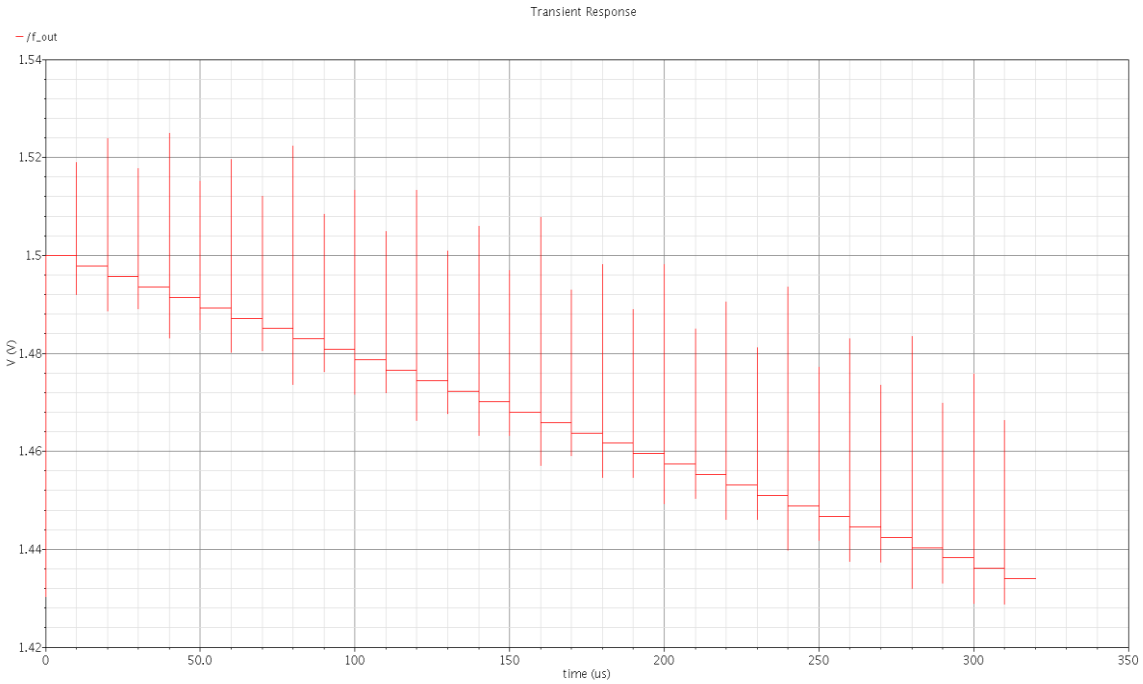

Figure 30 Voltage Levels of Fine DAC

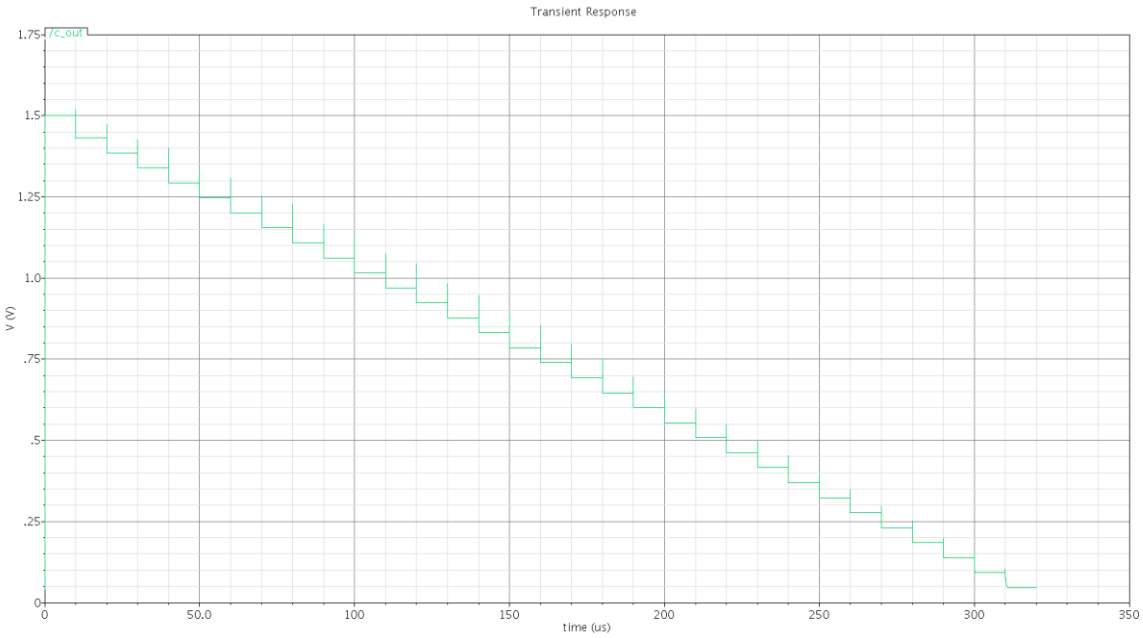

Figure 31 Voltage Levels of Coarse DAC

5.6 Bandgap Reference

The Bandgap Reference is used to provide the reference voltage for the resistor string DAC's. A charge pump was used to provide the upper supply voltage and hence the bandgap reference also charges up gradually to the required reference voltage of 1.5V. The output of the bandgap reference is shown in Figure 32.

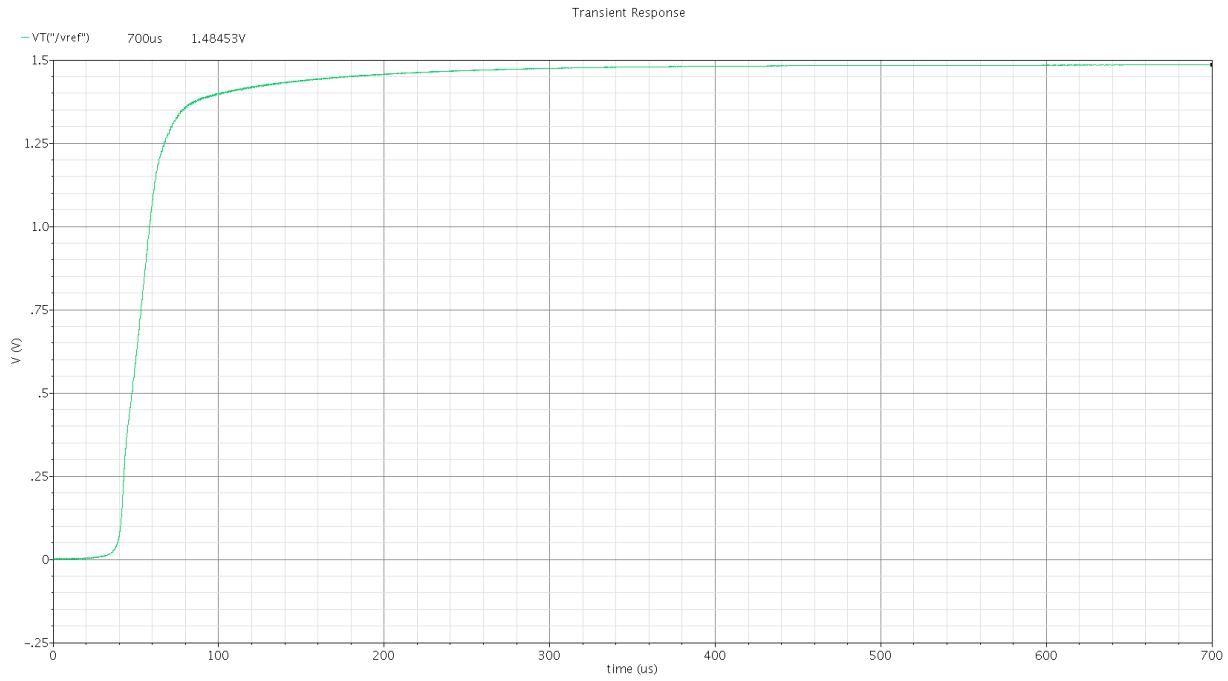

Figure 32 Bandgap reference voltage

The bandgap reference has a high PSR requirement. The PSR of the bandgap was measured to be above 60dB. This provides sufficient damping to power supply fluctuations. The PSR of the bandgap reference is shown in Figure 33.

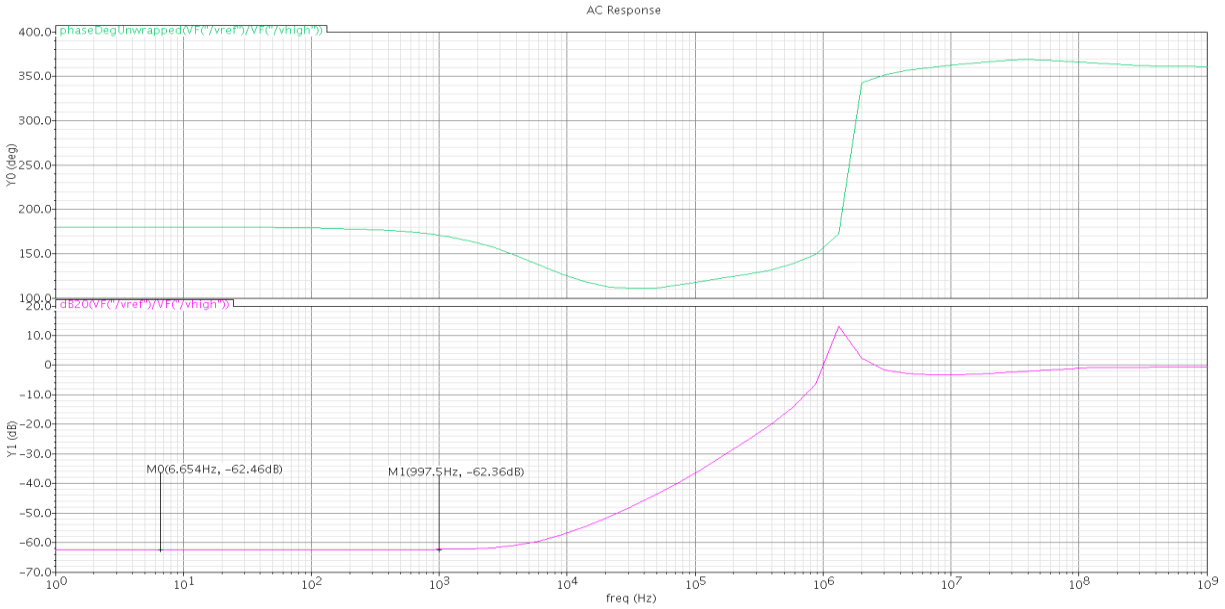

Figure 33 PSR of bandgap reference

5.7 Total Harmonic Distortion

The total harmonic distortion is measured using the cadence toolkit. The simulation was run for 12 cycles and a single cycle from the 10^{th} to the 11^{th} time interval was chosen and its DFT computed. The THD is then measured to be **0.017%.**

Thd(v("/OUT1"?result "tran-tran")1.4285e-3 1.5714e-3 1000 7000)

The DFT of the output signal is shown in Figure 34.

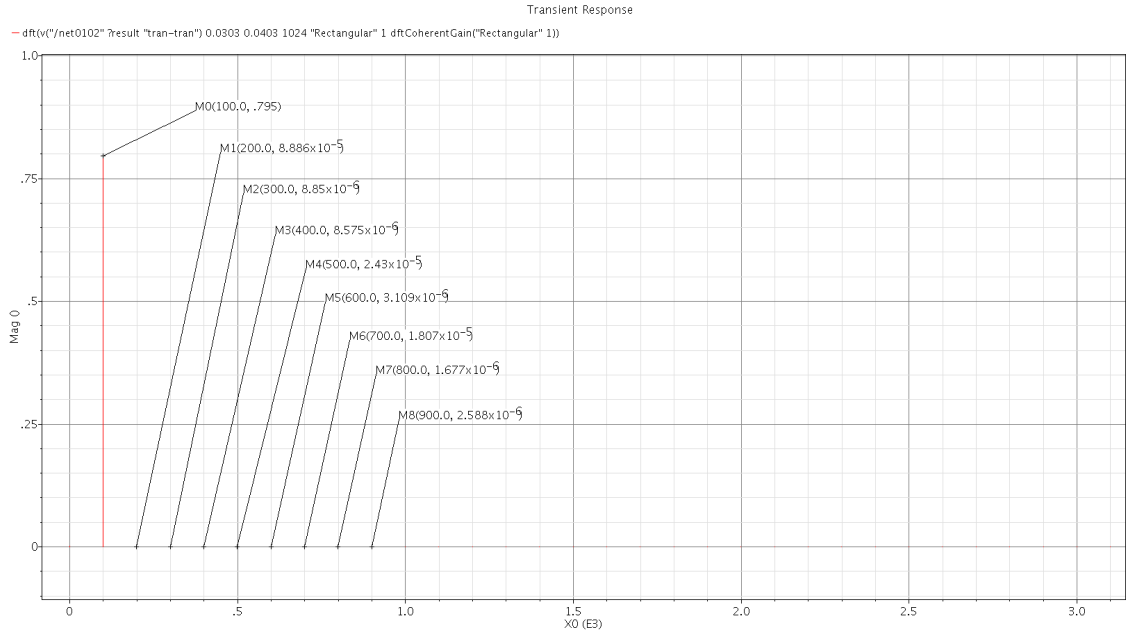

Figure 34 Discrete fourier transform

The DFT plot with a logarithmic scale is shown in Figure 35

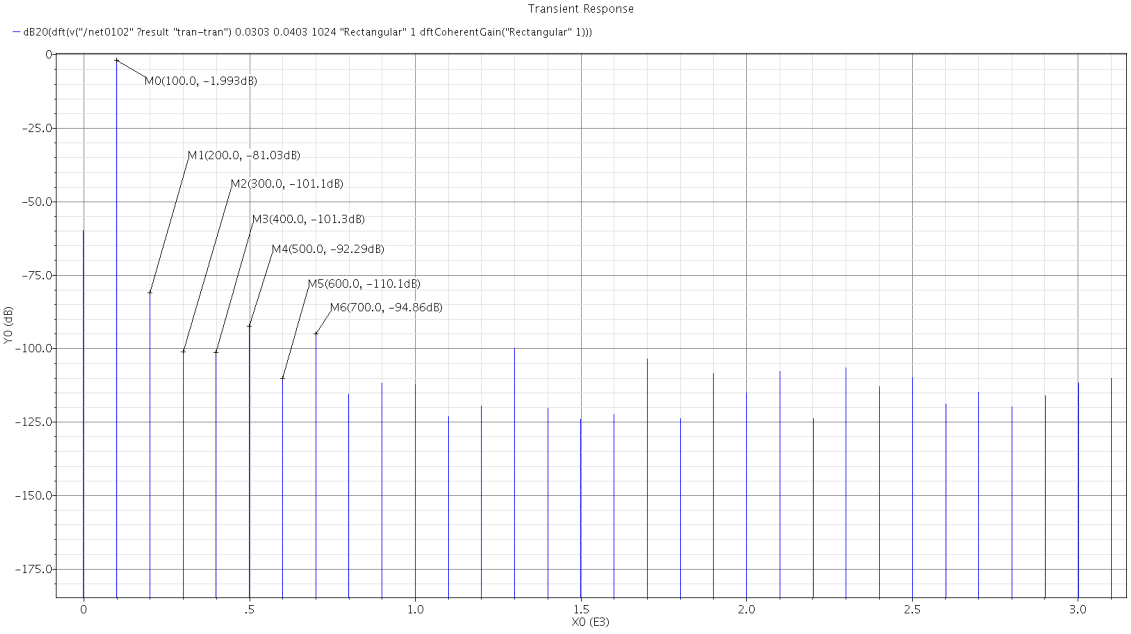

Figure 35 Discrete fourier transform (Log Scale)

To compute the SNDR the root mean squares of the harmonics is found. The computed value of SNDR is above 78dB.

Root mean square of harmonics = $\sqrt{(v2)^2 + (v3)^2 + (v4)^2 + (v5)^2}$

$= 92.04\mu$

SNDR $= \dfrac{v1, rms}{\sqrt{(v_h)^2 + (v_n)^2}}$

$=$ **78.72dB**

CHAPTER SIX

LAYOUT AND FUTURE WORK

6.1 LAYOUT

The layout of the sensor amplifier is nearing completion. The most important criterion during layout is to ensure that the devices are properly matched. This is especially important to the op-amp in the first stage of the channel. The input pair which has bulk control is laid out in a 4X4 grid with adequate spacing to isolate the bulks of the differential pair. The substrate between the spaced out n-well's can lead to stray capacitance. To avoid this they are all clamped together using a p-substrate connector.

The input pair along with the active load and the degeneration resistor's are also to be laid out in common centroid configuration. Common centroid layout's provide good matching and help avoid offsets which might affect the performance of the sensor amplifier.

6.2 FUTURE WORK

The DC offset cancellation on the current version of the sensor amplifier is +/- .3 volts. For certain applications of the sensor amplifier it would be desirable to have a higher DC offset cancellation. An approach to increase the DC offset cancellation of +/- 0.8 volts is presented. The channel would use a mix of techniques used in the current version of the design and the previously fabricated version. A 5-bit DAC or a resistor string can be used to introduce an additional offset cancellation of +/- 0.5 volts at the input of the first stage of the Op Amp.

The trade off due to this design change is the noise that will be introduced by this additional circuitry. The noise would be amplified by the two stages of the channel and hence would be one of the dominant contributors to the overall noise of the system.

This sensor amplifier together with an analog to digital converter on a single chip will be fabricated on the Jazz 0.18μm CMOS process. 16 channels from the sensor amplifier would be multiplexed to an analog to digital converter and direct digitized output will be available. A control block will be used to program the gain, adjust switches for offset cancellation on the individual channels and select the channel that needs to be measured using the ADC.

Remote powering of this setup to avoid the clutter of cables and battery usage has also been planned. It would essential to lower the power of the system to enable wireless

powering of the system and is a key design challenge. A fully integrated system after these improvements would provide an excellent tool to study neurological behavior.

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