WIDEBAND BODY ENABLED RF FRONT END TRANSCEIVER IN 0.18-µm TECHNOLOGY

By

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WIDEBAND BODY DRIVEN FRONT END TRANSCEIVER IN 0.18-µm TECHNOLOGY

Abstract

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To develop and implement a wideband body enabled front end transceiver for use in 0.18 µm. The front end transceiver implementation for this thesis will consist of the common first two devices which are the LNA and mixer. The LNA is the first device from antenna which is there to amplify the signal received from the antenna. The mixer is there to take the next step which is to mix the amplified signal from the LNA and mixer it with the signal from the local oscillator (usually a PFD).

The wide range of operation for both LNA and mixer will be from 4 – 12.5 GHz. The range of operation will require that over the range the input and output matching must be less than -10 dB. The gain of the LNA must be over 10 dB while the passive mixer will not have any gain therefore the goal will be to get the gain as close to zero as possible. The noise of the LNA should never get above 5 dB at any point during the range of operation. The noise of the mixer will be comparable to previously published papers where the noise is around 9 – 14 dB.

The LNA will implement forward body bias voltage applied to the body of the transistors to reduce the voltage required and current through the LNA and therefore saving power while maintaining the specifications of the LNA. The mixer will implement body driven topology in which the amplified signal from the LNA will be applied to the

body terminal therefore allowing the mixer to achieve better results than if the amplified signal was coming through drain of the transistors.

Overall the design of the LNA is a completely new idea that has never been researched before and will allow for the LNA to achieve a wide range of operation while reducing the voltage supply. The mixer is a concept adapted from a published paper and developed for a new mixer topology and will allow for increased results and better range of operation than previously published papers.

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Dedication

This dissertation/thesis is dedicated to my parents and my fiancé who provided financial and emotional support.

CHAPTER ONE

INTRODUCTION

In recent years there has been an increase in demand for low voltage and low power consumption wireless communication devices to preserve battery life. This leads to lower cost and higher performance of these devices. The progress of RFICs (radio frequency integrated chips) have allowed for wireless devices to decrease the size and power while either maintaining or increasing the key specifications. This allows the designer to have fully integrated RF (radio frequency) frontend in a CMOS (complementary metal-oxide semiconductor) process on a single chip.

1.1 The Need For Smaller Devices

The ability to decrease the size of the chip will allow for more single chip devices. The applications are endless when it comes to the creation of a smaller chip design. It will allow for implementation of chips in medical devices to become realistic and improve the quality and longevity of life. The implementation of small devices will also lead to more advancement in power saving technology and decrease energy costs across the board. The decrease in size also leads to much higher operating frequency in devices and increase the speed and accuracy of the chip.

If the medical world had smaller longer lasting implants in patients it would allow for communication with the device to last longer and decrease the discomfort for the patient. The implants allow for patients to keep constant track of their medical health. The longer lasting communication and accurate reading will lead to earlier detection and fast action when something goes wrong which will allow the patient to more likely be saved from an incident. The fact that most sensors need to be placed in very sensitive

areas the smaller size will allow for less discomfort and less likely that the chip to become dislodged.

The wireless communication world with power saving devices will be able to create state of the art wireless devices that will be able to last longer before the power supply has to be changed or recharged. The smaller devices get the more development in new devices become realistic and more money a company will be able to make. The ability to increase the operating frequency will allow for the further away from the transmitting source and still be able to maintain communication which is a key advantage in wireless technologies.

1.2 The State Of The Art

The radio frequency is the range of oscillation of a signal usually between 3 Hz to 300 GHz. The world of wireless communication exists in the SHF (super high frequency) which is the range of 3 GHz to 30 GHz. Although for all WLAN (wireless local area network) these ranges are set by the IEEE standards committee to 2.4 GHz, 3.6 GHz, and 5 GHz.

The recent decrease in chip size follows Moore's Law [1]. Moore's law states that since the invention of the integrated circuit in 1958, the number of transistors that can be placed inexpensively on an integrated circuit has increased exponentially, doubling every two years [1]. Almost every digital electronic device is closely related to this law.

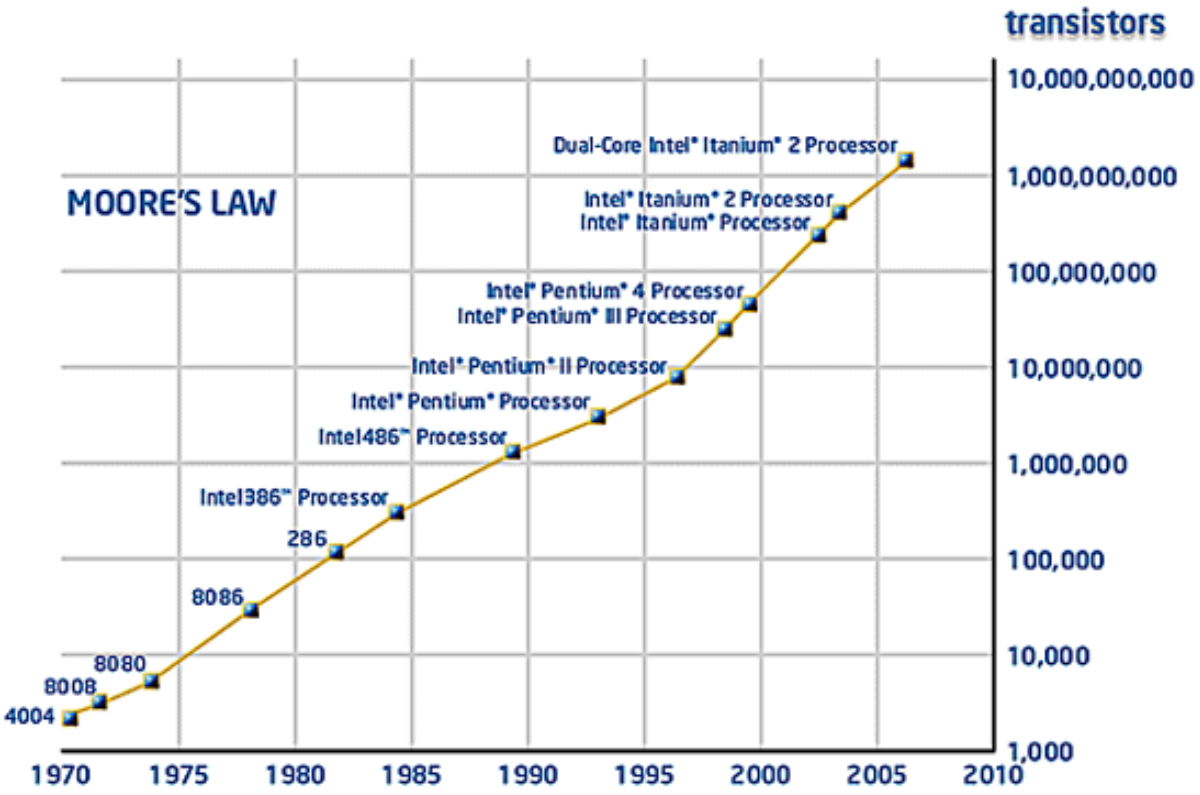


Figure 1: Moore's Law (property of Intel)

The technology length of CMOS is also an area of research interest in deciding which package to use. The length is important because as the length decreases there is going to be direct tunneling leakage current. This is in relation as the gate length decreases then it becomes inversely related to the current which will cause more current to flow through the drain and less current through the gate. Recent advancements have reached down to 40 nm. These are still experimental and not all parameters have been verified. The technology available for these experiments was .18 µm and 90 nm. The process of .18 µm was used because all components have been verified, process tested, and chip analyzed by earlier work. Whereas 90 nm the process has been verified but not all components were accessible.

1.3 Power Consumptions

The key idea is to reduce the size of the chip and power consumption for all developed chips. This is seen in that most wireless communication devices must use a battery to supply the chip. This means that the lower the power consumption the longer the battery life. For this reason power reduction is the most critical issue in many wireless applications. The most efficient technological approach for reducing the power consumption is by reducing the voltage supply. The reduction of the voltage supply will also cause the current to decrease, which in turn will reduce key specifications. So the idea is to find a way to reduce the voltage while maintaining the current through the designed chip.

The power consumption calculation is difficult to calculate due to the fact that not all components of the chip are on at all times. This causes for design to be focused on the components that require the most power to run when on. These are mainly focused on the CMOS transistors that are involved in the chip.

Once the voltage is reduced on the transistor it is possible to be within the ultra low voltage which is below 1 V. The problem with this is that once supply voltage is reduced down to .6 volts is in high risk of being in weak inversion. This occurs when the $V_{gs} < V_{th}$ which basically says that the transistor is turned off. This will cause the current to vary exponentially with gate-to-source until it reaches zero. The weak inversion will cause the voltage to be restricted during design.

1.4 Transistor at High Frequency

The use of transistors at radio frequencies will require extra time spent on researching and parameters to consider into calculations due to parasitic capacitances

and resistances. These need to be taken into account during all forms of calculations (gain, noise figure, and matching). Figure 2 is transistor at high frequency used for analysis in RF circuits.

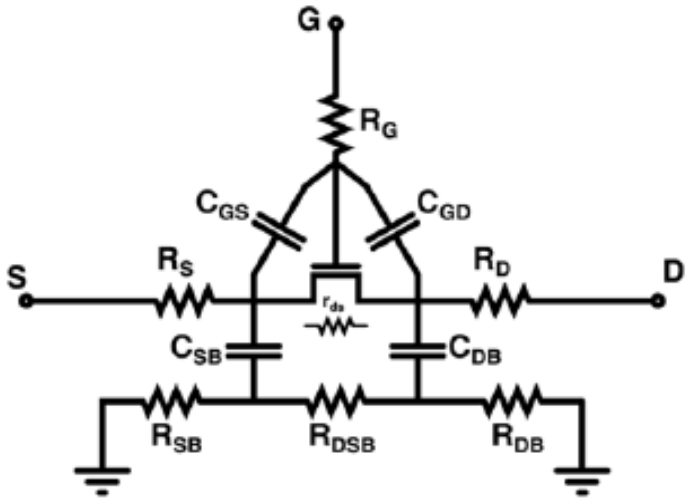


Figure 2: High frequency model for transistor

1.5 The Affect of the Body Terminal

The reduction of the power consumption will be done by reducing the supply voltage which will cause the current to be reduced (figure 3b). To offset this reduction in current the body terminal in a CMOS transistor will be used. The body terminal can be added due to the fact that when a deep N-well is below the transistor it separates the substrate of the entire chip so that it has its own substrate (figure 3a). The deep N-well technology is fairly new and is now recently being use to increase the threshold voltage using equation 1.

$$V_{th} = V_{tho} + \gamma\left(\sqrt{2\phi_f - V_{bs}} - \sqrt{2\phi_f}\right) \quad (1)$$

Where V_{bs} is the body to source voltage and φ_f is the surface charge (fremi potential) and γ (gamma) is the body threshold factor. Normally the body voltage is

zero, which has no affect on threshold voltage and it depends only on source voltage. A forward body bias voltage is applied to the equation if a positive voltage is applied to the threshold voltage equation. The threshold voltage will decrease due to the body voltage and intern through equation 2 will cause the current to increase. This also will cause the transconductance G_m to change to G_{mb} (equation 3) [2].

$$I_D = \frac{\beta}{2}\left(V_{gs} - V_{th}\right)^2 \tag{2}$$

$$G_{mb} = \frac{\gamma g_m}{2\sqrt{2\phi_f - V_{bs}}} \tag{3}$$

Although this voltage V_{bs} needs to be limited to under .7 volts. This .7 volts is the threshold voltage and if V_{bs} is above this a body leakage current will be negligible. There is another inherit advantage to the deep N-well process. The process will allow for greater isolation and lower substrate noise. This is caused by the fact that the separate body region cause by the N-well. Isolation factors are key in mixers and the reduced substrate noise will be key in both a mixer and LNA. Also a reverse bias voltage can be applied to the body but is not commonly used for obvious reasons.

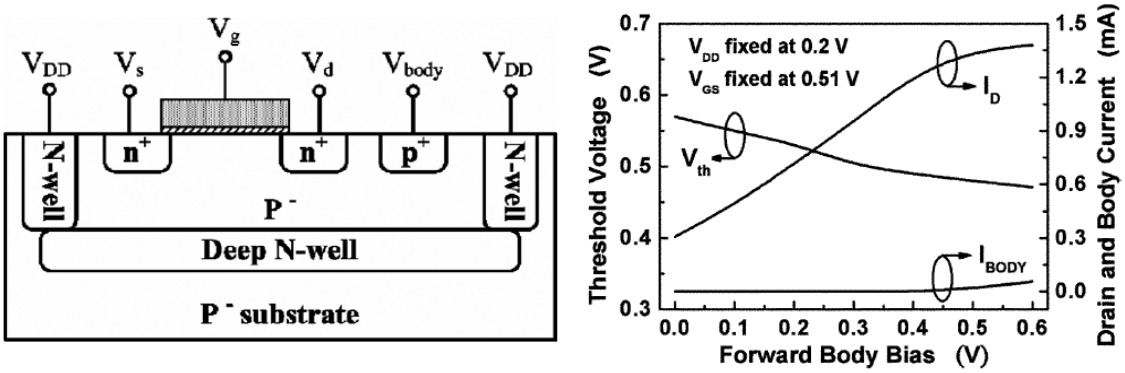


Figure 3: (a)Cross-sectional view of NMOS transistor with deep N-Well Technology [2]
(b) Visual description on how body terminal affects current of the system [9]

There is another way to use the body terminal which is by using the port to drive a signal using the port. The driven port will in turn reduce the overall size of the chip by reducing the number of transistors. The body port will also increase the current therefore allowing for a reduction in the supply voltage. This reduction in power supply leads to a reduction power consumption.

1.5 Overview of this Work

The RF frontend has a lot of potential for advancement especially in the PLL (phase locked loop), frequency synthesizers, low-noise amplifiers, and mixers. The research topics of this paper are the effects of the body for the LNA and the mixer. The body effect can exploit a way of reducing the operating voltage (to reduce the power consumption) and to reduce the size of the chip (figure 4). Also the body terminal can be used as a port in the mixer to allow for better simulation results. In addition to designing the chips to take advantage of the body effect there will also be designing for use in wideband range. Wideband consists of a range of operation where all specifications are met. To be considered wideband, the specifications must be better than the minimum over a range of at least 3-5 GHz.

The low-noise amplifier is a crucial component that predetermines the sensitivity of the dynamic range in a wireless communication system. The low-noise amplifier's propose is to amplify the gain of the incoming signal while simultaneously keeping the noise figure relatively low. Low-noise amplifiers can use forward body bias technique to increase the current. Therefore, this allows the chip to be run in low voltage operation while staying out of the inversion region. The LNA will be designed to reduce the voltage headroom while still maintaining the range of operation and specification minimums.

The mixer allows signals to be converted to different frequencies and to therefore allow for better processing. The mixer will take the signal coming in and either convert the signal to a higher or lower frequency through the LO (local oscillator) port. The mixer will always want good isolation between ports. The body terminal will allow for the mixer to drive a port through the body terminal while also lowering the power consumption. Allowing the body terminal to have either LO or RF terminal come through the body terminal will also help with isolation and matching. The wideband technology will allow for better range of operation and therefore allow for only a single chip be designed for a range of operation rather than several chips each for a single frequency. The advantages of body enabled technology and the wideband range of the LNA and mixer will be implemented in the RF transceiver architecture (figure 4). The mixer will translate the frequency to a lower frequency to be used in the ADC.

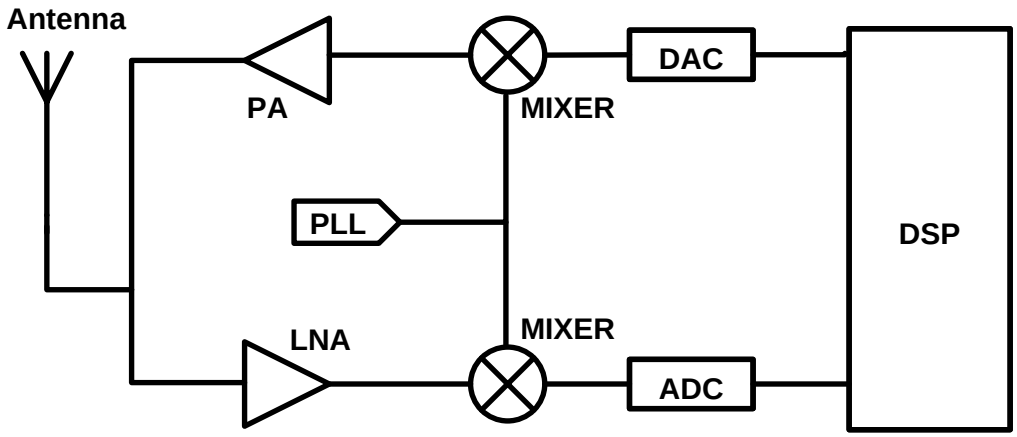


Figure 4: RF Transceiver Architecture

The introduction, background material, applications, proposed ideas, simulation, and layout will be presented in chapter 2 and chapter 3 for the low-noise amplifier and mixer respectively. Chapter 4 will consist of the future work that can be researched on this subject.

CHAPTER TWO

LOW-NOISE AMPLIFIER

2.1 LNA Background Information

The low-noise amplifier is a crucial component that predetermines the sensitivity of the dynamic range in a wireless communication system. The low-noise amplifier's propose is to amplify the gain of the incoming signal while simultaneously keeping the noise figure relatively low. The LNA determines the overall performance of the transceiver because the LNA is usually the first topology to get the signal from the antenna. The recent years' objectives to increase the operating frequency of LNA's have put tremendous stress on the existing LNA architectures. CMOS LNA's are increasingly getting more attention due to the fact that users want a cheaper, fully integrated solution. The CMOS LNA provides this solution.

The LNA design requires tradeoffs between the noise figure (NF), gain, linearity, impedance matching, and power dissipation. Generally, the goal of LNA design is to achieve simultaneous noise and input matching at any given amount of power dissipation [4]. The LNA is usually designed to have impedances that closely resemble a 50 Ω termination at both the input and output maximum power transfer at RF. LNA input and output matching is very important because the RF filter responses are heavily dependent on the matching conditions. LNA must also have good reverse isolation so that the signal at the output is not allowed to traverse backwards through the LNA into the antenna.

The first portion of LNA design is whether to do a wideband or narrow band LNA. The narrow band LNA is designed around a specific frequency and should work near that frequency but any other frequency would not work for a narrow band LNA. The next

choice is the wideband in which it has usually two LNA's where each is designed around a specific frequency and is then connected together to allow the LNA to run in a wideband region (figure 5).

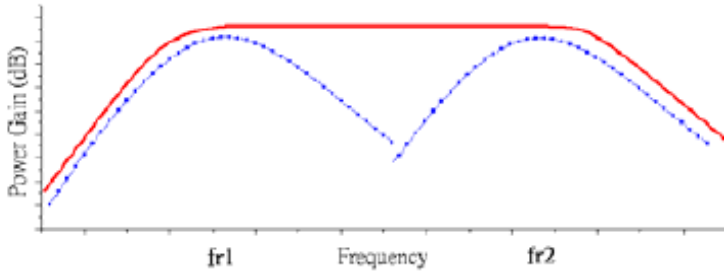


Figure 5: Operating frequency for a wideband LNA [3]

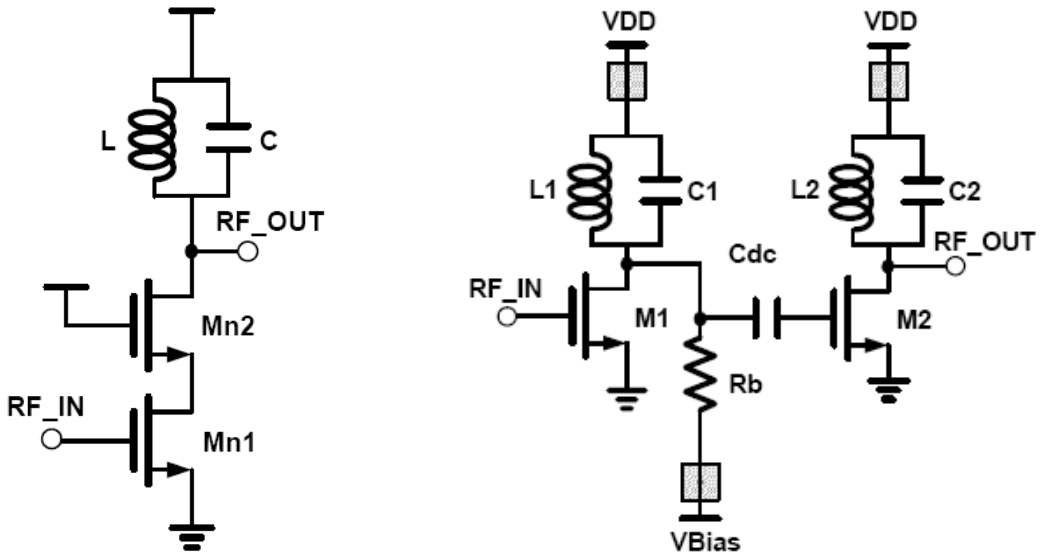
The most widely used LNA is the cascode amplifier which helps in the matching because it is nearly unilateral and has virtually no noise at low to high frequencies (figure 6a). The noise is small due to the degeneration because when the total current is taken into account after both cascoded amplifiers. This will give a total current noise close to zero (equation 4). Cascoded LNA's are also considered to be current reuse because both transistors are using the same current coming from the source voltage. This allows for considerable decrease in current and overall power consumption.

$$\left(1-\frac{-g_m r_o}{1+g_m r_o}\right) i_d = \left(\frac{1}{1=g_m r_o}\right) i_d \approx 0 \qquad (4)$$

The next topology that can be used in the LNA is the LC tank. The LC tank is an inductor and capacitor in parallel to each other. This is placed at the top of the LNA which will eliminate the Miller effect on the input of the transistor to allow for high frequency performance. The Miller effect is the increase in equivalent input capacitance on an amplifier due to the amplification of capacitance between input and output

terminals. This is mainly used in narrow band LNA's because of its high selectivity in frequency (figure 6a).

Therefore, two stages of LC tank in a wideband (figure 6a) will achieve higher power gain. This is called cascade amplification where the drain of the first transistor is connected to the gate of the second transistor (figure 6b).



(a) (b)

Figure 6: (a) Cascode LNA with LC tank (b) Cascade LNA with LC tank [3]

The input matching is best achieved through inductive source degeneration. Inductive source degeneration is when an inductor is added at the gate and the source of the transistor this will help with the noise performance and input matching of the LNA at higher frequencies (figure 7). L_s is used to generate the real impedance to match the input impedance around 50 Ω which is extremely helpful in keeping the noise figure to a minimum (equation 5). At resonance the s terms go to zero and we are left with $g_{m1}*L_s/C_{gs1}$.

$$Z_{in}(s) = sL_g + sL_g + \frac{1}{sC_{gs1}} + g_{m1}\frac{L_s}{C_{gs1}} \tag{5}$$

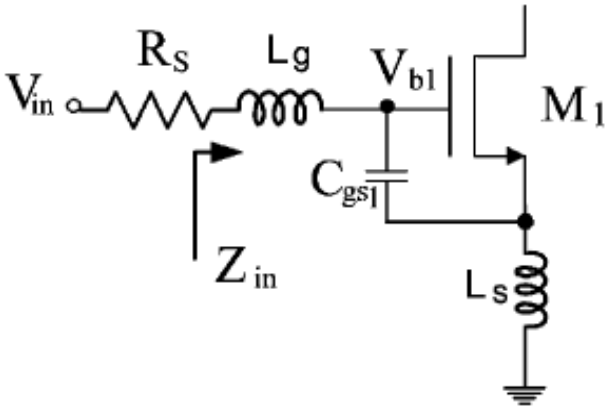


Figure 7: Inductive source degeneration with parasitic capacitor

The transistor Mn1 of figure 6a could have a capacitor from the gate to the source to improve the input noise matching of the LNA (figure 8 and equation 6). This capacitor runs parallel with the parasitic capacitance C_{gs1}. If this capacitance is tuned correctly it can optimize the noise characteristic and also the input return loss.

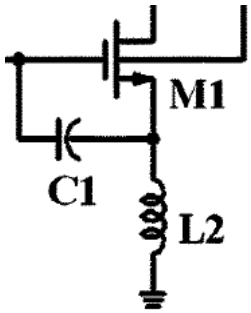


Figure 8: C_1 added to help with matching

$$Z_{in} = \frac{1}{j\omega(C_1 + C_{gs})} + j\omega(L_1 + L_2) + \frac{g_m L_2}{C_1 + C_{gs}} \tag{6}$$

*NOTE L_2 is the same as L_s and L_1 is the same as L_g

2.2 LNA Specifications

LNA's have several different aspects to consider during design, including input/output return loss, power gain, reverse isolation, noise figure, input 3rd order intercept point, 1 dB (decibel) compression point, voltage supply, and power consumption. The derivation and characterization of these are described in the below sections.

S-parameters

The S-parameters are a way of calculating a two-port network in terms of incident and reflected power. Shown in figure 9 a_1 is the portion of the wave that originates at the source and is incident on the two-port device (input wave), b_1 is the reflected wave, a_2 is the amount of the transmitted signal is then reflected from the load and becomes incident on the output port of the two-port device (output wave), and b_2 is a portion of the signal (a_2) is reflected from the output port back towards the load (transmitted wave).

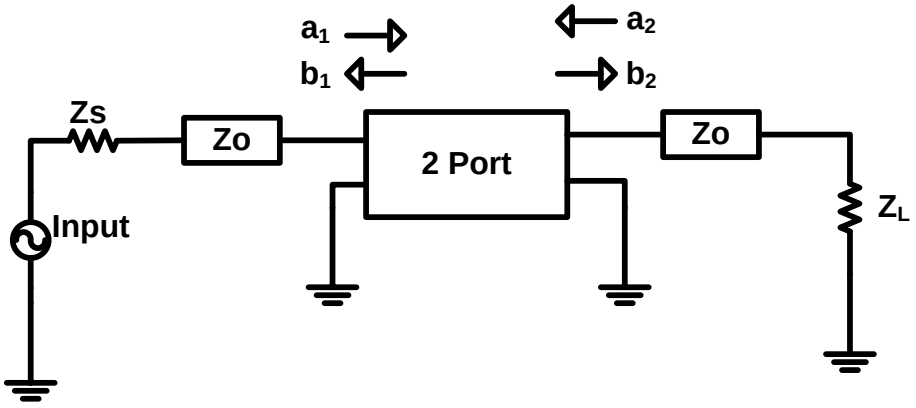


Figure 9: Two port RF system

A transmission line is terminated in a load that has the same resistance as its characteristic impedance, then no load absorbs all incident power traveling along the

transmission line and there is no reflection. This is why RF systems are designed around 50 Ω.

Any traveling wave present in the circuit is composed of two components. This allows the s-parameters to be described in a relationship of these waves (equation 7,8). They can also be represented in matrix form (figure 10).

$$b_1 = s_{11}a_1 + s_{12}a_2 \tag{7}$$

$$b_2 = s_{22}a_2 + s_{21}a_1 \tag{8}$$

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = [b] = [S][a]$$

Figure 10: Matrix form relating S-parameters to 2 port system

Then using the matrix form the s-parameters can be solved and defined. The S_{11} (equation 9) is the input reflection coefficient measured with the output terminated with Z_o. This means the output is matched and all the transmitted power is absorbed by the load (a_2 is zero).

$$s_{11} = \frac{b_1}{a_1} \tag{9}$$

S_{21} is the forward transmission coefficient. It is also measured when the output terminated with Z_o (a_2 is zero). This represents the equivalent gain of the system (equation 10).

$$s_{21} = \frac{b_2}{a_1} \tag{10}$$

S_{22} is the output reflection coefficient measured by applying a source to the output and with the input terminated with Z_o (a_1 is zero). This can be seen in equation 11.

$$s_{22} = \frac{b_2}{a_2} \tag{11}$$

S_{12} is the reverse transmission coefficient measured with the input terminated with Z_o (a_1 is zero). This can be seen in equation 12.

$$s_{12} = \frac{b_1}{a_2} \tag{12}$$

The LNA can be characterized completely by its s-parameters. These will allow for calculation of potential instabilities, maximum available gain, input/output impedances, and transducer gain. Also it will allow for optimization of the source and load impedances for simultaneous matching. Transducer gain is defined as the output power delivered to the load by the source, divided by the maximum power available from the source. It includes the effects of the impedance matching at the input and output while also considering the contribution made by the overall gain of the LNA.

Noise Figure

The noise factor is defined as the SNR_{in} divided by SNR_{out}. Thus the noise figure is a measure of the degradation of the SNR through each stage of the LNA. The lowest the noise factor can get is 1. The noise figure is 10 log(Noise Factor).

There are different noise figure calculations for different LNA's. The cascaded system will take the noise of the first stage and add noise of the second stage and divide by the gain of the first stage (equation 13). The noise of a cascode system (equation 14) is calculated by the taking each transistor individually and combing them. The noise minimum is where the system is the frequency at which it is designed around.

$$F_{CASCODE} = F_1 + \frac{1}{G_1}(F_2 + 1) \tag{13}$$

$$F = F_1 + F_c \cong F_1 + 4R_s\gamma_2 g_{do2}\left(\frac{\omega_o^2 C_x}{\omega_T g_{m2}}\right) \quad (14)$$

Linearity

The IIP3 is a measure of its linearity at the input of the LNA. While many analog and RF circuit are approximated with a linear model to obtain their response to small signals, non-linearities often lead to harmful problems. This is why it needs to be considered with an input of x(t) to a system to the linear and nonlinear output (equation 15).

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \quad (15)$$

It shows that if x(t) consists of two sinusoidal signals of different frequencies (w_1 and w_2), then the output contains terms at every integer addition and subtraction of the frequencies. The consideration for LNA is at the 3rd order where $2w_1$-w_2 and $2w_2$-w_1 will be the closest the original signal (figure 11). A measure of the strength of these unwanted signals at the input is called the IIP3 (equation 16).

$$IIP3 = P_{output}(dBm) - P_{imd3rd}(dBm)\Big/_2 + P_{output(dBm)} \quad (16)$$

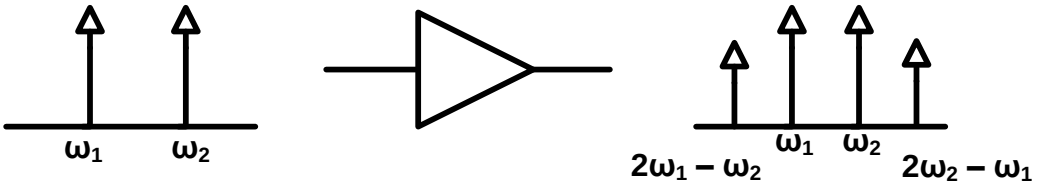


Figure 11: 3rd order intermodulation in a nonlinear system

The 1 dB compression point (P_{1dB}) is used with the conversion gain to allow for a fair comparison of the LNA topologies. This is important because the ability to get high gain and keep it that high is very important to the LNA.

Figure of Merit (FOM)

The LNA has 3 different FOM's that are commonly used in comparing LNA's. Equation 17 is a FOM that looks at ratio of the gain in dB to the dc power consumption in mW. Equation 18 is FOM used to compare power gain, noise figure, and power dissipation performances. It can also be extended to include P_{1dB} and cutoff frequency of the LNA (equation 19) [5]. It should be noted that after these calculations the FOM needs go into the equation 20*log(FOM) to give the comparable value.

$$FOM_1\left[dB/mW\right] = Gain[abs]/P_{dc}[mW] \tag{17}$$

$$FOM_2[mW^{-1}] = \frac{Gain[abs]}{(NF-1)[abs]*P_{dc}[mW]} \tag{18}$$

$$FOM_3[Hz] = \frac{Gain[abs]*P_{in\_1dB}[dBm]*f_c[Hz]}{(NF-1)[abs]*P_{dc}[mW]} \tag{19}$$

2.3 LNA Topologies

This section will discuss the different LNA's that have already been published. These will be used for comparison to the designed LNA. The idea of two frequency peaks used in [3] was implemented to achieve wideband range for the LNA. The idea of

forward biased voltage applied to the body used [5] was applied to this research to get reduced voltage and therefore power supply will be reduced.

Wideband LNA

The wideband LNA is developed by taking two narrow band LNA's and combining them to allow for a large operational frequency range. The wideband usually consists of the conventional source degeneration using inductors. It also consists of cascoded transistors to increase the gain of the LNA. The transistors are then connected in two stages for both upper and lower frequency (figure 12).

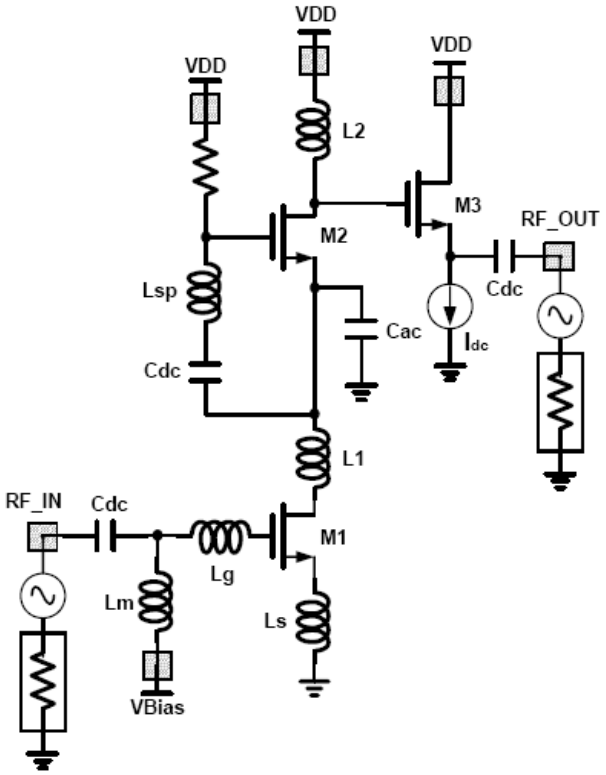


Figure 12: Wideband LNA design [3]

M_1 and M_2 are the cascoded transistors used for increased amplification in the gain. C_{ac} is used as a temporary ground for M_2 to use to be able to work in saturation region. C_{dc} is the dc blocking capacitor to not allow dc voltage to go through L_{sp} to the

node. The dc current flows through transistors M_1 and M_2 therefore, the dc current is saved and the power dissipation is also saved [3]. L_{sp} is used as a peaking inductor where it helps all the characteristics of the LNA to not degrade as fast and helps the system get even better values.

Body enabled LNA

The body enabled LNA is a narrow band LNA in which it uses the body terminal to forward bias the LNA to allow for the supply voltage to be reduced. The LNA is also cascoded to allow for an increase in the overall gain and reduction in the noise figure (figure 13). The forward body bias technique also increases the noise figure and gain performance [5]. The body terminal was achieved using triple well technology for each transistor. L4 is used to choose the resonant frequency to allow the LNA to work for specific frequency.

The input matching is achieved through source inductive degeneration in which L_1, L_2 are used. C_1 is also used to achieve better matching. Again C_3 is used as the temporary ground for M_2 so that it can operate in the saturation region. C_2, L_3 are employed for better matching networks between M_1 and M_2 [5].

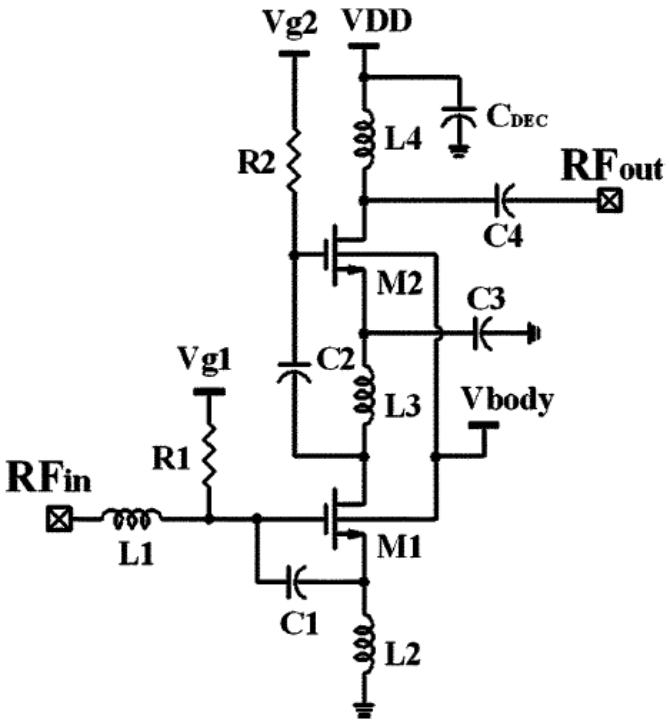


Figure 13: Forward body biased cascoded LNA [5]

2.4 Proposed work and simulations

Body Enabled Wideband LNA

The previously published papers discussed are LNA's in which the ideas were introduced to have a wideband LNA and forward body biased LNA. The proposal here is to combine the two previously published ideas and create a forward body biased wideband LNA. This will allow the designed LNA to use the advantages of both of the previously discussed LNA's.

Structure

The topology of the body enabled wideband LNA will be first started by designing a body biased LNA and then add a second stage to complete the second stage to create the wideband effect. Both sections will be designed around two different

frequencies. Then when they are combined they are going to make a wideband LNA that is body biased. This will lead to lower supply voltage and overall reduction in power consumption. Figure 14 is the proposed LNA to be implemented.

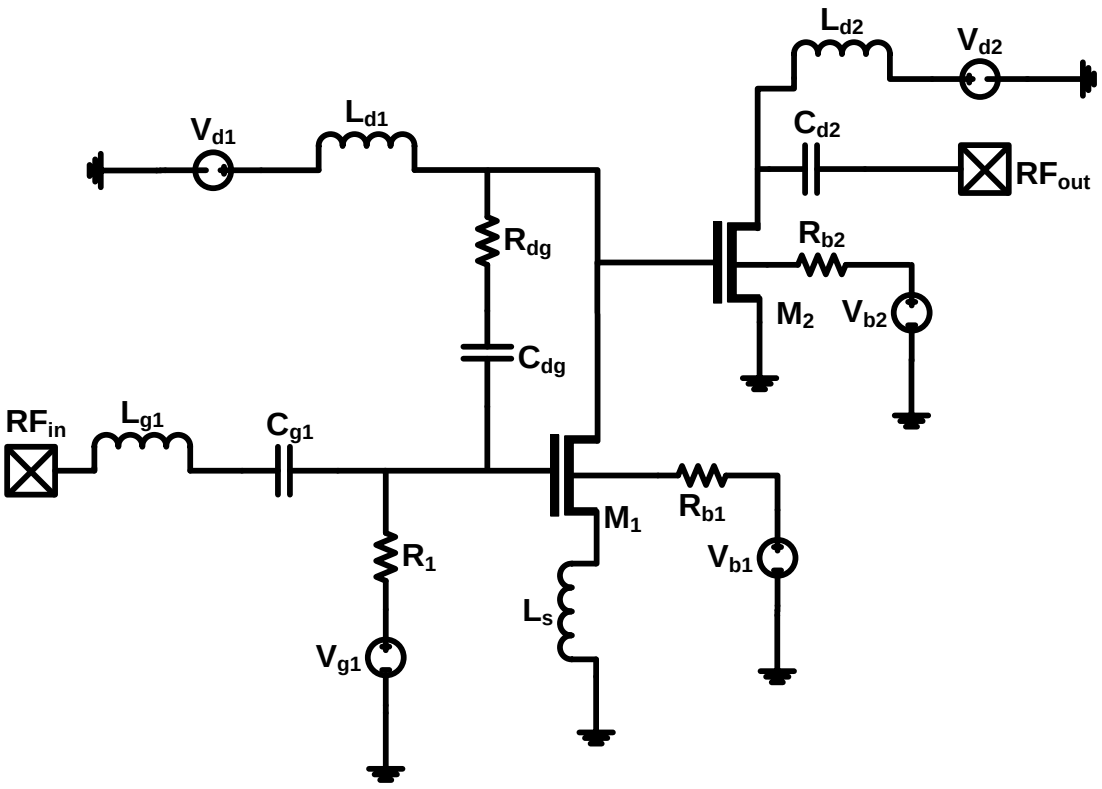


Figure 14: LNA implemented

L_{g1} and C_{g1} are used as the input impedance matching. They were calculated using hand calculations and then tweaked in simulation to achieve the best performance over the correct range of operation. L_s is also added to help with input matching. V_{g1} is the voltage added to power the gate of the M_1 to power the transistor.

L_{d1} and V_{d1} are added to achieve two things. First, it was added to designate the first frequency peak on M_1 for the first of two frequencies to achieve wideband availability. Second, it is there to power the gate voltage needed to turn on the transistor M_2.

C_{dg} and R_{dg} are the capacitance and resistance added to allow for feedback from the gate of M_2 to the gate of M_1. These will allow for increased gain over a large range. I choose this advantage over adding a second transistor stacked on top of M_1 because it was easier to implement and had a better range. Also M_2 used after stacked transistors had a harder time achieving and maintaining the second frequency for wideband operation.

L_{d2} is added there to choose the second frequency operation to force the whole system to be operating over a large range of frequencies therefore having wideband range of operation. V_{b1} and V_{b2} are the voltages added to the system to reduce down the overall voltage and therefore allow for the power consumption of the LNA to be reduced.

Lastly, the C_{d2} is added for the output impedance matching to make sure we meet specification for matching on the output of the RF system. This will make sure that the matching going into the mixer will be ready for the mixer operation.

Simulation

The wideband idea was implemented as stated above, but a resistive feedback was added to help with input matching and gain. Also inductive source degeneration was added to help with matching. There was also added matching network and capacitor on the output to help with input and output matching. These values were all hand calculated and tweaked to give the best results to meet specifications.

The idea of the LNA is implemented and the decision of the specifications was based on LNA's that were similar in design (either body biased or wideband). The input and output matching for my specification is -10 dB for both S_{11} and S_{22}. This was

chosen because most papers stayed around that range for both wideband and body biased designs. The bandwidth all references used was from 3.1 – 10.6 GHz. The goal I set was for 4 – 12 GHz so that I may be able to use the higher frequency translation. The gain of the LNA varied anywhere from 5 to 13 dB. Therefore a gain (S_{21}) above 10 dB should be implemented. The noise figure should not be greater than 5 dB at anytime during the bandwidth to be considered low noise. The comparison of the specifications and the results of my LNA design are seen in table 1.

Table 1: LNA comparison sheet.

Reference	**Vdd (V)**	**BW (GHz)**	**S21 (dB)**	**Noise Figure (dB)**	**S22 (dB)**	**S11 (dB)**	**P1dB (dBm)**
[6]	1.8	3.1 – 10.6	10-13	2.7 – 4.9	<-10.9	<-8.7	-19
[7]	*	3.1 – 10.6	9.5	5 – 5.6	<-8	<-8.6	*
[8]	1.2	3.1 – 10.6	7 - 10	3.9 – 5.8	<-13.7	<-5.7	-14
[9]	1.2	2.2 – 9	5 – 11	3.9 – 4.6	<-9	<-9.2	-8
Body Biased Wideband LNA	1.5	4.2 – 12.5	10 - 21	2 – 2.6	<-10	<-10	-9.43

The gain (S_{21}), noise figure, P_{1dB} and s-parameters are then plotted and displayed below to prove my results from table 1.

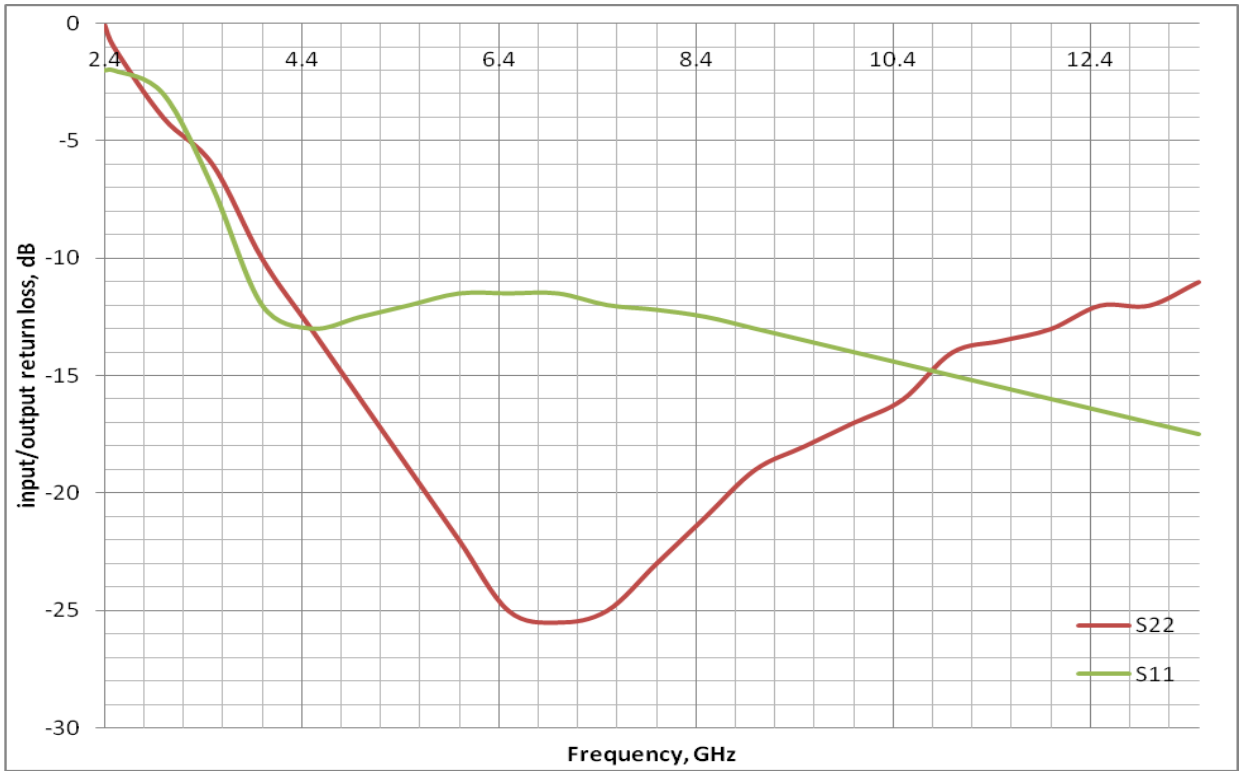


Figure 15: Input and Output matching of LNA

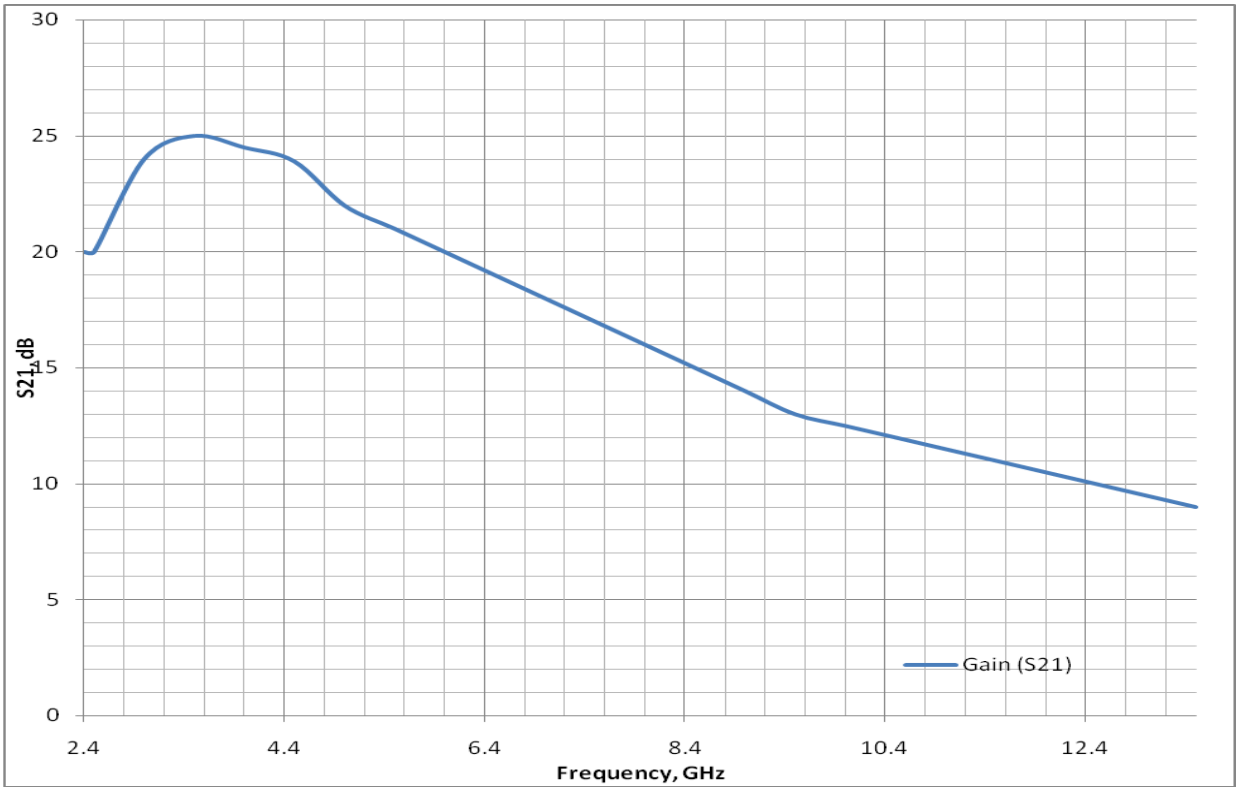


Figure 16: Gain of the LNA

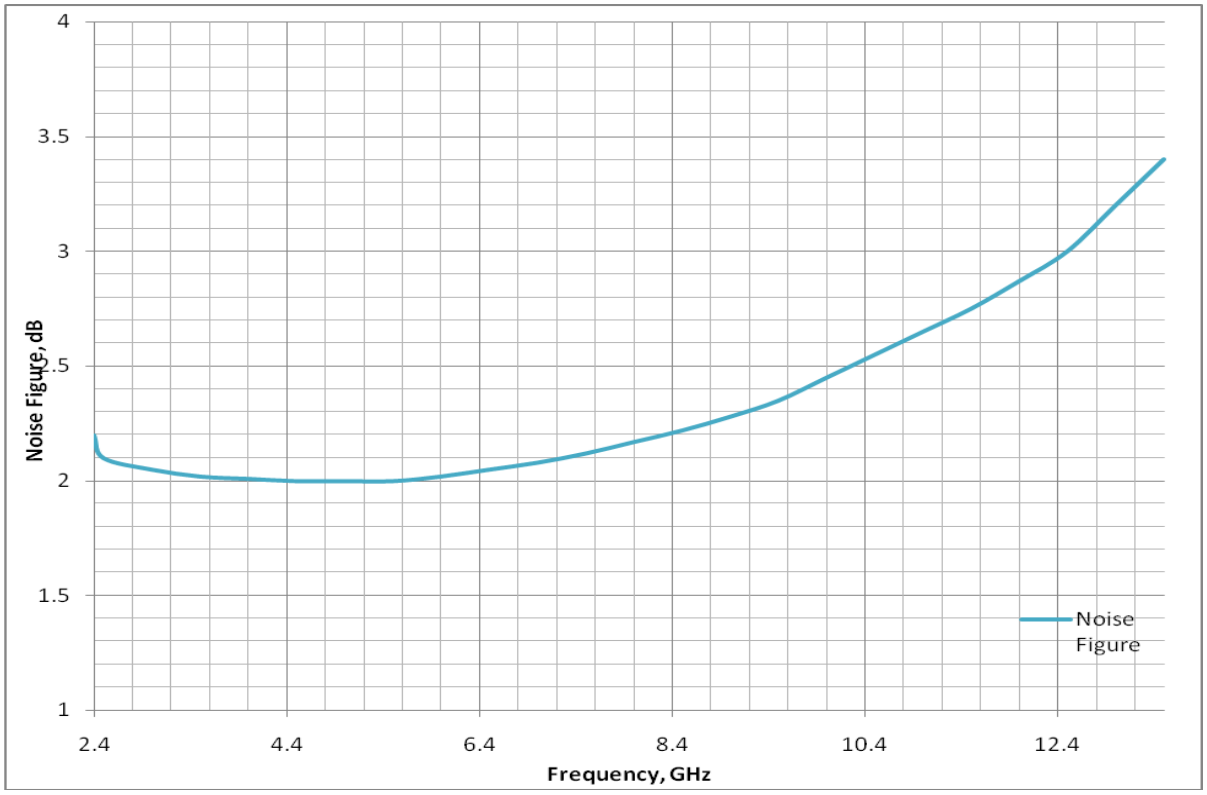


Figure 17: Noise figure of the LNA

The above graphs show that for the gain S_{21} the gain is above 10 dB until 12.5 GHz, which determines the upper bound range of operation. The input and output matching S_{11} and S_{22} is what determines the lower range of operations. S_{22} was the more strict range and it reaches below -10 dB at 4 GHz. This is how the range of 4 – 12 GHz was determined.

The noise figure image above shows that over the range of frequency range determined above the noise figure easily meets the specification of less than 5 dB to be considered low noise. The noise figure obtains a max of 3.4 dB as the largest noise within the range of operation.

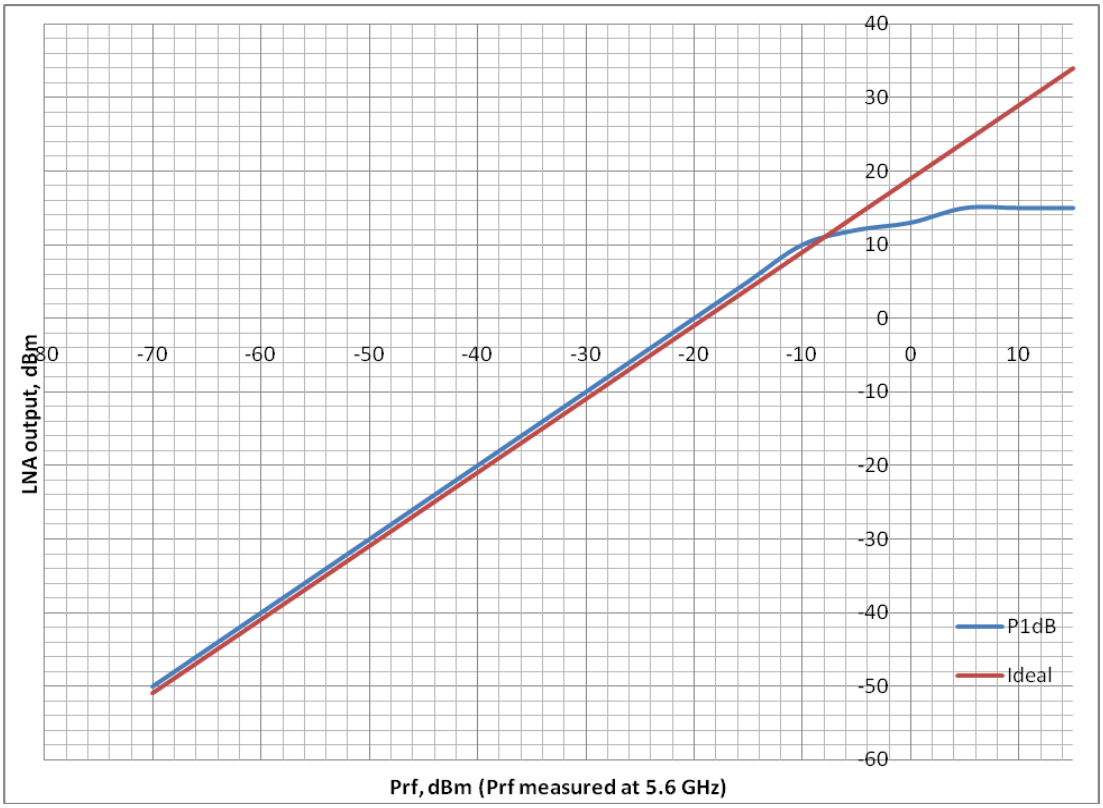


Figure 18: P1dB compression point for LNA

The P_{1dB} for the designed system is -9.43 dBm which is comparable to all of the published papers. The P_{1dB} was read during several different frequencies and they were all comparable to each other and posted is the frequency of 5.6 GHz which is in our range of operation.

Once table 1 proved that my design was better than previously published papers compared in the above table it was time to move onto the layout of the LNA. The layout was developed to achieve the smallest amount of parasitics by keeping the length of wires short. Also the layout was developed to meet all specifications designed in the schematic and simulation results. The LNA was tested in the design rule check (DRC) and layout versus schematic (LVS) verification to make sure it can pass all processing

rules to therefore allow for actual implementation onto a chip. The chip size of the wideband body enabled LNA is 750 µm x 512 µm.

Then once the LNA was laid out to be put on a chip and was DRC and LVS clean it was then re-simulated with all parasitics. The following is the chip layout and the simulation of the LNA again with parasitics.

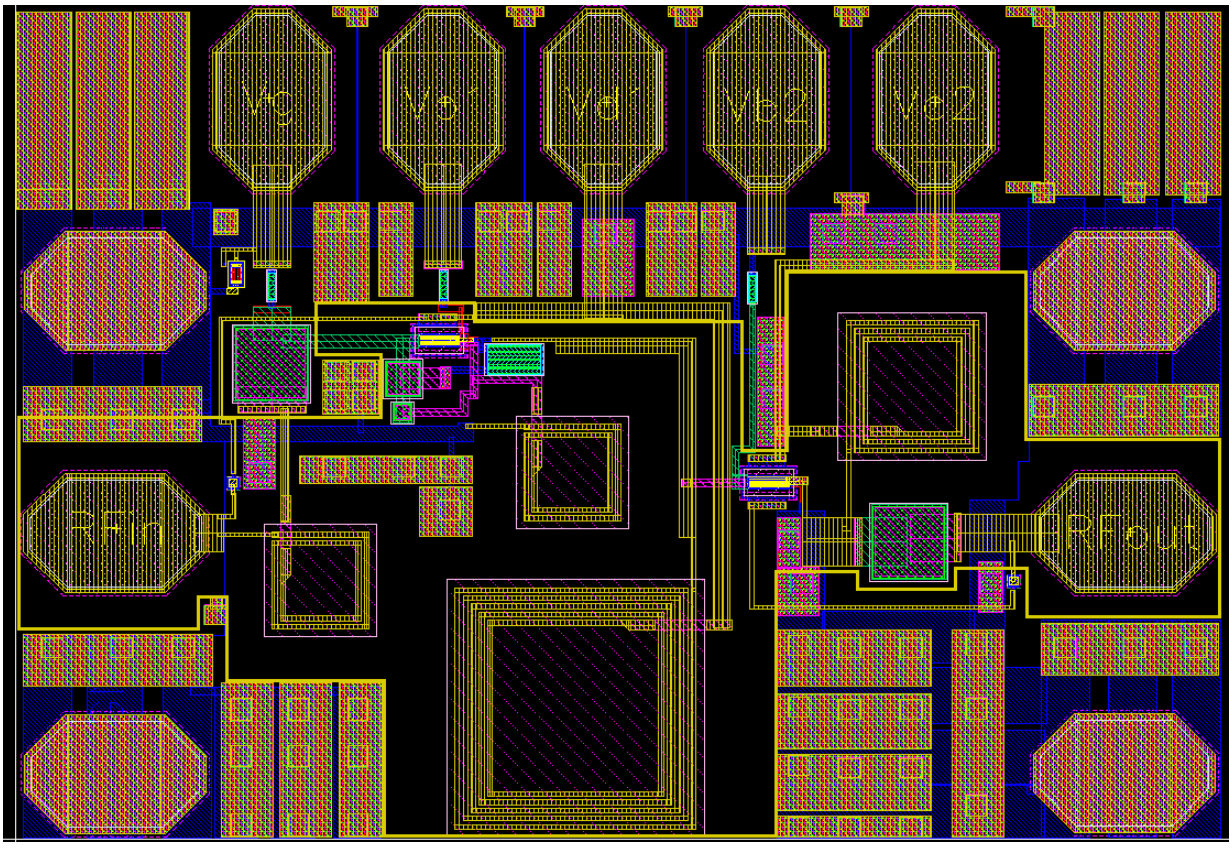


Figure 19: LNA layout (750 µm x 512 µm)

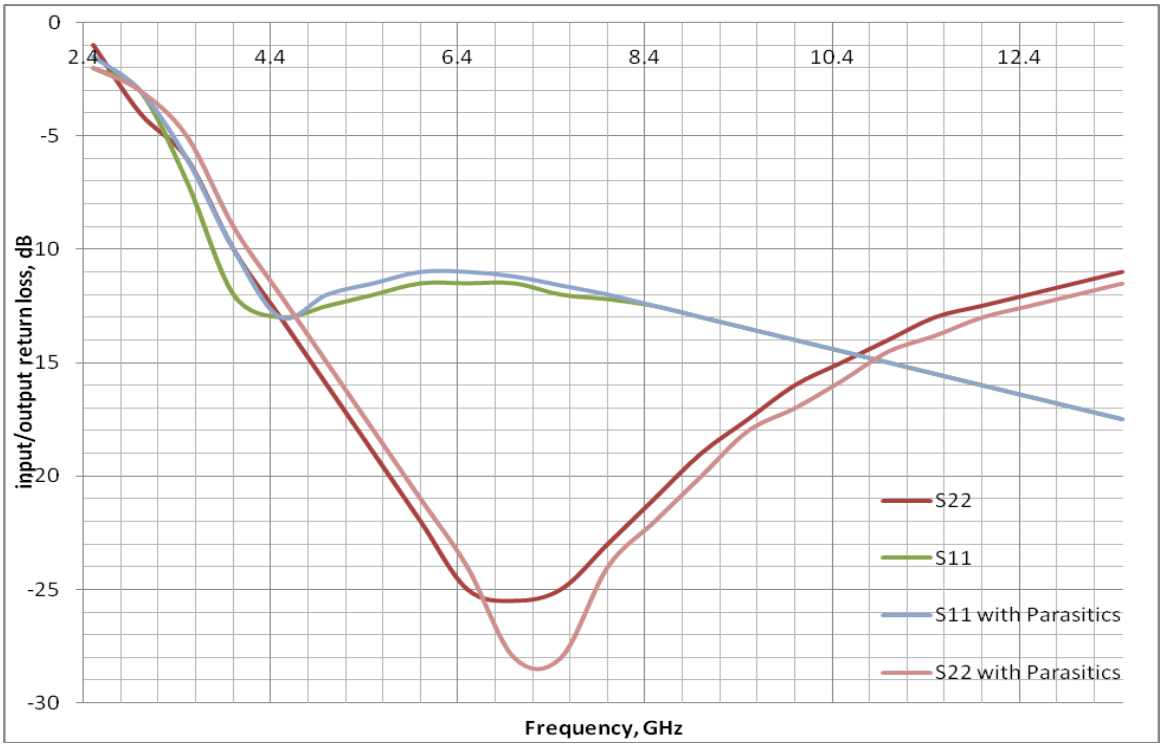


Figure 20: Input and output matching of the LNA along with parasitics

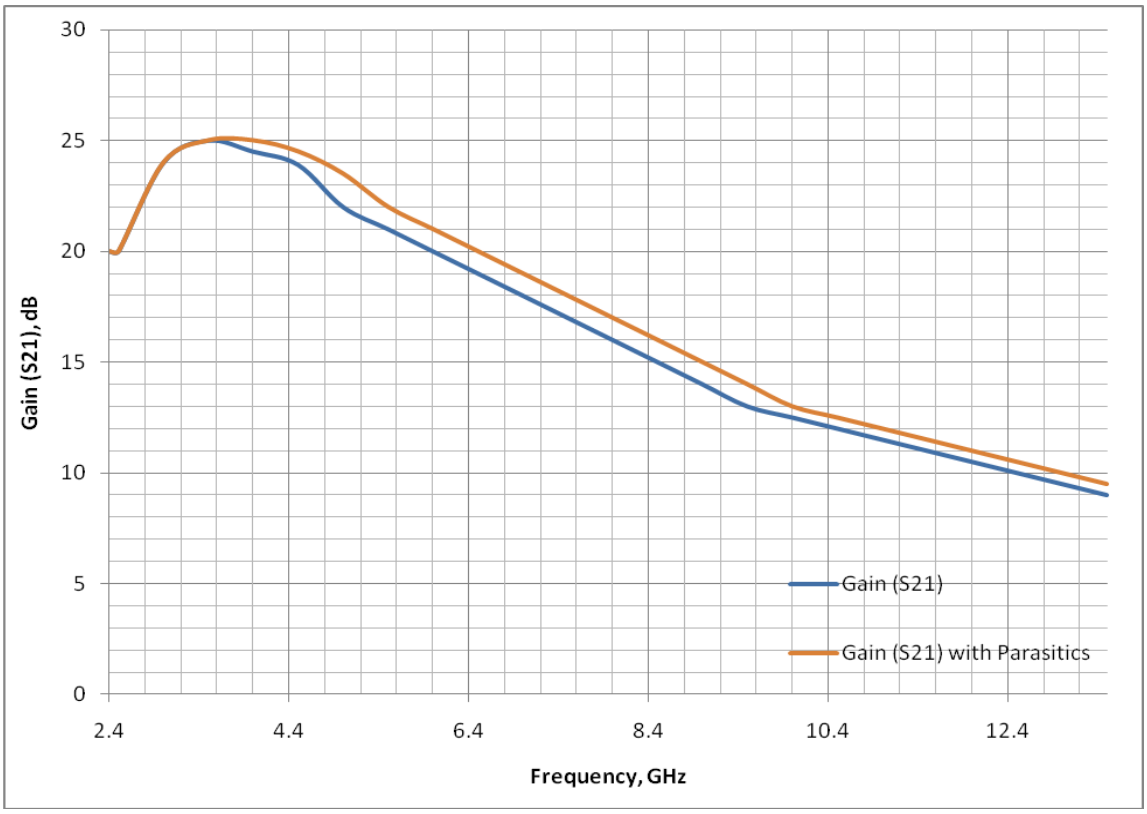


Figure 21: Gain of the LNA along with the Parasitics

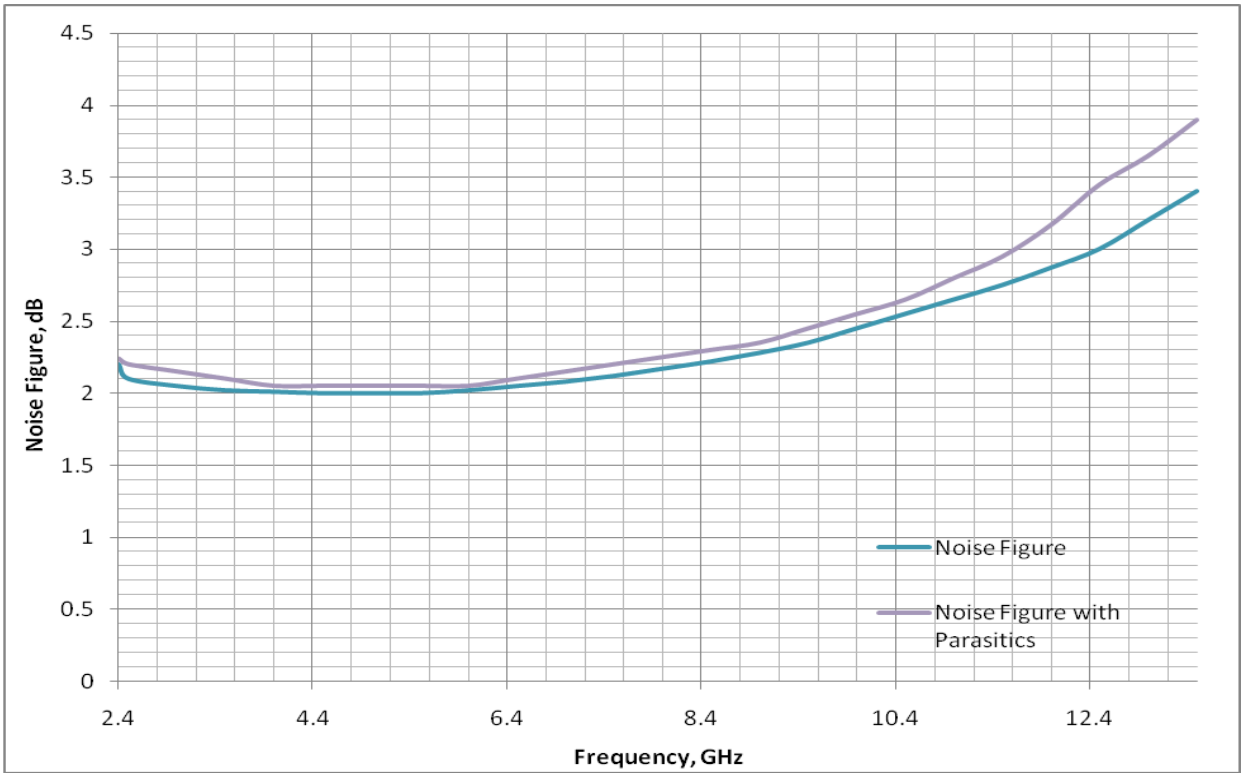


Figure 22: Noise figure of the LNA along with the parasitics

The above simulation results shows that gain (S_{21}) will remain the same while the biggest changes came from the input and output matching. S_{11} and S_{22} moved the frequency boundary to the left which actually increased the range of operation buy only by a few MHz which means that our system is now parasitic independent therefore we can infer that our system was laid out correctly and is now currently ready for development onto a chip.

Temperature simulations show the ability to maintain the results over a wide range of temperatures. The average range for chip testing is -30 degrees Celsius to 50 degrees Celsius. The nominal testing for all previous simulations was 27 degrees Celsius. The following is the temperature variations for the input/output return loss, gain, and noise figure.

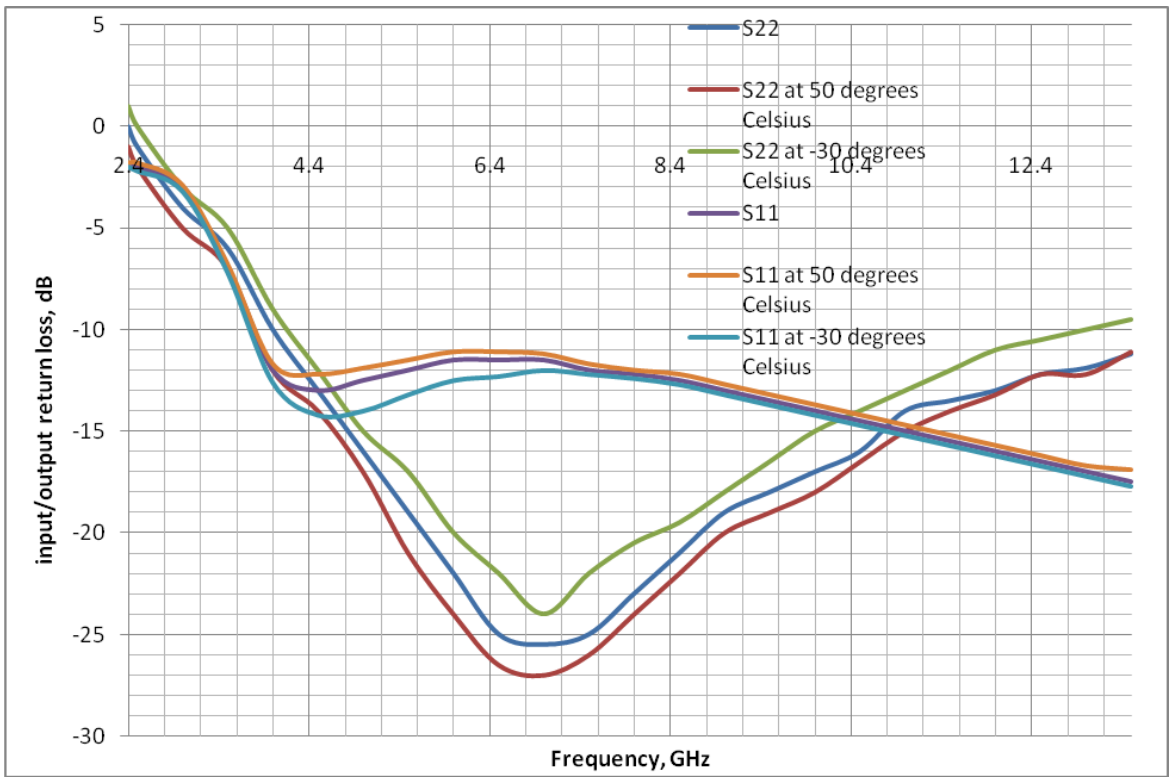


Figure 23: Temperature variation for S_{11} and S_{22} of the LNA

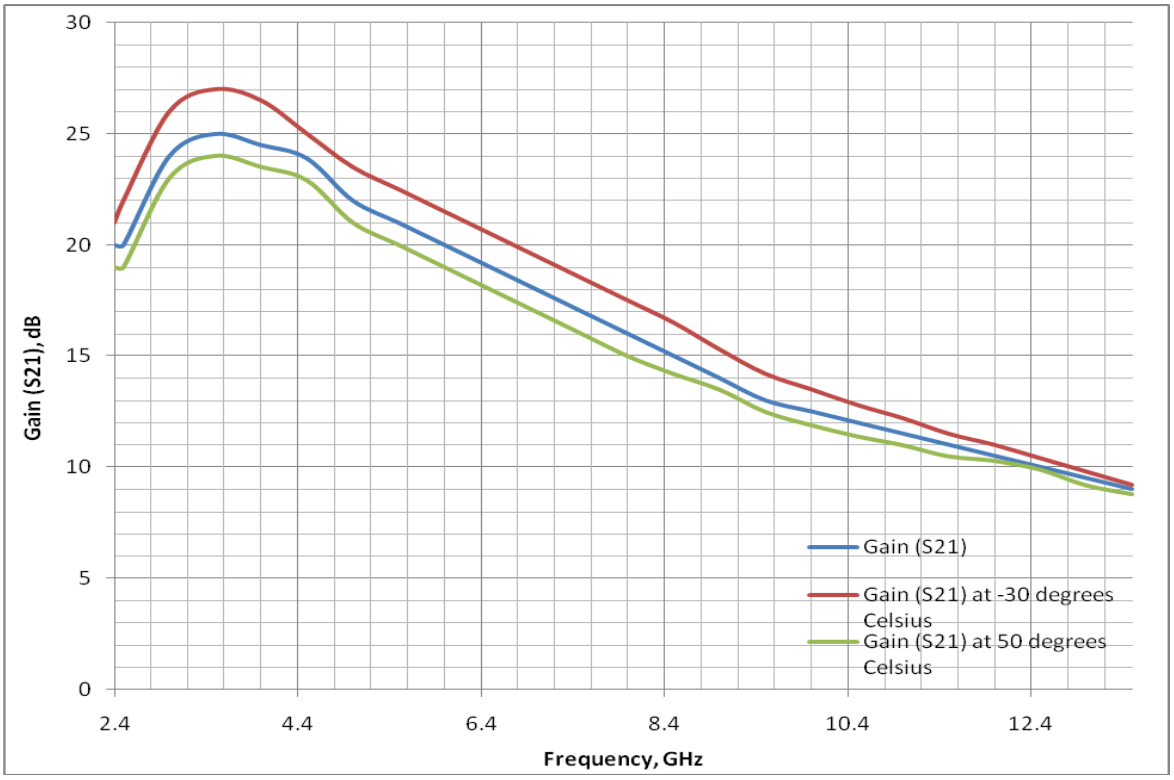


Figure 24:Temperature variation for Gain of the LNA

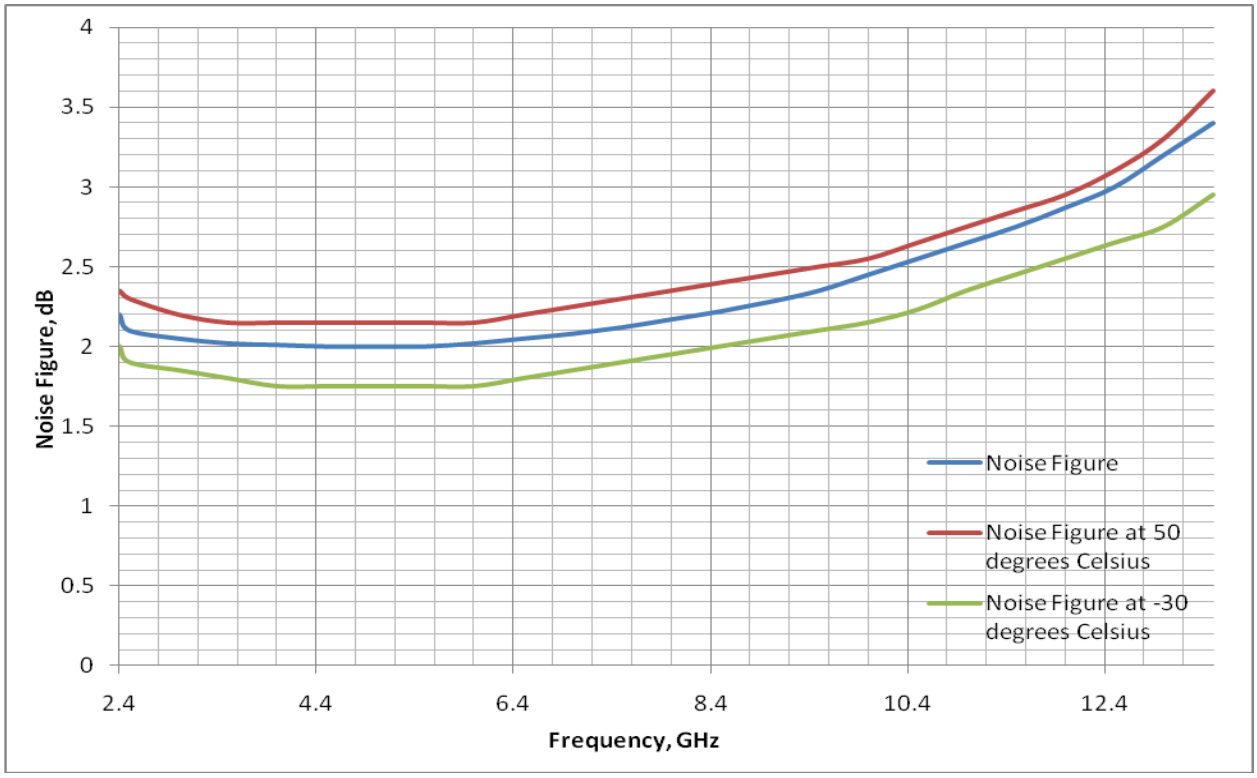


Figure 25: Temperature variation for noise of the LNA

Advantages

The body enabled wideband LNA will allow for ideal input/output impedance matching. The LNA will allow for lower supply voltage while still maintaining the large operating frequency for use in multiple different devices. The figure of merit comparison is seen in table 2 to show that the design of the LNA is better than previously published papers. The decision to include all three figures of merits was chosen to give a robust comparison to insure the developed LNA is the most successful.

Table 2: FOM comparison to recently published papers

Reference	**FOM_1**	**FOM_2**	**FOM_3**
[6]	59.4	47.59	90.07
[8]	64.82	51.19	91.02
[9]	51.51	40.39	75.11
This Work	64.84	57.23	98.31

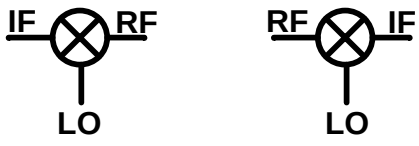
CHAPTER THREE

MIXER

3.1 Mixer Background Information

Mixers are a key process in RF circuits in which they are used to achieve frequency translation, but can also be used as phase detectors in PLL's [10]. Mixing allows for signals to be converted to different frequencies and therefore will allow for better processing. In the common mixer there are 3 different ports (RF – radio frequency, LO – Local oscillator, and IF – Intermediate frequency). Mixers will often involve trade-offs between conversion gain, linearity, noise figure, isolation, voltage supply, and power consumption.

Frequency translation is needed because filtering out a particular RF signal channel centered among many densely populated, narrowly spaced neighboring frequencies would require a high Q filter of extremely high accuracy. The signal becomes easier to manage if the RF signal carrier frequency can be reduced or down converted with in the communication system. The mixing is done by taking a set LO frequency signal multiplying it by the RF signal to give a suitable IF signal on the output (figure 26).



(a) (b)

Figure 26: (a) Up converter mixer (b) Down converter Mixer

RF mixing is a non-linear process that involves the instantaneous level of one signal affecting the level of the other at the output. This involves the two signal levels

multiplying together to any given instant in time and the output is a complex waveform consisting of the product of the two input signals. If one of the inputs is a sinusoidal signal, then the spectrum of the other signal is a shifter in frequency as a result of time-domain multiplication. If both signals are cosine then equation 20 would be the translation to the IF frequency.

$$V_o = [A_1 \cos(\omega_1 t)][A_2 \cos(\omega_2 t)] = \frac{A_1 A_2}{2}[\cos((\omega_1 - \omega_2)t) + \cos((\omega_1 + \omega_2)t)] \qquad (20)$$

Equation 20 shows that the signal will produce 2 different signals. It will produce a signal adding the frequencies together this is called the up conversion. The other is when the frequencies are subtracted from each other and is considered the down conversion (figure 27).

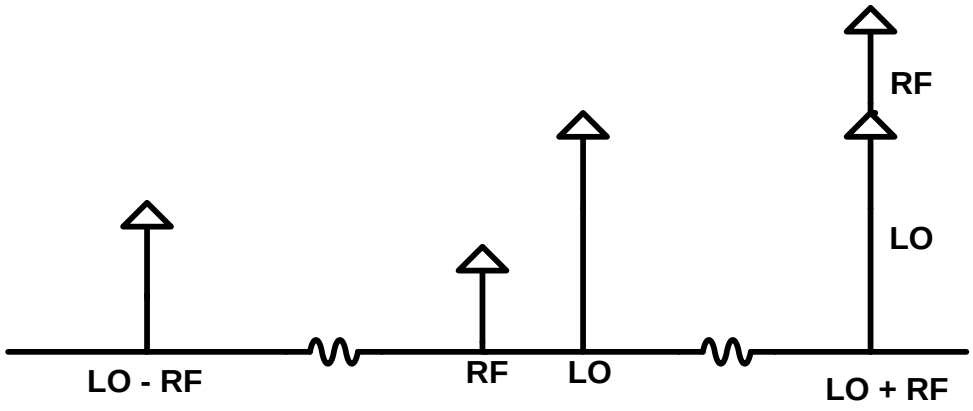


Figure 27: Up and down conversion

This image represents the normal filter response that comes after the mixer. The mixer will produce both of these images; in design, you either want one or the other. This means that one has to be taken out usually by a low or high pass filter depending on which of the responses you want. The overall block diagram with the filter is seen in figure 28. Also, the filter can be used to suppress certain harmonics that exist due to the

mixing process. These harmonics will occur at odd harmonics of the system and usually need to be eliminated for correct processing.

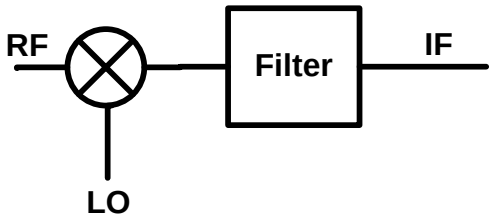


Figure 28: Block diagram of mixer with filtering

The down converter (figure 26b) is used in a receiver and will convert a higher signal to a lower signal to be easier to manage within the rest of the processes of the chip. The input of the down converter will be RF and the output will be the IF (figure 26b). The down converter isolations of importance are between (LO-IF, RF-IF). The gain is calculated by taking the power of the IF divided by the power of the RF (equation 28).

$$G_c = 10\log\left(\frac{P_{if}}{P_{rf}}\right) \tag{21}$$

The up converter (figure 26a) is used in a transmitter and will convert a low frequency to a higher frequency to be used for transmitting wirelessly to a destination. The input of the up converter will be IF and the output will be the RF (figure 26a). The up converter isolations of importance are between (LO-RF, IF-RF). The gain is calculated by taking the power of the RF and divide by the power of the IF (equation 22).

$$G_c = 10\log\left(\frac{P_{rf}}{P_{if}}\right) \tag{22}$$

The gain of the up/down converters is used to determine if the mixer is active or passive. An active mixer is if the gain is above zero and the passive mixer is when the gain is zero or below. The most common active mixer is the gilbert cell. Passive mixers are usually treated similarly to a switch. The gilbert cell mixer is a passive mixer with a gain stage.

Additionally, there are single balanced and double balanced mixers. Single balanced mixer will either suppress either the LO or RF signal but not both, but the double balanced mixer will suppress both of the input signals. The most common is the double balanced because most applications require that both inputs be suppressed. The double balanced mixer has all the ports inherently isolated from each other, and has increased linearity while having improved suppression of the spurious products. The double balanced also has high intercept points and is less susceptible to supply voltage noise. The single balanced does not require a high LO drive level and only needs a single balun (balanced signal to unbalanced signal).

3.2 Mixer Specifications

Mixers have several different aspects to consider during a design. They are conversion gain, linearity, noise figure, isolation, spurious free dynamic range, voltage supply, and power consumption. Also, the leakage between mixer ports is very important so that no signal is transferred between ports that are unwanted. The derivation and characterization of these are described in the below sections.

Conversion Gain/Loss

Conversion gain/loss is a measure of efficiency of the mixer and is measured in dB. It is measured by the ratio of the level of one of the output sidebands to the level of input (equation 23).

$$G_c = \frac{P_{out}}{P_{in}} \tag{23}$$

CMOS devices the conversion gain/loss is usually measure in terms of voltage gain instead of power gain because of the lack of precisely defined characteristic impedance. The voltage conversion gain/loss is defined as the ratio of RMS voltage of the desired output signal divided by the RMS voltage of the input signal.

$$G_{cv} = \frac{V^2{}_{out}}{V^2{}_{in}} \tag{24}$$

Ideally the mixer gain will be ½ of the amplitude of the LO signal. The gain of a mixer is always measured with a low enough input signal level so that all of the non-linear effects are negligible.

Noise Figure

Noise figure is defined as the ratio of SNR (signal to noise ratio) at the output port to the SNF of the input port and is measure in dB. Wireless communication systems receive a signal that is very weak; therefore, the noise within the system is always important because if there is any noise in a weak signal it is ruined with the slightest amount of noise when processed. Noise figure is often taken as the noise factor (equation 25). An ideal noise factor would be 1.

$$NF = 10\log(F) = 10\log\left(\frac{\frac{S_i}{N_i}}{\frac{S_o}{N_o}}\right) \quad (25)$$

SSB (single sideband) assumes only the input signal and not the image frequency to be considered. This is the case when a band pass filter is added to the front of the mixer. It has difficulty associated with providing LO energy while maintaining separation between LO, RF, and IF signals for broad band applications.

DSB (double sideband) considers both sidebands are available thus it has twice as much power available at the IF port compared to the SSB. This means that the conversion gain/loss is 3 dB less than that of the SSB.

Isolations

Isolation is a measurement of how much feedthrough of the input and LO signal to the desired at the output band. Also included in this is the amount of leakage that will occur between each of the 3 ports. Isolation is defined as the power of a port measured at a different port (equation 26, 27, 28). Ideally the port to port isolation would be -∞ dB. There is also reverse isolation which is the LO and output port back to the input port. This is very important especially in minimizing the interference to other receivers.

$$Isolation_{LO\_IF} = P_{LO}\,@\,IF \Big/ P_{LO} \quad (26)$$

$$Isolation_{LO\_RF} = P_{LO}\,@\,RF \Big/ P_{LO} \quad (27)$$

$$Isolation_{RF\_IF} = P_{RF}\,@\,IF \Big/ P_{RF} \quad (28)$$

Poor isolation is a significant problem and usually is within SoC (system on chip) design and layout of a chip. This is because of the proximity of the components and the relatively low resistivity of the substrate. The bad isolation can cause DC offset at the mixer output resulting from the self-mixing of the input signal when it finds its way to the input [11].

Linearity (1 dB Compression Point)

The 1 dB compression point (P_{1dB}) is used with the conversion gain/loss to allow for a fair comparison of the mixer topologies. The mixer has nonlinear amplitude above certain input levels resulting in gain compression characteristic. Above this point the IF fails to track the RF input power level. Normally a 1 dB rise in RF power will result in a 1 dB rise in the IF power level [12]. P_{1dB} is the input power level where the output signal level is dropped by 1 dB from the ideal linear case (figure 29). The 1 dB compression point also gives rise to the dynamic range. The dynamic range is considered to be the range of operation for the mixer which is calculated by taking the difference between the 1 dB compression point and the minimum discernible signal (MDS) [6]. The MDS is dependent on the noise floor of the mixer.

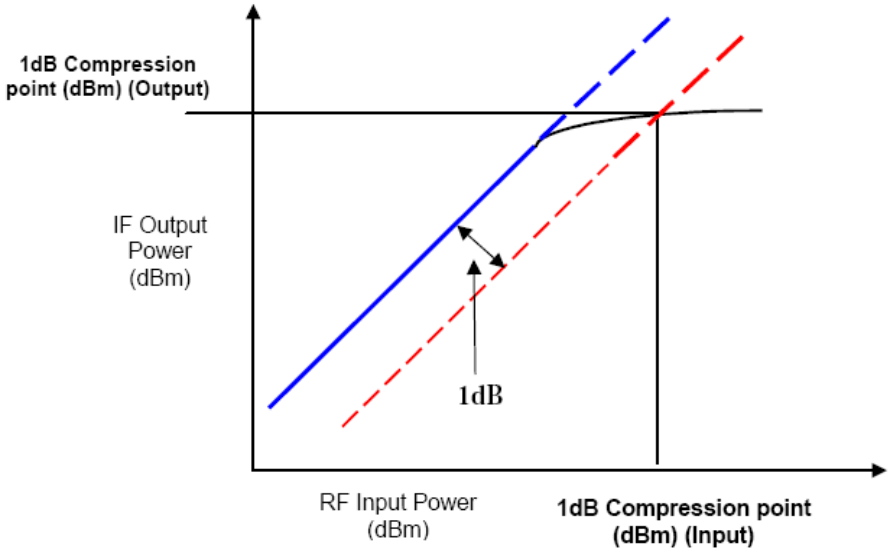


Figure 29: 1 dB compression point [12]

Linearity (3rd Order Input/Output Intercept Points)

The mixer itself will experience a limitation on the input signal strength. This is called the intermodulation distortion (IMD). The IMD is measured by applying to closely spaced input tones at different frequencies (equation 29). The intermodulation ratio (IMR) is the difference in dB between the desired output and spurious signal. The main concern is the 3rd order intercept point (IP3 or IM3).

$$F_{imd} = (2f_{1or2} +/- f_{2or1}) +/- f_{LO} \tag{29}$$

This is an area of concern because if we look at the 3rd order products (equation 30) and once they are multiplied with the LO frequency the IMD will have a chance to fall within the filter bandwidth of the output and therefore cause an interference to a desired signal. This will cause a reduction in the P_{1dB} which is not desirable for any mixer. The input signal and desired output signal are defined as (IIP3 and OIP3

respectively) and are calculated in equation 31. IIP3 is an entirely imaginary point at which the 3rd order product becomes as large as the direct product. It is common practice to extrapolate the intercept point from the data taken to at least 10 dB above P_{1dB} (figure 30). The IIP3 is especially important in wireless applications because the 3rd order product with two adjacent channels could land in the next channel over causing errors.

$$F_{imo3} = (2f_{1and2} - f_{2and1}) - f_{LO} \tag{30}$$

$$OIP3 = {(P_{if} - P_{imd})}/{2} + P_{if} = IIP3 + G_c \tag{31}$$

IIP3 is important in mixers because it is situated after an LNA and therefore subjected to substantially stronger signals coming from the LNA [11]. The 3rd order products will rise exponentially relative to the power of the signals which produce them. The ones produced within the first mixer are usually what define the receiver's overall IIP3 performance [11].

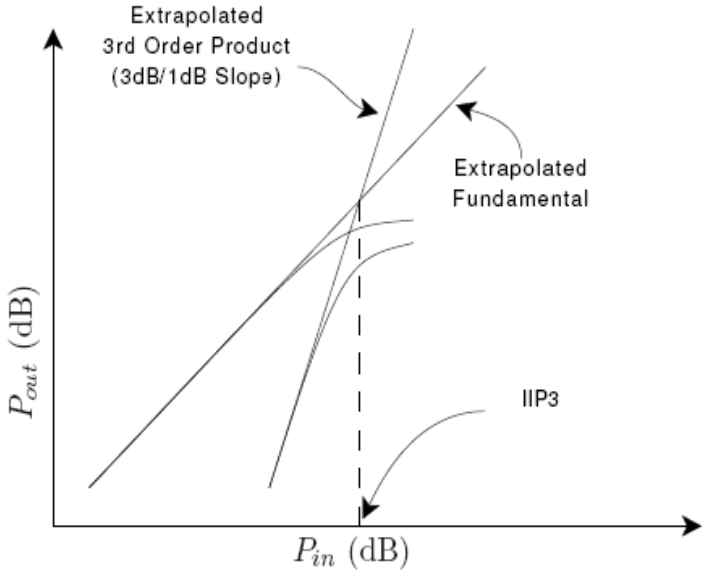


Figure 30: Extended gain comparison to show the 3rd intercept point [11]

Figure of Merit (FOM)

The FOM is a way to take all of the specifications of importance and combine it to a single equation and weight each of them to the most importance. The figure of merit used for mixer is seen in equation 32. This FOM is considered a standard for mixer because every recent published paper uses this FOM as comparison to other published papers.

$$FOM = 20\log(f_{RF}) + G_c - NF + IIP3 - 10\log(P_c) \quad (32)$$

3.3 Mixer Topologies

This section will discuss the different mixers that have already been published. These papers along with others will be used for comparison to the works developed in this paper.

Passive CMOS Mixer

The passive mixer will have a conversion gain less than or equal to zero. The passive mixer operates by running the transistors directly as switches (figure 31). There is no active gain state in the passive mixer which is why the conversion gain is low. The passive mixer basically forms a voltage divider with the source and load which attenuates the signal similar to that of the gilbert cell mixer in that it has no DC current and will switch on/off. The LO ports of the passive mixer work as switches to determine which of the transistors are on and therefore determining the RF signal that is feedthrough to the IF port. When LO+ is high RF+ goes to IF- and RF- goes to IF+ and vise versa when LO- port is high.

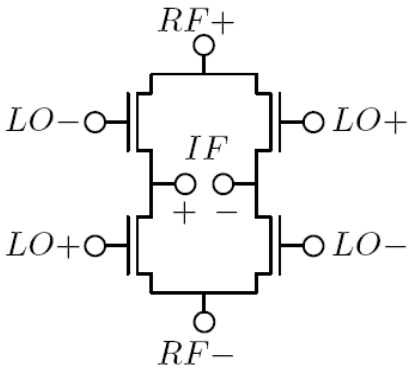


Figure 31: Passive Mixer

The passive mixer is often more linear than the rest of the mixing structures. This is from the large use of transistors to better approximate the ideal switches and the fact there is no amplification stage [11]. The passive mixers will have a considerably larger conversion loss and the larger transistors will require a higher drive from the LO port. The passive mixer also has no flicker noise because there is no DC current into the quad transistors. No current needs to flow through the transistors because they are only being treated as resistors to be either on or off when desired.

The resistance that is used to calculate the turn on resistance of the transistors in the passive mixer is in equation 33. Therefore, to find the conversion loss resistances, it can be plugged into the circuit because when the transistors are treated as switches, they can be replaced with resistors when finding the small signal (figure 32). The resistance R_{on} uses the threshold voltage which is why the body driven topologies can help reduce the resistance and overall reduce voltage of a passive mixer.

$$R_{ON} = r_{ds} = \frac{L_g}{\mu_n C_{ox}((V_g - g_c v_{RF}) - V_{th} - V_{ds})} \tag{33}$$

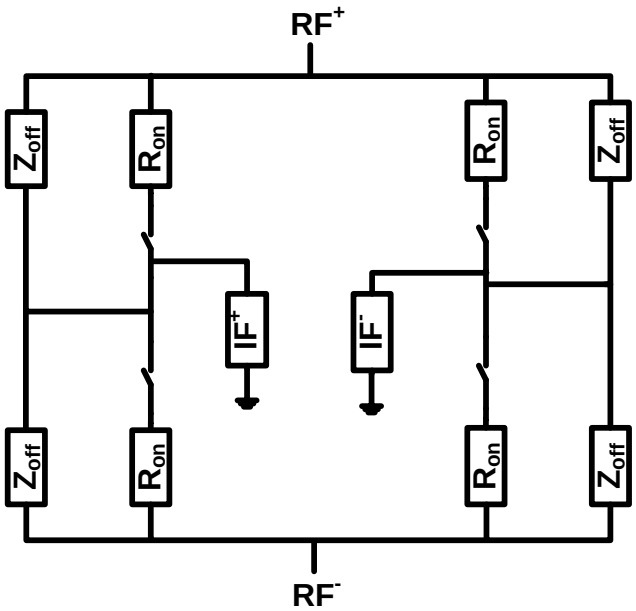


Figure 32: Transistors replaced with resistors for conversion loss calculation [13]

It should be noted that a resistor is added to the output to convert the signal back to voltage and for ease in calculating the conversion loss. Equation 34 is the conversion loss for the passive mixer. Only the switching thermal noise needs to be calculated (equation 35) because it is the biggest factor in the noise. The other noise factors can be excluded due to the fact they will not add much compared to the thermal noise. Isolation is also measured similarly to that discussed earlier.

$$G_c = 20\log\left(\frac{2}{\pi}\left(\frac{Z_L}{Z_L + R_{ON} \,//\, Z_{off}}\right) - \frac{2}{\pi}\left(\frac{Z_L}{Z_L + Z_{off}}\right)\right) \tag{34}$$

$$F = \frac{1}{g_c^2} + \frac{F_{mixer}}{g_c^2 k T_o R_s} = \frac{1}{g_c^2} + \frac{8kT_o \big/ g_{ds}}{g_c^2 k T_o R_s} \tag{35}$$

Wideband mixer

A wideband mixer is designed as a passive mixer but with its range of operation to be over several GHz while still maintaining all of the specifications. A wideband mixer will have to operate around the threshold voltage which will make it linear but at the same time because it is near this it has the chance to become unstable. This is why my design will allow for relaxation of the threshold voltage by using the body driven topology.

The way to obtain wideband region of operation is to design the matching network to allow the specifications to meet specifications over a wide range of frequencies. The wideband design is advantageous because it will allow a transceiver to not only operate at a certain frequency but other frequencies if the user needs. Figure 33 shows a designed wideband mixer used for a range from 2 – 9 GHz.

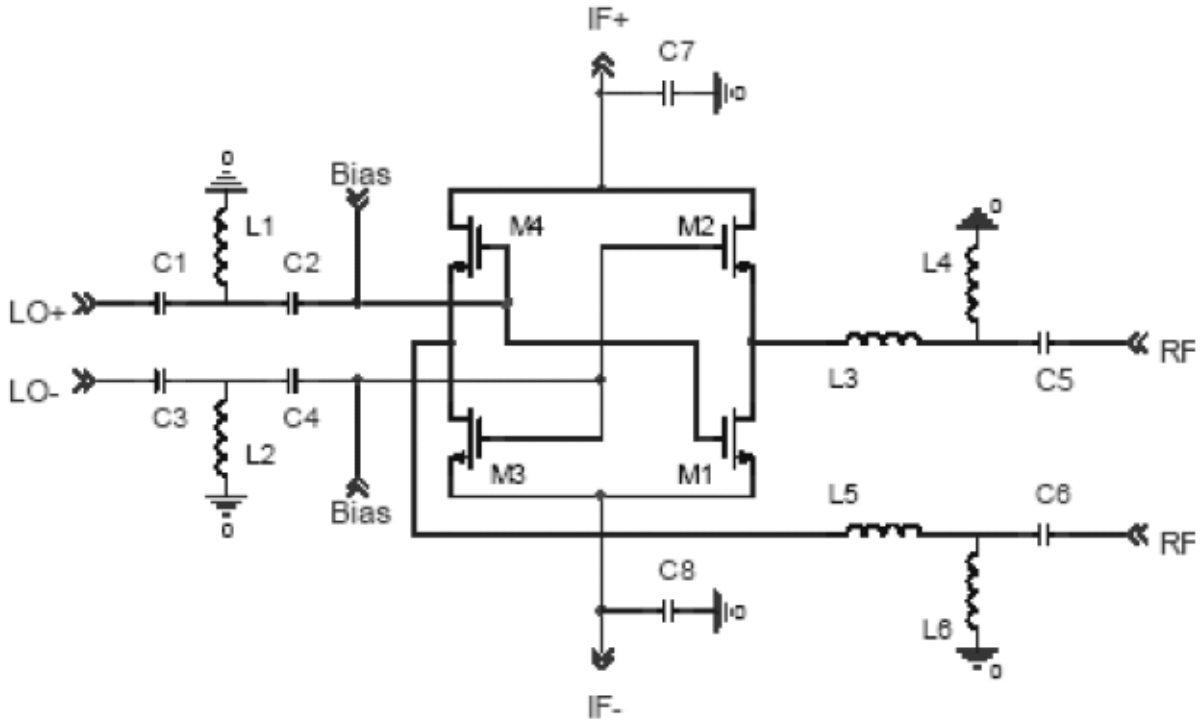


Figure 33: Wideband mixer design [14]

Body Enabled Mixer

The body enabled mixer is fairly new idea and has not been developed for the passive mixer. Which means a good comparison will be the gilbert cell mixer which is the passive mixer with a gain stage.

The body enabled gilbert cell mixer uses the triple well technology. The body terminal used for this is to drive the RF port by coming through the body terminal of the transistor. This allows for complete elimination of the transistors originally used for the RF port. The switching action is provided by the gate, while the transconductance is obtained through the body (figure 34).

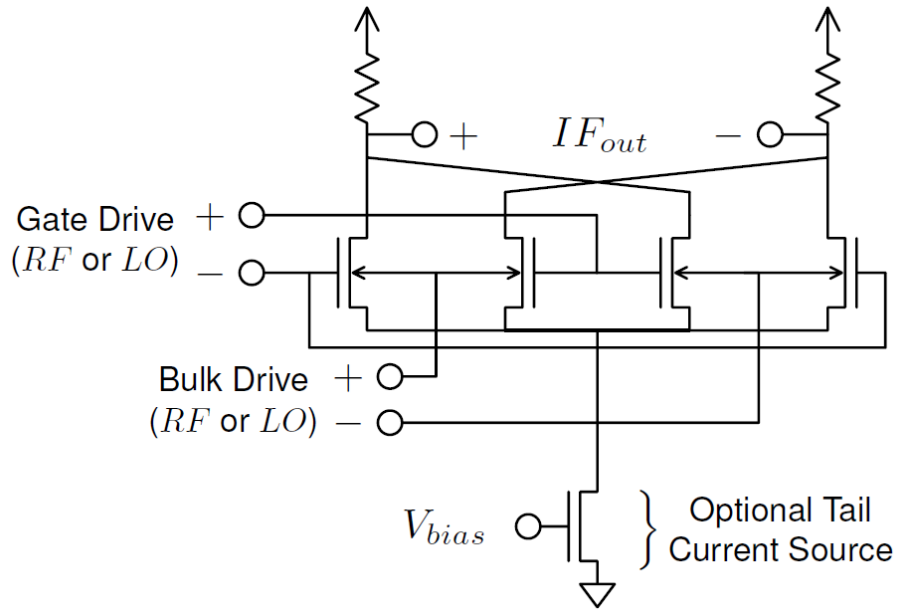


Figure 34: Gilbert cell mixer with body driven technology [11]

The LO +/- are the antiphase signals from the local oscillator that are used to switch M_1-M_4 on or off. When the transistors are on, they are held in the saturation region by a large V_{ds}. This ensures that the gain is reasonably high enough. If the transistors are off, they are held in the cutoff region. This allows for the RF to pass

through the back gate the transistors that are on. The RF input is now inverted when it appears at the IF output, thus the RF input is commutated by the action of the local oscillator and hence converted to desired IF frequency.

3.4 Proposed work and simulation

Body Enabled Passive Mixers

Body enabled mixers address the continuing trend of the supply voltage being reduced to allow for low voltage headroom. This means that the transistor threshold level is lowered. Previous passive mixers have not implemented any such idea to help with the lowered voltage supply. Passive mixers without body enabled structure and with lowered supply voltage would see a considerable decrease in key specifications (see section 3.1). The body enabling implemented for this mixer is the body driven technology which will allow for the supply voltage to be reduced and therefore lower power dissipation.

The body enabled technology will also allow for the RF signal to come through the body terminal therefore freeing up the drain terminal of the transistor. Also compared to the RF at the drain the specifications are all increased dramatically.

Structure

The structure to be implemented as a passive mixer with the body driven technology is the ring quad structure (figure 31). The body driven technology will allow for increases in the specifications. The RF port will also include a bias voltage will be

added to help with the power consumption of the system (figure 35). Also included in this structure is input and output matching of the mixer itself.

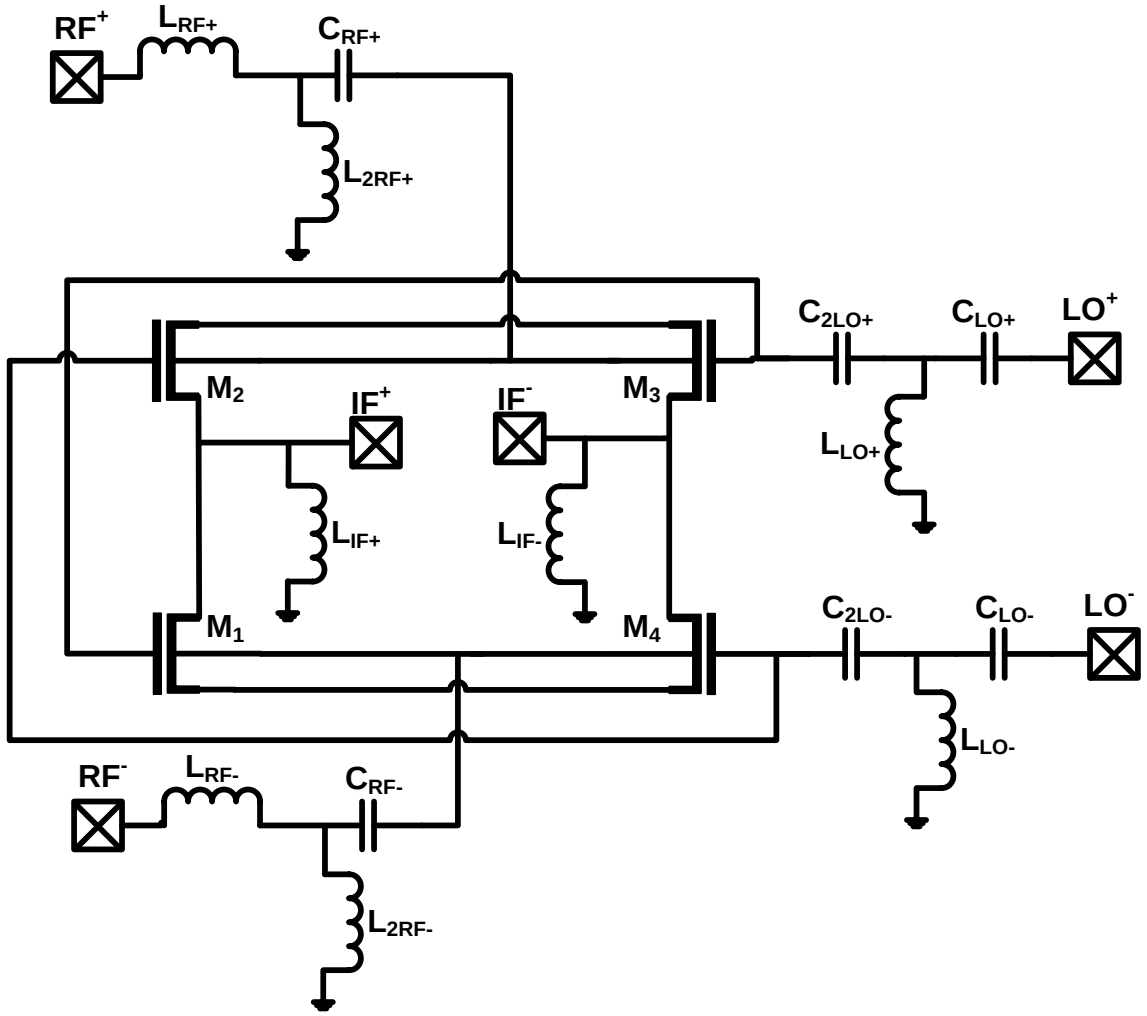


Figure 35: Body driven wideband mixer

The passive mixer has LO+/-. The LO+/- are designed to be identically opposite. This is necessary to allow the signal to make sure there is no feedthrough between RF+/-. If they are not opposite, there will be a time in which all gate will be on and will cause errors in the IF+/-. The same can also be said if all gates were off for a certain period. LO+/- also need high translation between on and off setting for the gate to cut

down the time were they are both in the on/off state during the switching period. LO+/- will have $L_{LO+/-}$, $L_{LO2+/-}$, and $C_{LO+/-}$ to help with the input matching.

The passive mixer has RF+/-. The RF+/- is where the signal comes from the LNA discussed in previous sections. Similar to the LO+/- the RF+/- will need directly opposite signals. It should be noted that coming from the LNA which only has one signal there requires a converter to take the output from the LNA and create an opposite signal with the same amplitude and frequency to be used as the RF-. Also RF+/- will have a matching network to help the input matching at each. The input matching network for the RF+/- consists of $C_{RF+/-}$, $C_{2RF+/-}$, and $L_{RF+/-}$.

Finally, the output IF+/- also requires an inductor $L_{if+/-}$, which is the inductor used for output matching of the system. Each of these components was hand calculated, but once they were inserted into the system the hand calculations were not very accurate. Therefore, each matching network had to be resimulated to vary each component to get the value that allowed for the specifications to be met. It should be noted that each component in the positive and negative had to be equal to each other to be a symmetric system.

Simulations

The wideband idea was implemented as stated above. The idea of the mixer is implemented and the decision of the specifications was based on passive mixers that were similar in design (either body driven gilbert cell or wideband passive). The input and output matching for my specification is -10 dB for both S_{11} and S_{22}. This was chosen because most research papers stayed around that range for both wideband and body driven designs. The designed bandwidth is from the mixers so that the overall

system will remain consistent throughout the two components. The gain of the published mixers varied anywhere from -6 to -12 dB. I decided to go for a gain (S_{21}) of 6 dB or below to be used. That way I will be all other published papers. The noise figure should be not greater than 10 dB at anytime during the bandwidth to be considered for this mixer because all other published papers had a range from 9 to 14 dB.

Table 3 shows the comparison of the specifications and the results of my mixer design. To show the advantage of the body driven mixer to a regular mixer with just a forward bias voltage to body, which I also simulated to achieve robustness in my simulation results, and also to show that I chose to put the RF signal to the body of the mixer instead of the drain. It should also be noted that all gains of the mixers used were the maximum gain attained during the range of operation, but it also met the minimum requirement of greater than -10 dB. Also, the noise figure is the maximum noise at any point of the range of operation.

Table 3: Mixer comparison

Reference	**Vdd (V)**	**Power (uW)**	**Gain (dB)****	**Noise Figure (dB)**	**P1dB (dBm)**	**BW (GHz)**
[15]	1.25	N/A	-6	10.6	5.5	2.4
[16]	N/A	N/A	-6	9.3	3	N/A
[14]	.45	0	-6.4	N/A	4 – 6.5	2-9
[17]	1.5	300*	-11.4	14.7**	25.2	19 - 26.5
Passive Mixer	.5	0	-6.8	12.7**	N/A	5 - 15
Body Driven Passive Mixer	.42	~0	-5.27	8.9**	45	4.5 - 13

* Current through matching network
** Highest gain point and highest noise point

The gain (S_{21}), noise figure, P_{1dB} and s-parameters are then plotted and displayed below to prove my results from table 3.

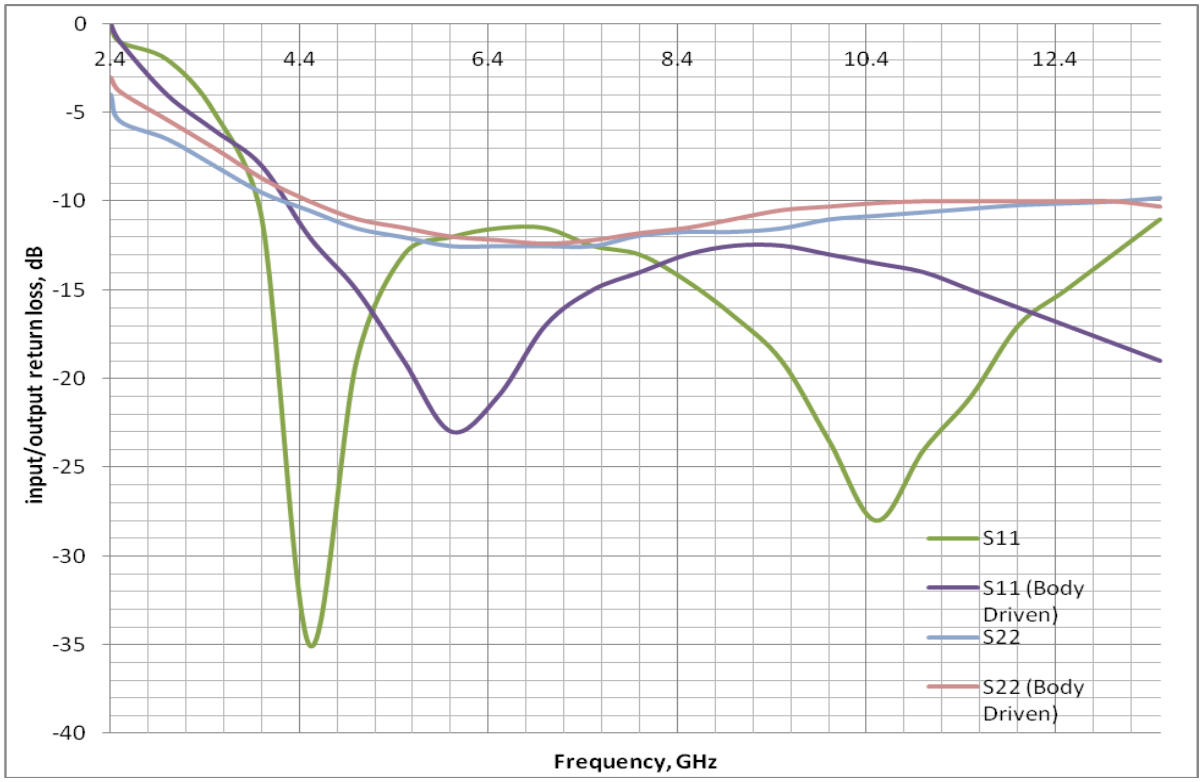


Figure 36: Input and output matching comparison to body driven passive mixer to a regular passive mixer

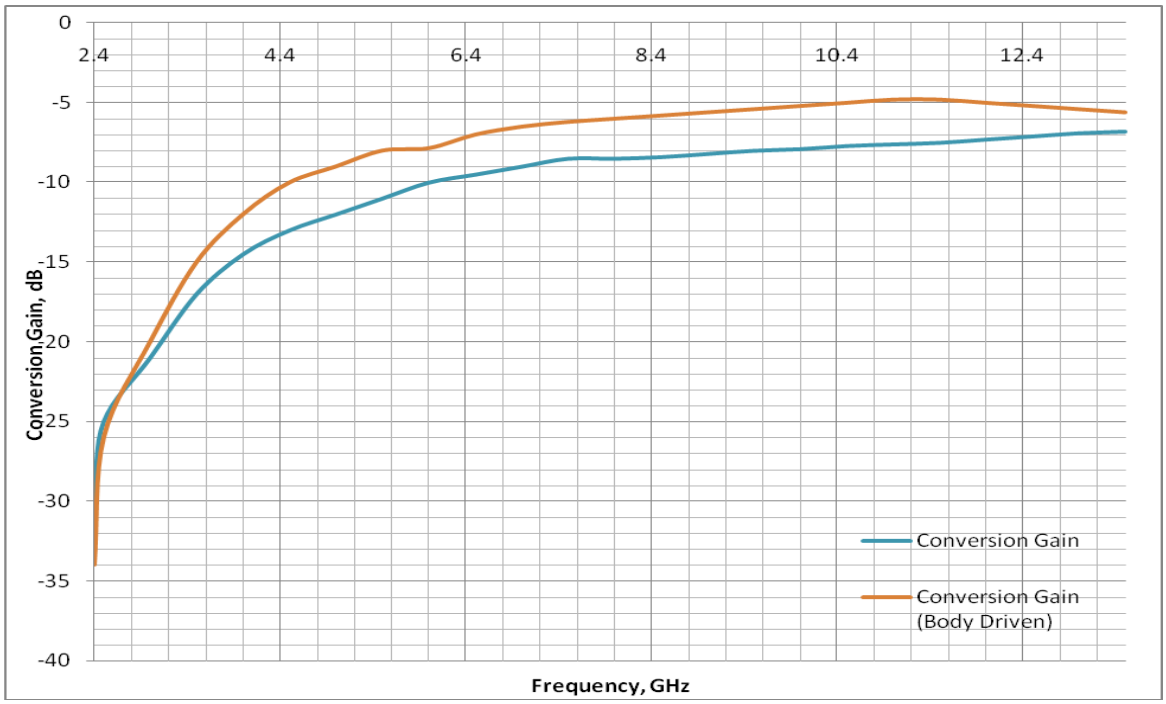


Figure 37: Gain comparison of a body driven passive mixer to a regular passive mixer

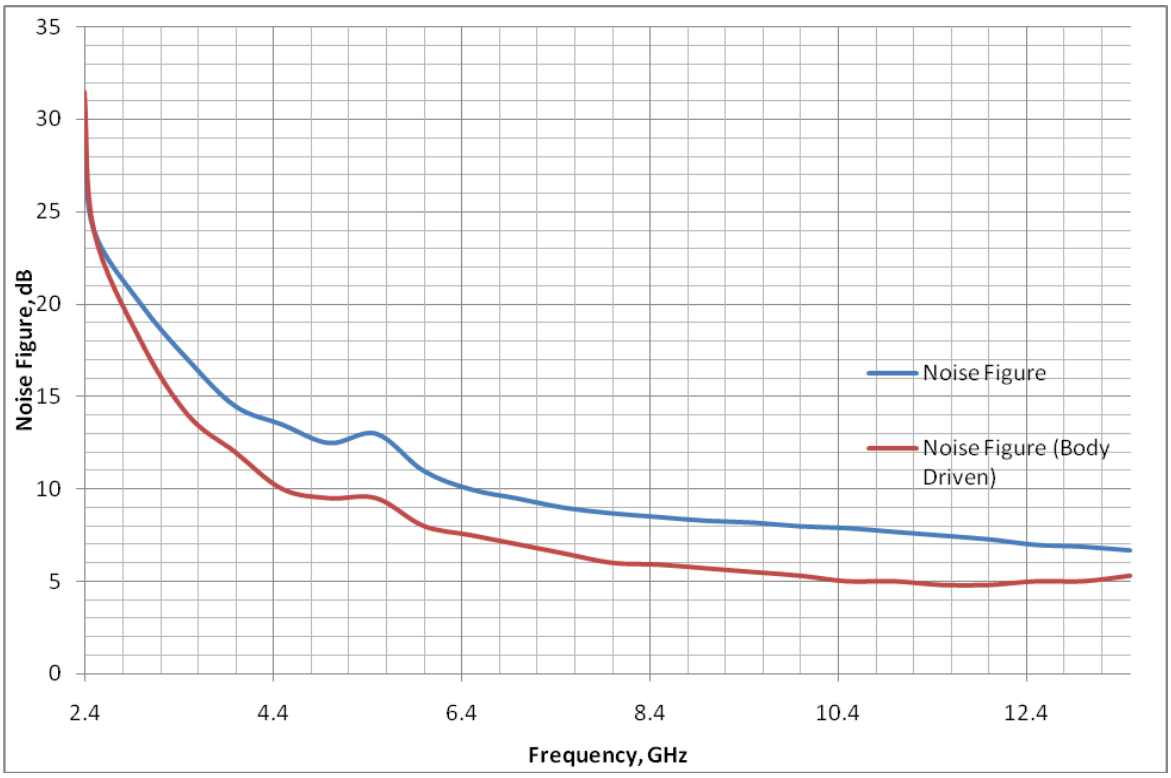


Figure 38: Noise figure comparison of a body driven passive mixer to a regular mixer

The above image displays the input, output matching, noise figure, and gain of system. There are two of each to show the difference between a regular passive mixer with forward body biased voltage and body driven mixer in which the RF port will go through the body of each transistor. It should be noted that the drain of the system is used as a floating node because there is no required current needed to go through the passive mixer.

S_{22} for the range of 4.5 GHz to 12 GHz is within the two dB of the –10 dB range therefore this system is still within the specification range. So I can say the output matching is comparable and still compatible for the system. This value of – 8 dB is better than what any of the other published papers could reach for the output matching

of a passive mixer. S_{11} met the specification of the matching and was able to maintain a value less than -10 dB the entire frequency range.

The noise figure is greatly reduced by converting the mixer to a body driven system. The gain of the mixer reaches its maximum during the range of operation which gets closer to zero than any of the other published papers.

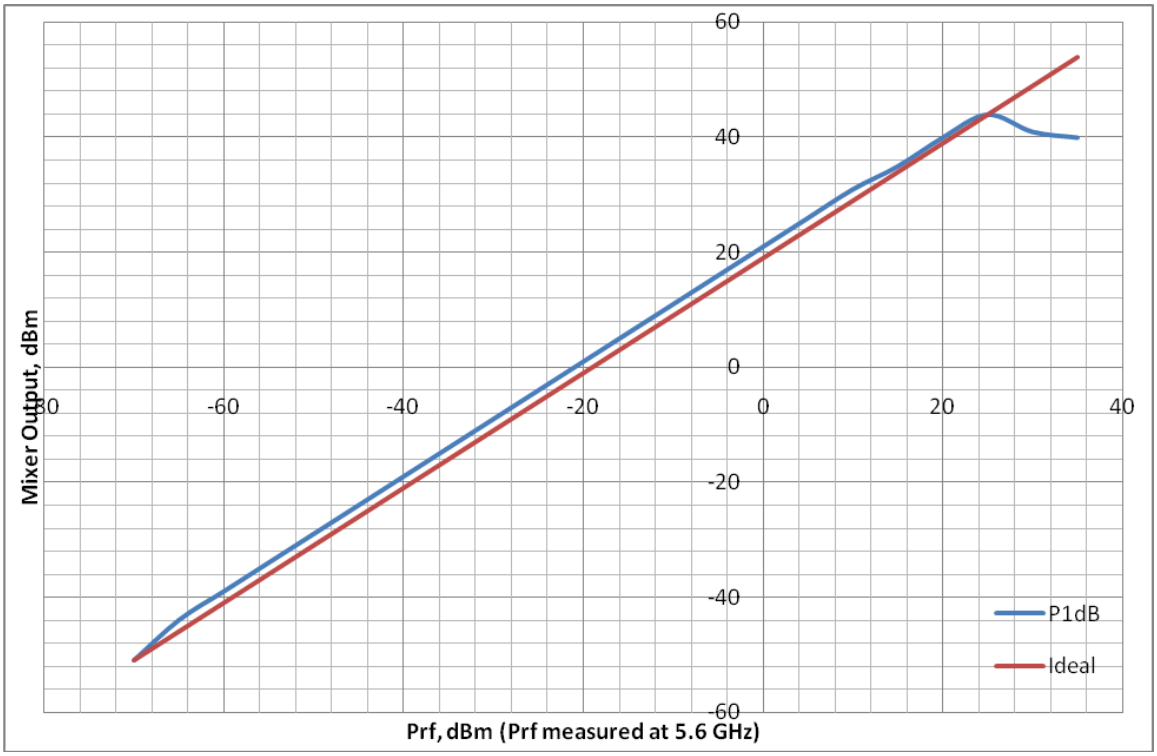


Figure 39: P_{1dB} compression point

Once again I generated multiple graphs of the P_{1dB} compression point to check the values at different frequencies within the operating range. I chose to include the 5.6 GHz here to show it achieves better results than the published papers described in the above table for the P_{1dB} specification. The gain calculated from the P1dB is same to which is calculated at 5.6 GHz in figure 37.

Once my design was better than previously published papers discussed in table 3 it was time to move onto the layout of the mixer. The layout was developed to achieve the smallest amount of parasitics by keeping the length of wires short. Also the layout was developed to meet all specifications designed in the schematic and simulation results. The mixer was tested in the design rule check (DRC) and layout versus schematic (LVS) verification to make sure it can pass all processing rules to therefore allow for actual implementation onto a chip. The chip size of the wideband body enabled passive mixer is 1217 μm x 961 μm. The chip has to be large due to the fact that the terminals had to be signal ground signal and could not share grounding terminals.

Then once the mixer was laid out to be put on a chip and was DRC and LVS clean, it was then re-simulated with all parasitics. The following is the chip layout and the simulation of the mixer again with parasitics.

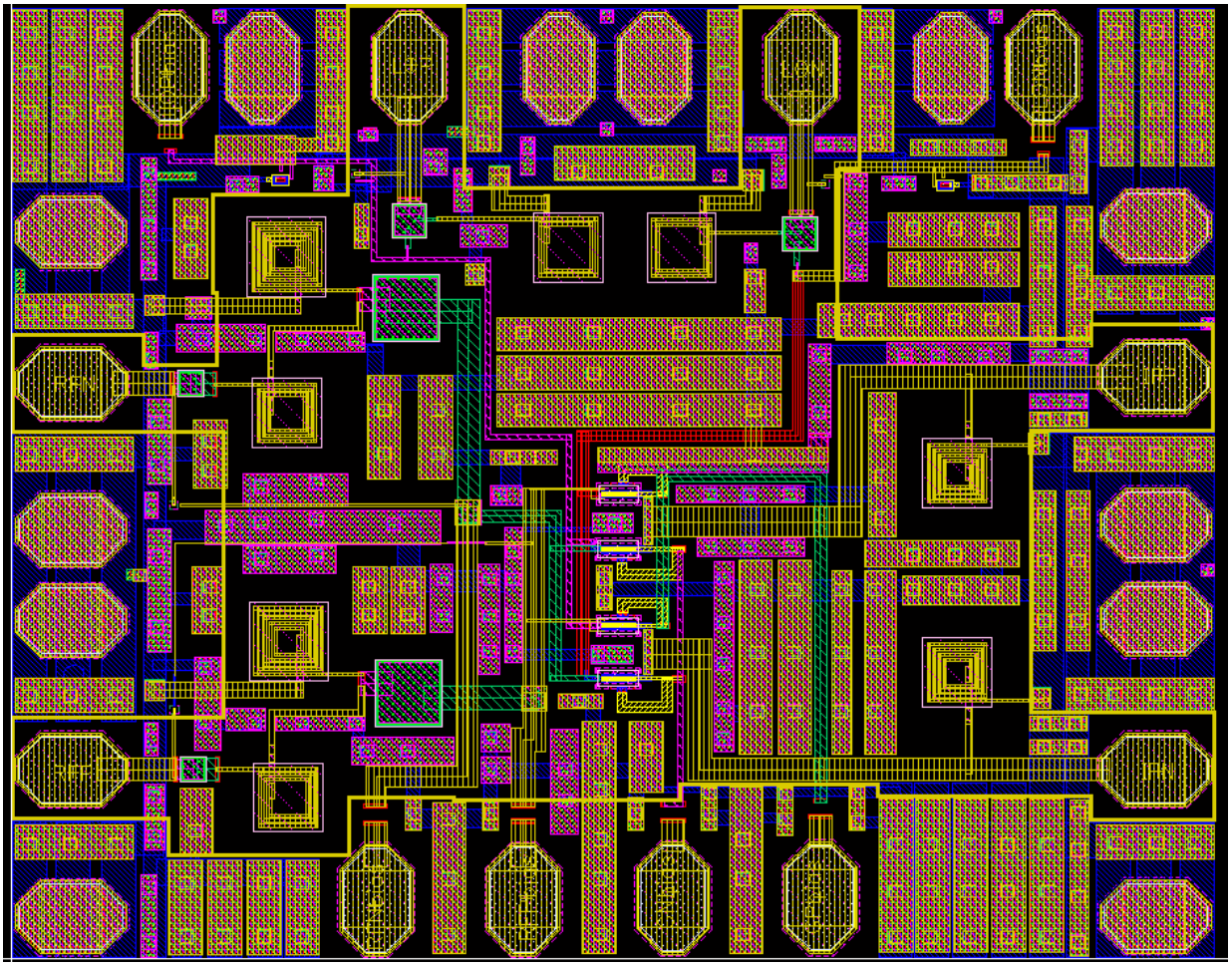


Figure 40: Layout of passive mixer (1217 μm x 961 μm)

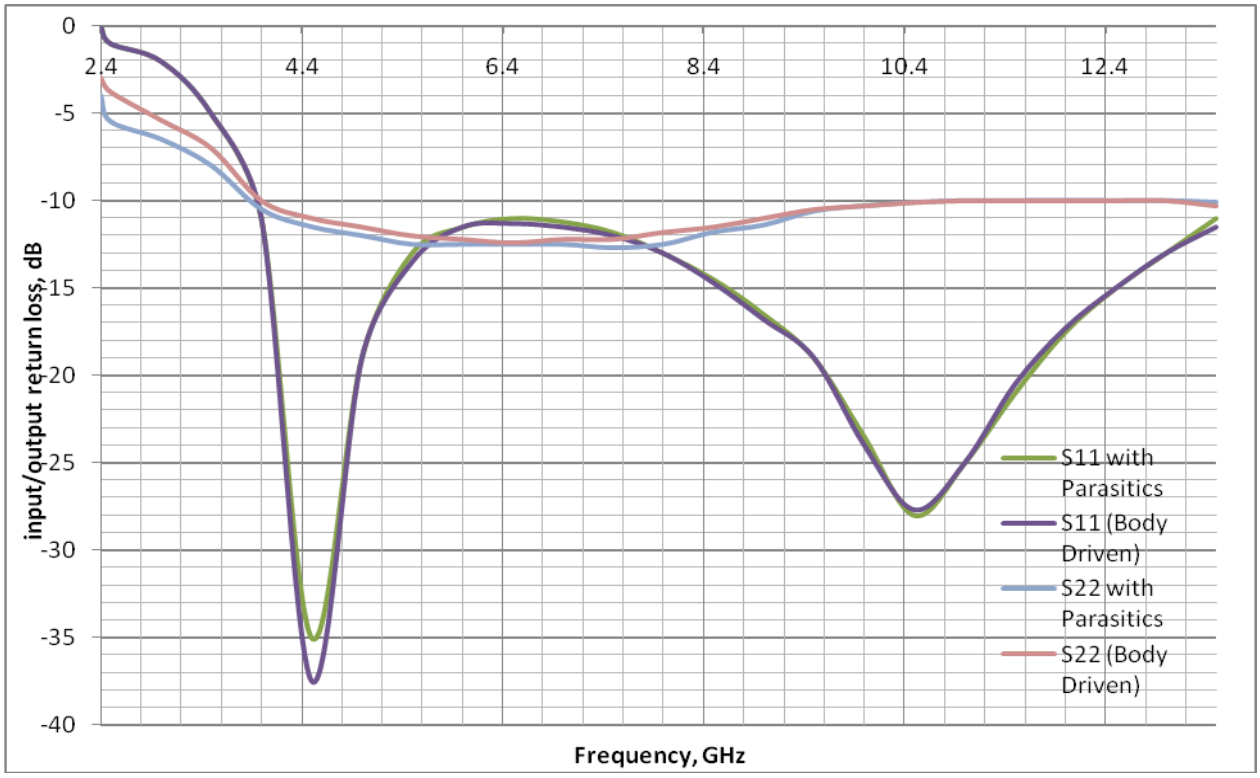


Figure 41: Input and output matching of body driven passive mixer along with parasitics

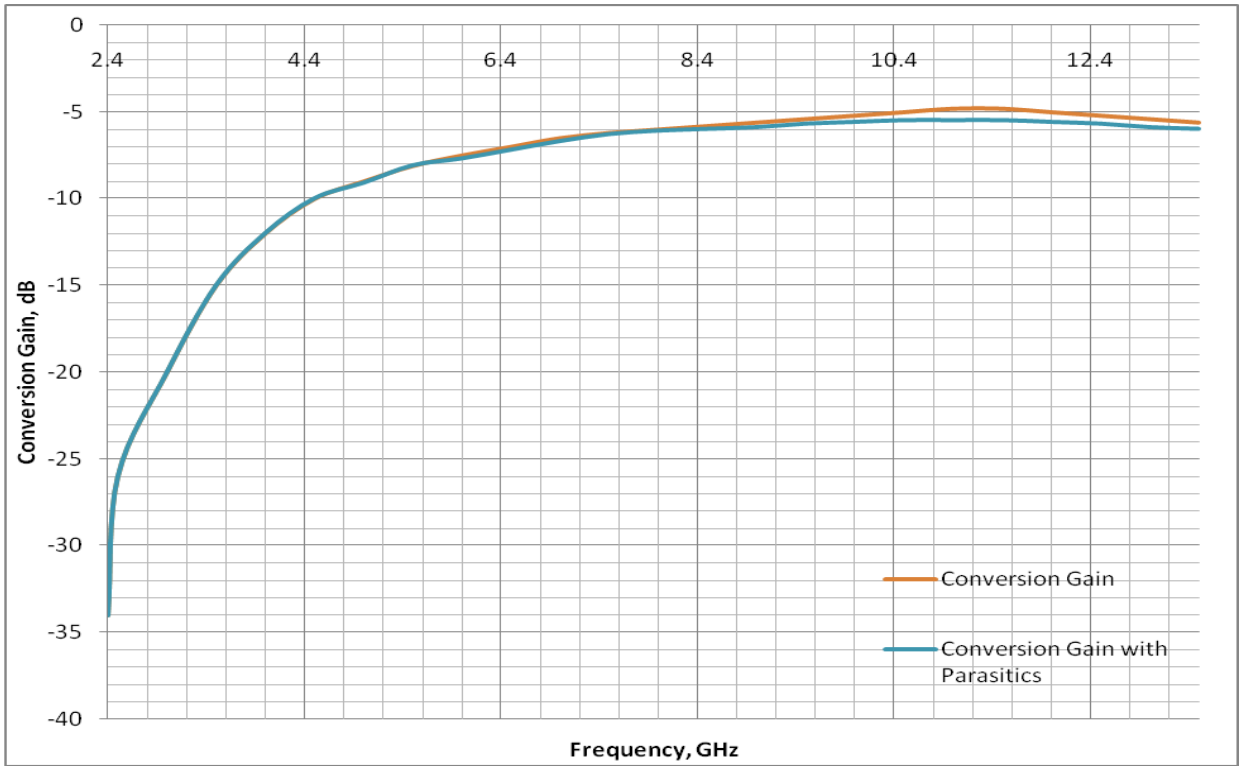


Figure 42: Gain of body driven passive mixer along with parasitics

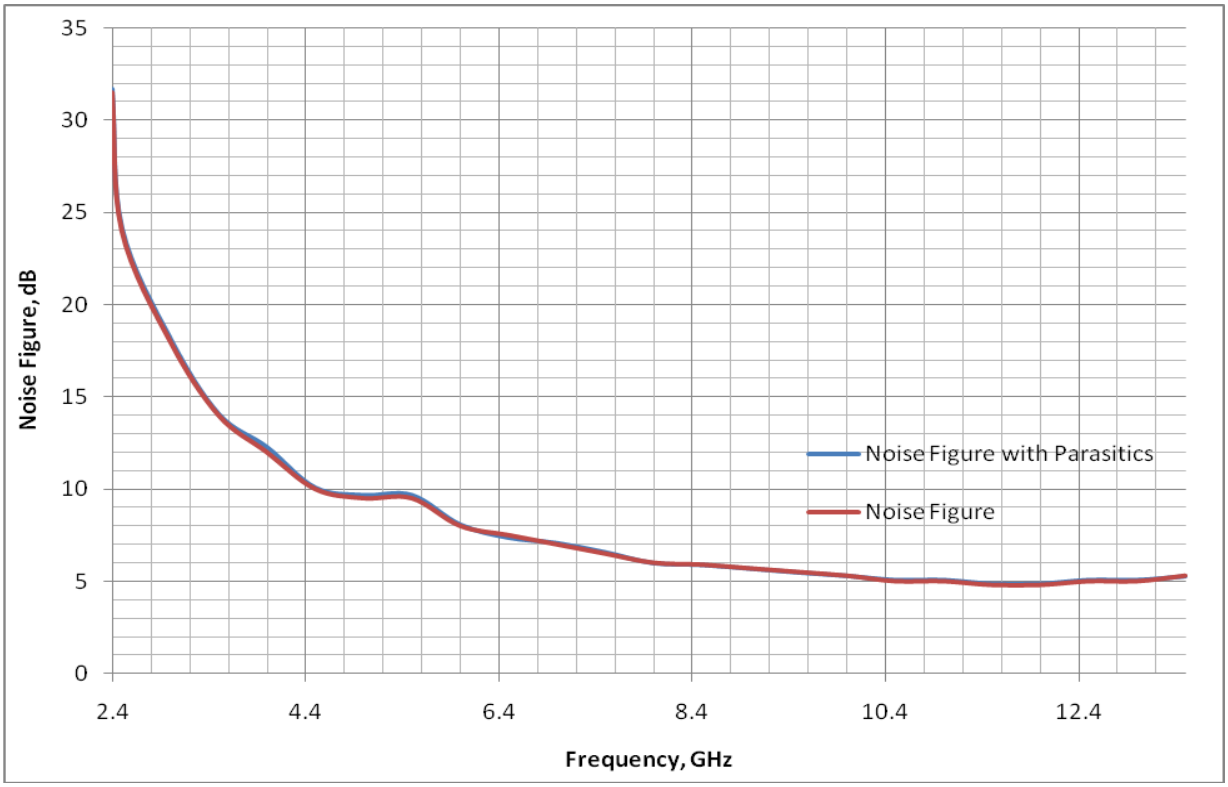


Figure 43: Noise figure of a body driven passive mixer along with parasitics

The above simulation results shows that gain (S_{21}) decrease the gain by about .27 dB from the original value. Input and output matching made the peaks more negative which is good. The parasitic had very little affect on the noise figure.

Temperature simulations show the ability to maintain the results over a wide range of temperatures. The average range for chip testing is -30 degrees Celsius to 50 degrees Celsius. The nominal testing for all previous simulations was 27 degrees Celsius. The following is the temperature variations for the input/output return loss, gain, and noise figure.

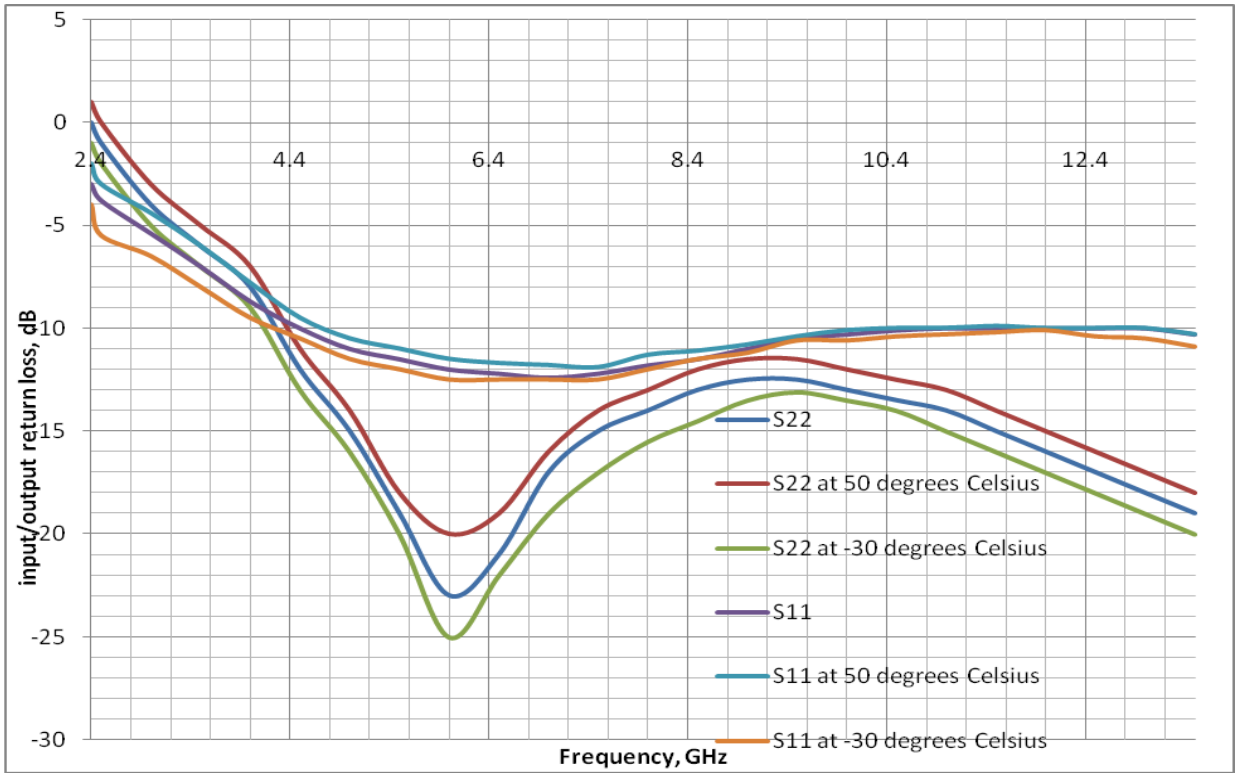


Figure 44: Temperature variation for S_{11} and S_{22} of the mixer

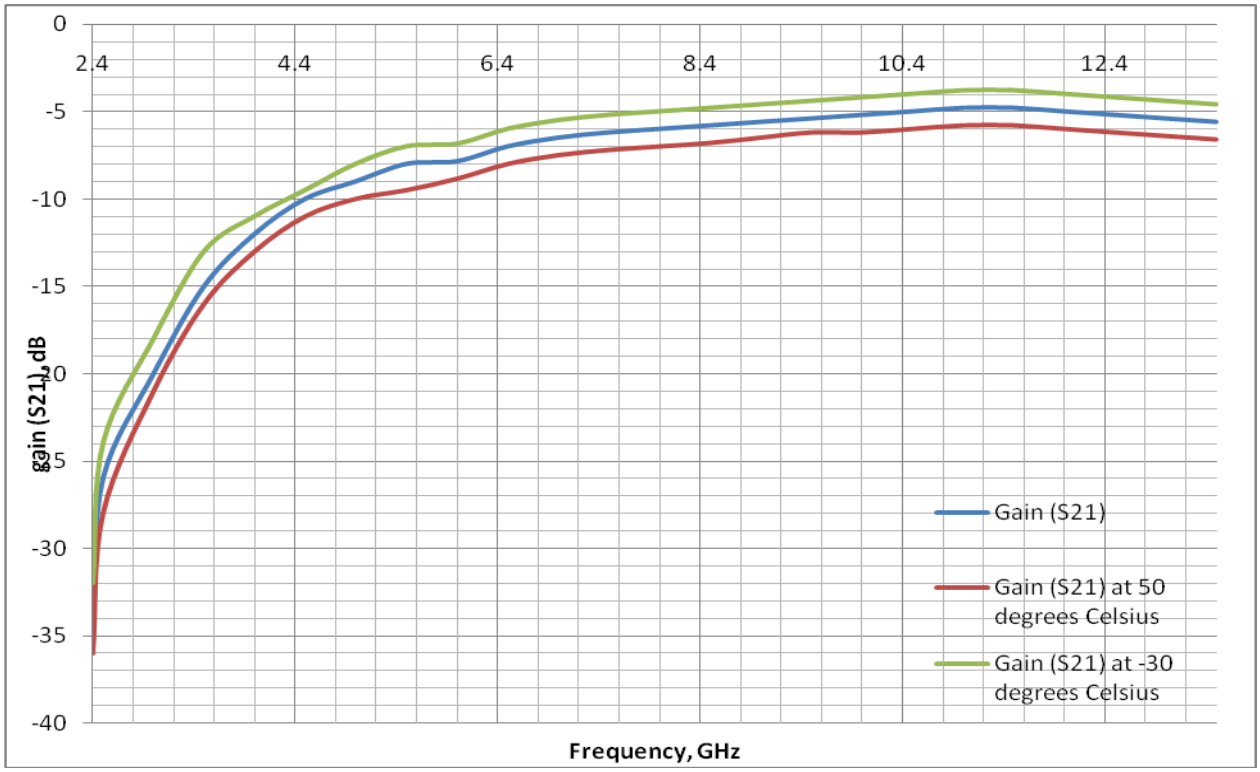


Figure 45: Temperature variation for gain of the mixer

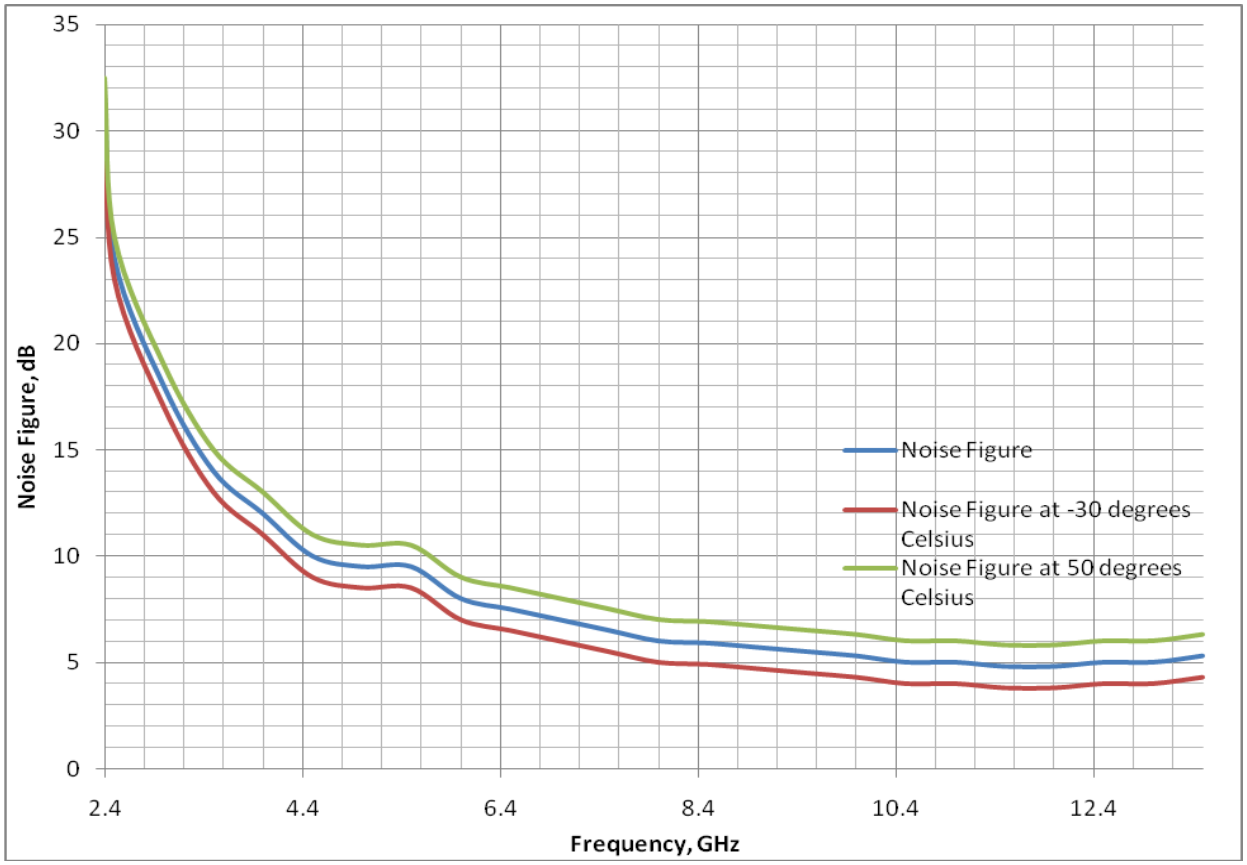


Figure 46: Temperature variation for noise of the mixer

Advantages

The advantages of using the body driven passive mixer are that the voltage supply will be decreased while still being able to maintaining specifications of the passive mixer. The port to port isolation is also increased due to the fact that triple well technology adds isolation. The triple well technology of the transistor is separates the substrate from the substrate of the entire chip. The ability to drive the RF signal through the body of the transistor will allow for all the specifications to be increased without sacrificing any other changes than switching the terminal to the body. In fact, the mixer has the ability to reduce the voltage applied to the RF when it goes though the body rather than drain of each transistor of the mixer.

Table 4: FOM comparison to recently published papers

Reference	**FOM**
[15]	116.50
[14]	128.10
[17]	136.6
Passive Mixer	120.5
Body Enabled Passive Mixer	149.4

CHAPTER FOUR

FUTURE WORK

4.1 Next research step

The next step directly related to the LNA and mixer is to put the LNA and mixer produced on a chip. Then after chip is back from fabrication testing can commence. Once the testing is completed and the recorded data is accurate the information will be inserted into a chart and submitted to IEEE for publication which will be accomplished by early 2010.

Further research in this area would be to develop a fully integrated body enabled PLL structure to feed the LO port of the mixer. Then the development of a body enabled filter is the next step after the mixer. The goal of the body enabled filter is to attenuate the mixer's unwanted signals, specifically the odd harmonics. After this, the final step would be in integrate a body enabled ADC. This would make for a fully developed front end transceiver that is body enabled. Once a fully developed transceiver with body enabled technology is developed, it will consume a very low power compared to those that don't utilize body enabling technology. This will allow for the front end transceiver to achieve low power and therefore allow for less often battery replacement.

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