TRANSIENT ERROR RESILIENCE IN NETWORK-ON-CHIP COMMUNICATION FABRICS

By

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To the Faculty of Washington State University:

The members of the committee appointed to examine the thesis of AMLAN GANGULY find it satisfactory and recommend that it be accepted.

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Chair

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Abstract

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Network on chip (NoC) is emerging as a revolutionary methodology to integrate numerous Intellectual Property (IP) blocks in a single System-on-Chip (SoC). Only an extensively communication centric paradigm like NoC can ensure seamless integration of such a large number of cores. A major challenge that NoC design is expected to face is related to the intrinsic unreliability of the communication infrastructure under technology limitations. As the separation between the wires is reducing rapidly, any signal transition in a wire affects more than one neighbor. This phenomenon is commonly referred to as the crosstalk effect. Crosstalk is one of the sources of transient errors. Among other sources of transient noise, factors like electromagnetic interference, alpha particle hits, cosmic radiation, etc. can be enumerated. To protect the NoC architectures against all these varied sources of noise an embedded self-correcting design methodology and its corresponding circuit implementation in the NoC communication fabrics is proposed. This embedded intelligence will be achieved through simple joint crosstalk avoidance and error correction coding schemes. In this work many existing crosstalk avoidance coding schemes and joint crosstalk avoidance and single error

correction coding schemes are implemented in a NoC interconnect architecture and are evaluated in terms of performance and gains in energy savings. Finally a novel joint crosstalk avoidance and double error correction scheme is developed. The performance of this novel code is compared with the other existing codes and is shown to deliver a higher savings in energy dissipation compared to the joint single error correction codes.

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Chapter 1

INTRODUCTION

1.1 System-on-Chip Design Issues

State-of-the-art commercial System-on-Chip (SoC) designs are integrating a large number of intellectual property (IP) blocks, commonly known as cores, on a single die [1] [2]. This number, which is currently between ten and hundred depending on the application, is likely to go up in the near future. An important feature of such Multi-Processor SoC's (MP-SoC) is the interconnect fabric, which must allow seamless integration of numerous cores performing various functionalities at different clock frequencies. The growing complexity of integration as well as aggressive technology scaling introduces multiple challenges for the design of such big multi-core SoC's.

One of the major problems associated with future SoC designs arises from non-scalable global wire delays [3]. Global wires carry signals across a chip, but these wires typically do not scale in length with technology scaling [4]. Though gate delays scale down with technology, global wire delays typically increase exponentially or, at best, linearly by inserting repeaters. Even after repeater insertion [4], the delay may exceed the limit of one clock cycle or even multiple clock cycles. In ultra-deep submicron processes, eighty percent or more of the delay of critical paths is due to interconnects. With supply voltage scaling down as ever and global wires becoming thinner the delay in transmission of signals over these wires will seriously affect the performance of the system. Long wires with lengths of the order of the dimensions of the die can have delays well over multiple clock cycles. This huge delay and the inherent complexity of integration of the IP cores necessitated new research to find a means of seamlessly integrating the multi-core SoC.

1.2 The Network-on-Chip Paradigm

The network on chip (NoC) paradigm has emerged as an enabling solution to this problem of integration and has captured the attention of the academia and the industry [2]. The common characteristic of these NoC architectures is that the processor/storage cores communicate with each other through intelligent switches. Communication between constituent IP blocks in a NoC takes place through packet switching. Generally wormhole switching is adopted for NoC's, which breaks down a packet into fixed length flow control units or *flits.* The first flit or the *header* contains routing information that helps to establish a path from the source to destination, which is subsequently followed by all the other *payload* flits. By design the lengths of the interconnects between the switches are kept within such limits as would enable communication in less than a clock cycle which maintains a pipelined structure in the entire communication fabric. Thus, delay on wires is bounded by an upper limit irrespective of the size of the network.

Some common NoC topologies used today are the Mesh, the Folded-Torus and the Butterfly Fat-Tree. The origin of these topologies can be traced back to literature on parallel computing. However, in addition to just throughput and latency constraints as in multiprocessing environments the designers of a NoC also need to consider energy consumption constraints.

1.3 Common NoC Topologies

There are a few NoC architectures proposed in literature. The characteristics of a few well-known NoC topologies are discussed below.

1.3.1 MESH

A Mesh based architecture called CLICHÉ (Chip Level Integration of Communicating Heterogeneous Elements) is proposed in [5]. This architecture consists of *mxn* mesh of intelligent switches interconnecting IP's placed along with each switch. Every switch except the ones on the

edge is connected to four neighboring switches and one IP block. In this case the number of IP's and the number of switches are equal. The Mesh topology is shown in Figure 1.1(a).

1.3.2 FOLDED-TORUS

A 2-D Torus was proposed in [6]. In this architecture the switches on the edges are connected to the switches on the opposite edge by wrap-around channels. However, in this case these wrap around channels tend to be very long and hence cause huge delays. As an alternative the Folded-Torus (FT) architecture shown in Figure 1.1(b) is suggested that folding the 2-D Torus structure so that all the wire lengths become same. Thus the long wrap-around wires are avoided in the Folded-Torus architecture.

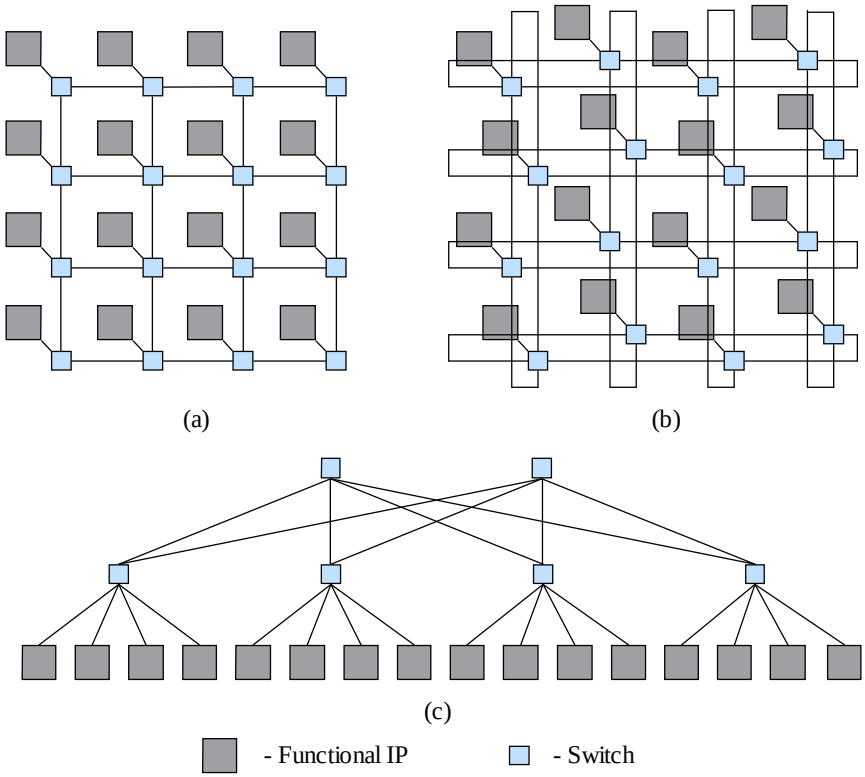


Figure 1.1: NoC architectures: (a) Mesh, (b) Folded-Torus (FT) and (c) Butterfly Fat Tree (BFT).

1.3.3 Butterfly-Fat-Tree

The Butterfly-Fat-Tree (BFT) proposed in [7] is shown in Figure 1.1(c). In this architecture the IP's are placed on the leaves and the switches are placed at the internal nodes. If there are *N* IP's then the IP's are connected to *N/4* switches in the first level. The total number of levels depends on the number of IP's. If there are *N* IP's then the total number of levels is given by ($log_4 N$). In the j^{th} level of the tree there are $N/2^{j+1}$ switches. For a 64-IP NoC, there are 28 switches according to the BFT architecture.

1.3 Signal Integrity in Future Technology Nodes

The *International Technology Roadmap for Semiconductors* (ITRS) [8] has predicted signal integrity to be a major challenge in current and future technology generations. Transient errors are becoming increasingly important due to increase in crosstalk, ground bounce and timing violations. These transient events are made more and more probable due to several reasons. With increased device density, the layout dimensions are shrinking and hence the charge used for storing the information bits in memory as well as logic, is reducing in magnitude [9]. Shrinking storage charges also make the chips vulnerable to radiations like alpha particle hits. Increasing gate counts force designers to lower the supply voltages to keep power dissipation reasonable thus reducing noise margins. Highly packed wires increases coupling between adjacent wires and opposing transitions induce crosstalk generated faults on these lines. Faster switching rates cause ground bounce and timing violations which manifest as transient errors. There are several ways to address signal integrity issues in an on chip environment like minimization of radiation exposure, careful layout, use of new materials and error control coding schemes. Error control coding enables us to address the transient sources of errors at a higher level of abstraction in the system design phase rather than at a post design, layout phase. Error Control Coding (ECC) is

possible to be implemented in NoC scenario because of the adoption of packet switching protocols in the communication, which allows an easy modification of the packet structure to accommodate redundant bits as a part of the coding schemes. However, for an on chip environment we need, simple and low redundancy coding schemes that will not impose a limiting overhead due to the encoding and decoding complexity.

1.4 Crosstalk Avoidance Coding

Crosstalk is one of the prime causes of the transient random errors in the inter-switch wire segments causing timing violations. Crosstalk occurs when adjacent wires transition (0 to 1 or 1 to 0) in opposite directions or even when adjacent wires have different slew rates although they are transitioning in the same direction. These two situations are shown in Figure 1.2(a) and (b). Opposite transition in the neighboring wires has the effect of slowing down the transition in the victim wire as shown in the figures.

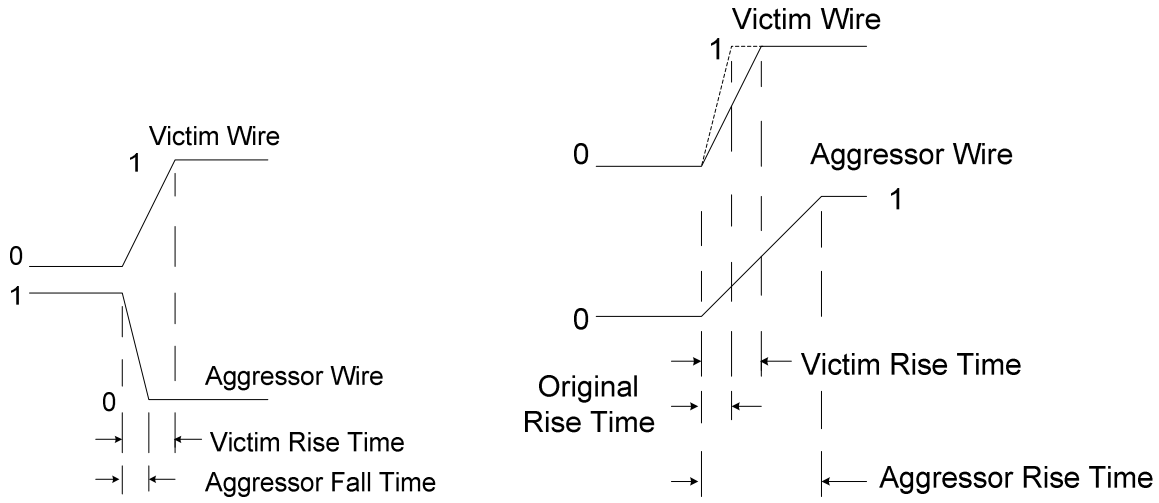


Figure 1.2: Crosstalk between adjacent wires for (a) opposite transitions and (b) similar transitions

The worst case crosstalk occurs when two aggressors on either side of the victim wire transition in opposite direction to the victim as shown in Figure 1.3.

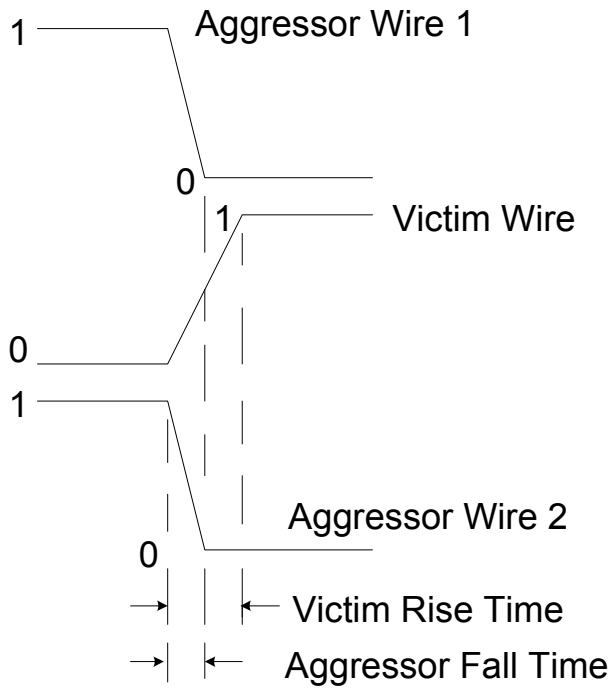


Figure 1.3: Worst case Crosstalk when two adjacent wires transition in opposite directions compared to the victim

Such a pattern of opposite transitions always increases the delay of each transition by increasing the mutual switching capacitance between the wires. In addition it also causes extra energy dissipation due to the increase in switching capacitance. Some common crosstalk avoidance techniques are increasing the distance between adjacent wires in the layout stage to reduce the coupling capacitance between the adjacent wires. However, this causes doubling the wire layout area [10]. For global wires in the higher metal layers that do not scale as fast as the device geometries, this doubling of area is hard to justify. Another simple technique can be shielding the individual wires with a grounded wire in between them. Although this is effective in reducing crosstalk to the same extent as increased spacing, this also necessitates the same overhead in terms of wire routing requirements. By incorporating coding mechanisms to avoid crosstalk the same reduction in crosstalk can be achieved at a lower overhead of routing area [6]. These coding schemes broadly termed as the class of Crosstalk Avoiding Codes (CAC) prevent

worst case crosstalk between adjacent wires by preventing opposite transitions in neighbors. Thus CAC's enhance system reliability by reducing the probabilities of crosstalk induced soft errors and also reduce the energy dissipation in UDSM busses and global wires by reducing the coupling capacitance between adjacent wires. Thus CAC's by reducing crosstalk eliminate one of the major sources of transient errors in NoC design in the nanometer technologies.

1.5 Error Control Coding

There are several other sources of transient errors apart from crosstalk as discussed earlier like electromagnetic interference, alpha particle hits and cosmic radiation which can alter the behavior of NoC fabrics and degrade signal integrity. Providing resilience against such failures is critical for the operation of NoC-based chips. Once again these transient errors can be addressed by incorporating error control coding to provide higher levels of reliability in the NoC communication fabric [11] [12]. The corrective intelligence can be incorporated into the NoC data stream by adding error control codes to decrease vulnerability to transient errors. Forward Error Correction (FEC) or error detection followed by retransmission based mechanisms or a hybrid combination of both can be used to protect against transient errors. The single error correction codes (SEC) are the simplest to implement among the FEC's. These can be implemented using Hamming codes for single error correction. Parity check codes and cyclic redundancy codes also provide error resilience by forward error correction. Error Detection codes can be used to detect any uncorrectable error patter and used to send an Automatic Repeat Request (ARQ) for retransmission of the data thus reducing the possibilities of dropped information packets. Higher order ECC's like Bose-Chaudhuri-Hocquenquem (BCH), Golay codes or Multiple Error Correcting Hamming codes can be used for multiple error corrections on the fly. However, these schemes are generally very complex and are not suited to an on-chip low

latency-high throughput environment.

One class of codes that have achieved considerable attention in the recent past is the joint coding schemes that attempt to minimize crosstalk while also perform forward error correction. These are called Joint Crosstalk Avoidance and Error Correction Codes (CAC/SEC) [13]. A few of these joint codes have been proposed in the literature for on-chip busses. These codes can be adopted in the NoC domain too. These include Duplicate Add Parity (DAP)[13], Boundary Shift Code (BSC) [14] or Modified Duplicate Add Parity (MDR) [15]. These are joint crosstalk avoiding single error correcting codes. These coding schemes achieve the dual function of reducing crosstalk and also increase the resilience against multiple sources of transient errors. But aggressive supply-voltage scaling and increase in deep sub-micron noise in future-generation NoCs will prevent Joint CAC/SEC's from satisfying reliability requirements. Hence, we investigate performance of joint CAC and multiple error correcting codes (MEC) in NoC fabrics. The main contributions of this work are the design of an original and novel but simple joint CAC/MEC mechanism, and the establishment of a performance benchmark for this scheme with respect to other existing coding methods. We also evaluate the novel scheme in terms of its applicability in the NoC domain and its impact on enhancement of communication reliability as well as energy dissipation, taking into consideration all the redundancies it introduces in the Network-on-Chip.

1.6 Contributions

The principal contribution of this thesis can be summarized as below:

- Implementation of several Crosstalk Avoidance Codes on the interconnect infrastructure of some commonly used NoC topologies. Evaluation of all the different codes in terms of the different metrics of energy dissipation, timing requirements and silicon area overhead.

- Comparison and evaluation of joint crosstalk avoidance and single error correction codes in the NoC environment. The implementation was done with encoder and decoder design for optimum results.
- Design of a novel joint crosstalk avoidance and double error correction code (CADEC) which has higher transient error resilience as well as similar crosstalk avoidance characteristics as the best sole crosstalk avoidance codes.

To the best of my knowledge this is the first attempt to invent a joint, crosstalk avoidance and multiple error correction code and study its applicability to NoC interconnect architectures.

1.7 Thesis Organization

The thesis is organized in six chapters. The 1st chapter introduces the complexity of the problem and the possible means of addressing those issues. Literature survey is presented in the 2nd chapter. The 3rd chapter explores the performance of various crosstalk avoidance codes in NoC communication fabrics. The fourth chapter characterizes the joint crosstalk avoidance and single error correction codes in a similar manner considering all the various important costs and trade-offs. In this chapter it is also demonstrated that joint codes typically perform better than sole crosstalk avoidance codes. In chapter five, the new code for the joint crosstalk avoidance and double error correction is introduced. The new mechanism is analyzed in sufficient depth to reach a fair comparison with all the other coding schemes considered in this thesis. It is shown that not only does the novel code achieve higher transient error resilience but it also results in higher energy savings on NoC interconnects among all the other schemes. Finally the last chapter summarizes the important conclusions and points out the direction of future research.

Chapter 2

Related Work

In recent years, there has been an evolving effort in developing on-chip networks to integrate increasingly large number of functional cores in a single die [1] [2]. But even before the advent of the NoC paradigm, different research groups investigated various coding schemes to enhance the reliability of bus-based systems. In [16] the authors proposed to employ data encoding to eliminate crosstalk delay within a bus. They presented a detailed analysis of the self-shielding codes and established fundamental theoretical limits on the performance of codes with and without memory. They succeeded in showing that codes with memory will require less routing overhead in the top-level interconnects where metal resources are scarce. However, the trade-off of using higher latency memory elements versus more wiring area needs to be studied. The authors however, have not clearly mentioned this trade-off in their work. In [15], the authors provided a comprehensive study of the usefulness of error correcting codes to reduce the crosstalk-induced bus delay (CIBD), and proved that Dual Rail codes perform better than Hamming codes. They have also proposed a way to layout the wires in the bus so that they achieve an optimal performance for the coding scheme suggested. The authors of [15] used single error correcting codes (SEC's) to minimize crosstalk. However, these codes are not as efficient as CAC's to handle only crosstalk related issues.

In addition, different low-power coding (LPC) techniques have been proposed to reduce power consumption of on-chip buses [17] but these LPC's aim at reducing only the self-transition in a wire. According to [18], the principal limitation of the applicability of the LPC's is that, due to higher power dissipation in the codec blocks, these codes are energy efficient only if the length of the wire segment exceeds a certain limit so that the savings along the wires can

supersede the expenses in the codecs. Since the self-transition determining codecs can be quite complex this constraint can limit the useful applicability of LPC schemes to only very long wires. In [13] the authors presented a unified framework for applying coding for systems on chips (SoC's), but targeted principally bus-based systems. In this work the authors suggest mechanisms for coding in UDSM busses to address multiple constraints of power dissipation, error correction and crosstalk avoidance. The authors successfully demonstrate that separate, sequential implementation of these different coding schemes to the bit stream is less efficient than coding schemes which address all the issues together in a unified manner. They compare various such codes like Duplicate-Add-Parity and Boundary-Shift-Code which are shown to be very efficient in a bus-based interconnect.

In [Hedge/Shanbhag 19] the authors model the transient noise in the busses as a white Gaussian pulse process and show that the bit error rate on a wire is related to the voltage swing on the wire. Exploiting this relation they are able to suggest that a reduction in the voltage swing on the wire is possible if the bit error rate is reduced due to increased resilience to transient errors.

In [11] [12], performance of single error correcting and multiple error detecting Hamming codes and cyclic codes in an AMBA bus-based system has been discussed. The energy efficiency and the area overhead of the codecs have been discussed too. These papers conclude that error detection followed by retransmission is more energy efficient than the forward error correction (FEC) schemes. However, one implicit assumption made in the papers is that the timing penalty associated with retransmissions is tolerable which may not be entirely true. In NoC environments latency and throughput issues are so compelling that retransmission might seriously hinder the overall system performance These works lack a comprehensive studies of

these trade-offs.

Error resiliency in NoC fabrics and the trade-offs involved in various error recovery schemes are discussed in [20]. In this work, the authors investigated performances of simple error detection codes like parity or cyclic redundancy check codes and single error-correcting, multiple error-detecting Hamming codes in NoC fabrics. The basic principle of this work is similar to that of [12]: the receiver corrects only a single bit error in a flow-control-unit (flit), but for more than one error, it requests end-to-end retransmission from the sender. The authors have also investigated various levels of trade-offs by comparing end-to-end retransmission with switch-to-switch retransmission to suggest a wide spectrum of choices to the user of such schemes. As mentioned in the concluding remarks of [12], in the ultra deep submicron (UDSM) domain communication energy will overcome computation energy. Retransmission will give rise to multiple communications over the same link and hence ultimately will not be very energy efficient. Moreover retransmission will introduce significant communication latency. In systems dominated by retransmission some additional error correction mechanisms for the control signals need to be incorporated also. Moreover, these codes do not have any crosstalk avoidance characteristics, which are absolutely necessary in the deep submicron (DSM) technology nodes. The role of communication infrastructure of NoC's on energy dissipation is discussed in [21]. Different strategies for power management for NoC's, following more classical VLSI techniques such as power-aware on-off networks [22], and dynamic voltage scaling [23] have been addressed previously.

Chapter 3

Crosstalk Avoidance Coding

In this chapter several Crosstalk Avoidance Codes (CAC) are implemented and compared in the NoC interconnect fabric. These CAC's reduce the switching capacitance between adjacent wires which are closely packed. In the following subsections the characteristics of CAC's are first described and then they are evaluated in terms of energy savings, timing and area requirements.

3.1 Crosstalk Avoidance Coding Schemes

There is a number of crosstalk avoidance codes [16] proposed in literature. Here we consider three representatives that achieve different degrees of coupling capacitance reduction.

3.1.1 Forbidden Overlap Condition (FOC) Codes

A wire has the worst-case switching capacitance of $(1+4\lambda)C_L$, when it executes a rising (falling) transition and its neighbors execute falling (rising) transitions. If these worst-case transitions are avoided, the maximum coupling can be reduced to $(1+3\lambda)C_L$. This condition can be satisfied if and only if a codeword having the bit pattern 010 does not make a transition to a codeword having the pattern 101 at the same bit positions. The codes that satisfy the above condition are referred to as Forbidden Overlap Condition (FOC) Codes. The simplest method of satisfying the forbidden overlap condition is half-shielding, in which a grounded wire is inserted after every two signal wires. Though simple, this method has the disadvantage of requiring a significant number of extra wires. Another solution is to encode the data links such that the codewords satisfy the forbidden overlap (FO) condition. However, encoding all the bits at once is not feasible for wide links due to prohibitive size and complexity of the codec hardware. In

practice, partial coding is adopted, in which the links are divided into sub-channels which are encoded using FOC. The sub-channels are then combined in such a way as to avoid crosstalk occurrence at their boundaries. Considering a 4-bit sub-channel the FOC coding scheme is represented in Table 3.1.

Table 3.1. FOC_{4-5} Coding Scheme

Data bits				Coded bits				
d_3	d_2	d_1	d_0	c_4	c_3	c_2	c_1	c_0
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	0	0	1
0	0	1	1	0	0	1	0	1
0	1	0	0	0	0	0	1	1
0	1	0	1	0	0	1	1	1
0	1	1	0	1	0	0	1	1
0	1	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0	0
1	0	0	1	1	0	1	0	0
1	0	1	0	1	0	0	0	1
1	0	1	1	1	0	1	0	1
1	1	0	0	1	1	0	0	0
1	1	0	1	1	1	1	0	0
1	1	1	0	1	1	0	0	1
1	1	1	1	1	1	1	0	1

In this case two sub-channels can be placed next to each other without any shielding, as well as not violating the FO condition as shown in Figure 3.1.

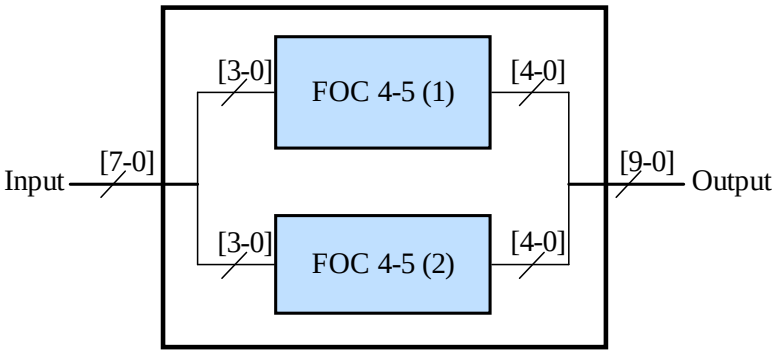


Figure 3.1: Block diagram of combining adjacent sub channels in FOC coding

The Boolean expressions relating the original input (d_3 to d_0) and coded bits (c_4 to c_0) for the FOC scheme are expressed as follows:

$$c_0 = d_1 + d_2\overline{d_3}$$
$$c_1 = d_2\overline{d_3}$$
$$c_2 = d_0$$
$$c_3 = d_2 d_3$$
$$c_4 = d_1 d_2 + d_3$$

3.1.2 Forbidden Transition Condition (FTC) codes

The maximum capacitive coupling and, hence, the maximum delay, can be reduced even further by extending the list of non-permissible transitions. By ensuring that the transitions between two successive codes do not cause adjacent wires to switch in opposite directions (i.e., if a codeword has a 01 bit pattern, the subsequent codeword cannot have a 10 pattern at the same bit position, and vice versa), the coupling factor can be reduced to *p*=2. This condition is referred to as Forbidden Transition Condition, and the CAC's satisfying it are known as Forbidden Transition Condition (FTC) Codes. Inserting a shielding wire after each signal line can employ the simplest FTC, but causes unreasonable overhead in redundant wires. For wider inter-switch

links, a hierarchical encoding is more suitable, where the inter-switch links are divided into sub-channels that are encoded individually. Considering a 3-bit sub-channel the coding scheme is expressed in Table 3.2.

For wider message words the entire flit can be subdivided into multiple sub channels, each having a three-bit width, and then the individual coded sub-words recombined following the scheme shown in Figure 3.2. This scheme of recombination simply places a shielded wire between each sub-channel. This ensures no forbidden transitions even at the boundaries of the sub-channels.

Table 3.2: FTC_{3-4} coding scheme

Data bits			Coded bits			
d_2	d_1	d_0	c_3	c_2	c_1	c_0
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	0	1
0	1	1	0	1	0	1
1	0	0	0	1	1	1
1	0	1	1	1	0	0
1	1	0	1	1	0	1
1	1	1	1	1	1	1

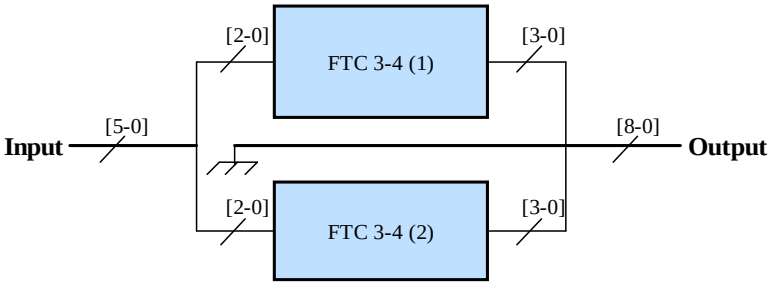


Figure 3.2: Block diagram of combining adjacent sub channels in FTC coding

The Boolean expressions relating the original input and coded bits for the FTC scheme are

expressed as follows:

$$c_0 = d_1 + d_2\overline{d_0}$$
$$c_1 = d_0 d_1 d_2 + \overline{d_0}\,\overline{d_1} d_2$$
$$c_2 = d_0 + d_2$$
$$c_3 = d_0 d_2 + d_1 d_2$$

3.1.3 Forbidden Pattern Condition (FPC) Codes

The same reduction of the coupling factor as for FTC's (p=2) can be achieved by avoiding 010 and 101 bit patterns for each of the code words. This condition is referred to as Forbidden Pattern Condition, and the corresponding CAC is known as Forbidden Pattern Condition (FPC) Codes. Considering a 4-bit sub-channel, the coding scheme is expressed in Table 3.3.

Table 3.3: $FPC_{4\text{-}5}$ coding scheme

Data bits				Coded bits				
d_3	d_2	d_1	d_0	c_4	c_3	c_2	c_1	c_0
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	1	1	0
0	0	1	1	0	0	0	1	1
0	1	0	0	0	1	1	0	0
0	1	0	1	0	0	1	1	1
0	1	1	0	0	1	1	1	0
0	1	1	1	0	1	1	1	1
1	0	0	0	1	0	0	0	0
1	0	0	1	1	0	0	0	1
1	0	1	0	1	1	0	0	0
1	0	1	1	1	0	0	1	1
1	1	0	0	1	1	1	0	0
1	1	0	1	1	1	0	0	1
1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	1	1

While combining the sub-channels we made sure that there is no forbidden pattern at the boundaries.

Figure 3.3 depicts the scheme of avoiding forbidden pattern at the boundaries, considering four-bit sub-channels. The MSB of a sub channel is fed to the LSB of the adjacent one. This method is more efficient than simply placing shielding wires between the encoded sub-channels and consequently results in lesser redundancy overhead.

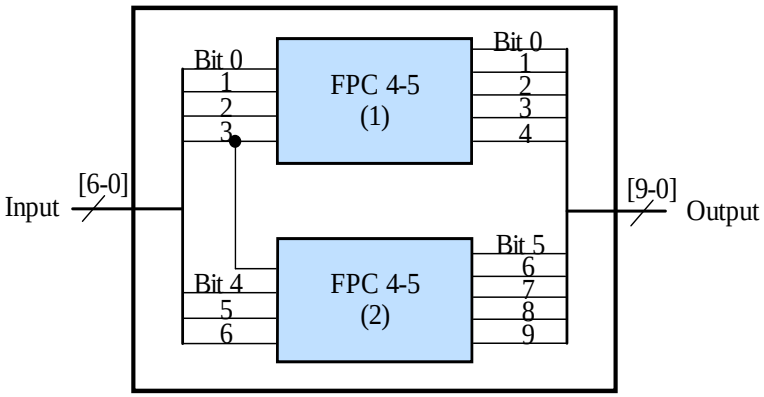


Figure 3.3: Block diagram of combining adjacent sub channels after FPC coding.

The Boolean expressions relating the original input (d_3 to d_0) and coded bits (c_4 to c_0) for the FPC scheme are expressed as follows:

$$c_0 = d_0$$
$$c_1 = d_0 d_1 + d_2 d_1 + d_1 \overline{d_3} + d_0 d_2 \overline{d_3}$$
$$c_2 = d_2 \overline{d_3} + d_1 d_2 + \overline{d_0} d_2 + d_1 \overline{d_0}\,\overline{d_3}$$
$$c_3 = d_2 d_3 + \overline{d_0} d_2 + d_2 d_1 + d_1 d_3 \overline{d_0}$$
$$c_4 = d_3$$

3.2 Data Coding in NoC Links

The coupling capacitance of an inter-switch wire segment in a NoC link depends on the

transitions in the adjacent wires. As shown in [23] the worst case switching capacitance of a wire segment is given by $(1+4\lambda)C_L$, where λ is the ratio of the coupling capacitance to the bulk capacitance and C_L is the load capacitance, including the self capacitance of the wire. By incorporating CAC's it is possible to reduce this switching capacitance to $(1+p\lambda)C_L$, where p=1, 2, or 3 and it is referred to as the maximum coupling. Thus the worst case energy dissipation of a single wire segment in a NoC link is reduced from $(1+4\lambda)V_{dd}{}^2C_L$ to $(1+p\lambda)V_{dd}{}^2C_L$, indicating a linear increase in energy savings in presence of CAC with the decrease in coupling capacitance.

The generic communication medium of any NoC fabric is shown in Figure 3.4. Between a source and destination pair there is a path consisting of multiple switch blocks [15]. Consequently, when data routing is performed, the flits need to be coded and decoded at each intermediate switch node. These operations will have a significant effect on overall energy dissipation.

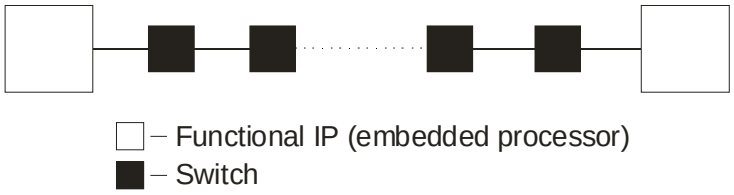


Figure 3.4: Generic Data Transfer in NoC Fabrics

Typical wormhole header and payload packets are shown in Figure 3.5. The header contains all the routing information which establishes a path from the source to the destination. The payload flits simply follow the header through this established path in a pipelined fashion.

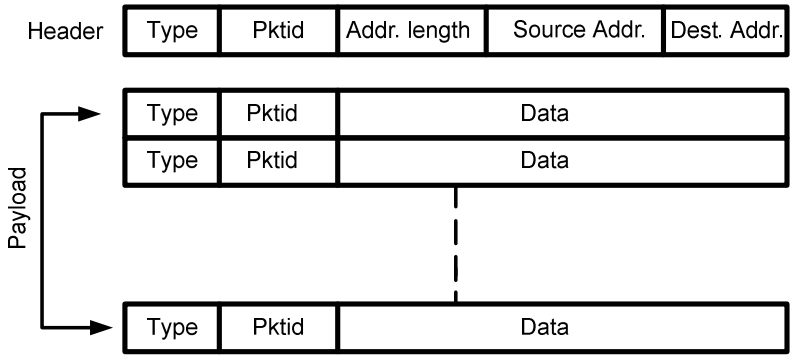


Figure 3.5: Flit Structure

While comparing the energy dissipation characteristics upon implementing the various CAC schemes on the flits, the redundant wires added as a result of the codes should be considered, as well as the overhead due to the codec blocks in addition to the reduction in energy on the interconnects due to crosstalk reduction.

3.3 Energy savings profile in presence of CAC

When flits travel on the interconnection network, both the inter-switch wires and the logic gates in the switches toggle, resulting in energy dissipation. The flits from the source nodes need to traverse multiple hops consisting of switches and wires to reach destinations.

The motivation behind incorporating CAC in the NoC fabric is to reduce switching capacitance of the inter-switch wires and hence make communication among different blocks more energy efficient. So, the metric of interest is the average savings in energy per flit with coding compared to the uncoded case. All the schemes have different number of bits in the encoded flit. A fair comparison in terms of energy savings demands that the redundant wires be also taken into account while comparing the energy dissipation profiles. The metric used in this work for comparison thus takes into account the savings in energy due to the reduced crosstalk, additional energy dissipated in the extra redundant wires and the codecs. The savings in energy

per flit per hop is given by,

$$E_{savings,j} = E_{link,uncoded} - (E_{link,coded} + E_{codec}) \qquad (3.1)$$

where $E_{link,\ uncoded}$ and $E_{link,coded}$ are the energy dissipated by the uncoded flit and the coded flit in each inter-switch link respectively. E_{codec} is the energy dissipated by each codec. The energy savings in transporting a single flit, say the i^{th} flit, through h_i hops can be calculated as

$$E_{savings,i} = \sum_{j=1}^{h_i} E_{savings,j} . \qquad (3.2)$$

The average energy savings per flit in transporting a packet consisting of P such flits through h_i hops for each flit will be given as,

$$\overline{E}_{savings} = \frac{\sum_{i=1}^{P} \sum_{j=1}^{h_i} (E_{savings\ ,j})}{P} . \qquad (3.3)$$

The metric $\overline{E}_{savings}$ is independent of the specific switch implementation, which may vary based on the design.

In order to quantify the energy savings profile for a NoC interconnect architecture, we determine the energy dissipated in each codec, E_{codec} by running Synopsys™ Prime Power on the gate-level netlist of the codec blocks. To determine the inter-switch link energy in presence and absence of coding, that is, $E_{link,coded}$ and $E_{link,uncoded}$ respectively, the capacitance of each interconnect stage, $C_{interconnect}$ is calculated taking into account the specific layout of each topology and it can be estimated according to the following expression

$$C_{interconnect} = C_{wire} \cdot w_{a+1,a} + n \cdot m \cdot (C_G + C_J) \qquad (3.4)$$

where C_{wire} is the wire capacitance per unit length, and $w_{a+1,a}$ is the wire length between two consecutive switches; C_G and C_J are the gate and junction capacitance of a minimum size

inverter, respectively, *n* denotes the number of inverters (when buffer insertion is needed) in a particular inter-switch wire segment and *m* is their corresponding size with respect to a minimum size inverter. While calculating C_{wire} without any coding we have considered the worst case switching scenario, where the two adjacent wires switch in the opposite direction of the signal line simultaneously [24]. The parameter $w_{a+1,a}$ can be calculated depending on the network architecture used. For Mesh architecture the inter-switch wire length is given by

$$w_{a+1,a} = \frac{\sqrt{Area}}{\sqrt{N} - 1}. \qquad (3.5)$$

Where *Area* is the area of the silicon die used and *N* is the number of individual IP blocks in the SoC. The inter-switch wire length for Folded-Torus architecture is twice that of the Mesh as it connects every alternate IP block in the network. The same inter-switch wire length for the BFT architecture between levels a+1 and a is given by Equation 3.6, where *levels* is the total number of levels needed for implementing the BFT architecture given by $\text{Log}_4 N$.

$$w_{a+1,a} = \frac{\sqrt{Area}}{2^{levels-a}} \qquad (3.6)$$

In the presence of CAC's the value of C_{wire} will be reduced according to the coding scheme and this will help in reducing the link energy. On the other hand the additional energy dissipated by the codecs and redundant wires added by the coding schemes need to be considered as well. Our aim is to study the effects of all these factors on the overall energy savings of NoC communication infrastructures.

3.4 Communication Pipelining in Presence of Coding

The exchange of data among the constituent blocks in a SoC is becoming an increasingly difficult task because of growing system size and non-scalable global wire delay. To cope with

these issues, designers must divide the end-to-end communication medium into multiple pipelined stages, with the delay in each stage comparable to the clock-cycle budget. In NoC architectures, the inter-switch wire segments, along with the switch blocks, constitute a highly pipelined communication medium characterized by link pipelining, deeply pipelined switches, and latency-insensitive component design [21] [25].

The switches generally consist of multiple pipelined stages. The number of intraswitch pipelined stages can vary with the design style and the features incorporated within the switch blocks. However, through careful circuit-level design and analysis, designers can make each intraswitch stage's delay less than the target clock period in a particular technology node. In one of the possible scenarios for the NoC architectures considered here, we have shown that the structured inter-switch wires and the processes underlying the switch operations require four types of pipelined stages [25] [26] [27] and the delays of each of these stages can be constrained within the clock period limits suggested by ITRS [8] for high performance multi-core SoC platforms. In accordance with ITRS, a generally accepted rule of thumb is that the clock cycle of high performance SoCs will saturate at a value in the range of 10-15 FO4 (Fan-out of 4) delay units. We need to ensure that by adding the codec blocks, the constraints on timing can still be met. The codec blocks add additional stages to the switches. If the delay of these codecs can be constrained within the clock cycle limit then the pipelined communication infrastructure will be maintained.

3.5 Area Penalty

Two out of the three most important parameters for VLSI design namely energy, timing and area are discussed in the previous subsections. In this subsection the other important meteric of area overhead for implementing these CAC schemes is discussed. Area for a circuit on chip is

usuaklly expressed in terms of the number of 2-input NAND gates possible to lay-out in the same area as occupied by the circuit. Each IP in a state-of-the-art big SoC today containes about a million transistors which is of the order of a hundred thousand gates, In coparison each switch of the NoC fabric maybe made of around 30K gates. Performance capabilities and complexity of the IP blocks are increasing rapidly and so is the area of such blocks. With progress in technology silicon area has almost become free now-a-days. However, in contrast to the huge area requirements of the cores and switches the coding and decoding blocks for the discussed codind schemes only take a few hundred gates for their implementation. So, incorporation of the coding schemes will not be affected if the area requirements do not have limiting contraints and are under a thousand gates.

3.6 Experimental Results and Analysis

To study the effects of the CAC schemes on the performance of different NoC infrastructures, we considered a system consisting of 64 IP blocks and mapped them onto the interconnect architectures, as shown in Figure 1.1. We characterize the NoC's in terms of three principal metrics: energy savings, area overhead and timing. Messages were injected with a uniform traffic pattern (in each cycle, all IP cores can generate messages with the same probability). The routing mechanism used for the MESH and Folded Torus architectures was the *e-cube* (dimension order) routing and for BFT was the Least Common Ancestor (LCA) determination [28]. Simulations were performed using 90nm technology node parameters. The codec blocks were synthesized with the CMP [29] standard cell libraries. The parameters used for the purpose of simulations are listed in Table 3.4.

Table 3.4: Simulation Parameters

Architecture	Message Length (Flits)	Buffer Depth (Flits)	Number of ports
MESH	16	2	5
FOLDED TORUS	16	2	5
BFT	16	2	6

3.6.1 Energy savings profile

The average energy dissipation profile for any NoC follows a saturating trend with injection load [24]. Consequently, the energy savings profile will maintain the same trend. The energy dissipation and hence savings in energy of each inter-switch wire segment is a function of λ, the ratio of the coupling capacitance to the bulk capacitance. For a given interconnect geometry, the value of λ depends on the metal coverage in upper and lower metal layers [12]. We investigate the energy savings profiles for comparison at the two representative values of λ =1 and 6 for the 90nm technology node [30].

Figures 3.6, 3.7 and 3.8 show the variation in energy savings per flit for MESH, Folded Torus and BFT-based NoC architectures respectively.

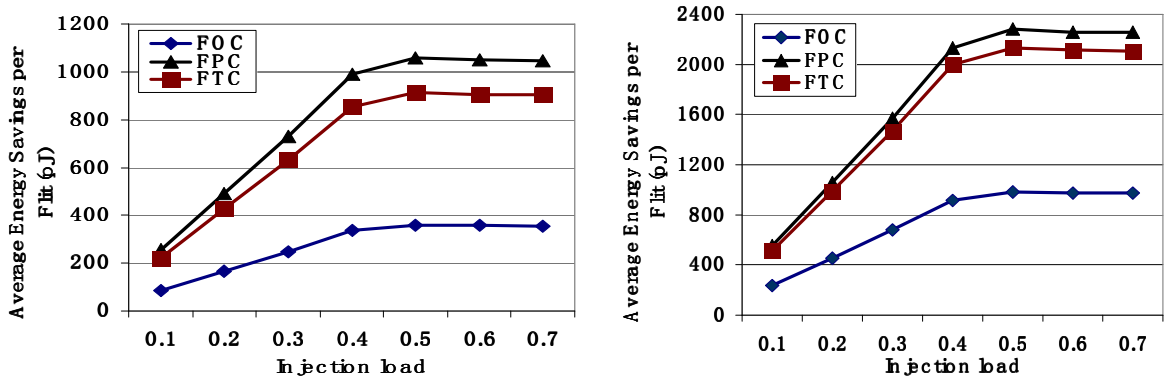


Figure 3.6: Energy savings profile for a Mesh based NoC at (a)λ=1 (b)λ=6.

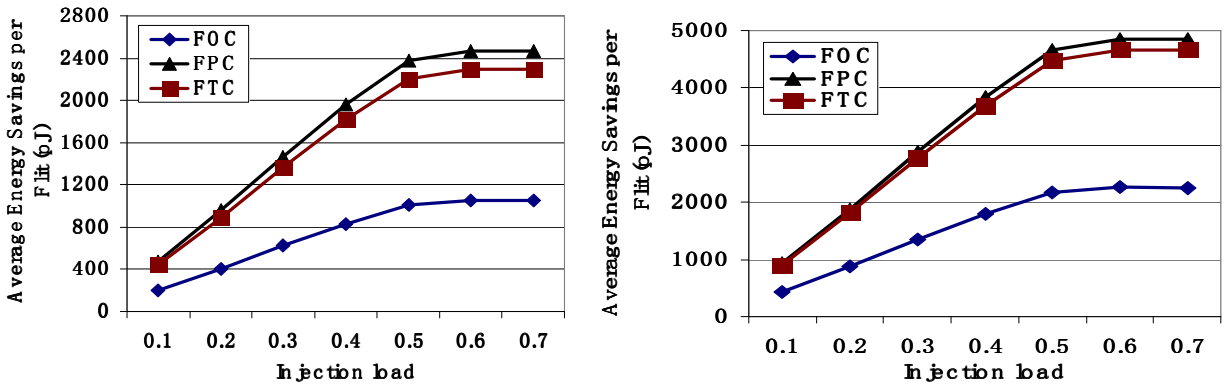


Figure 3.7: Energy savings profile for a Folded-Torus based NoC at (a)λ=1 (b)λ=6.

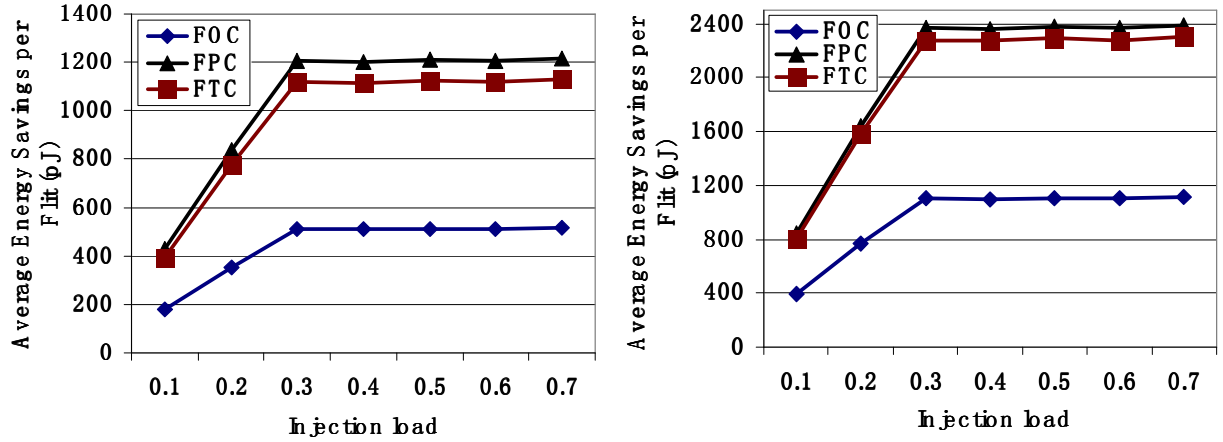


Figure 3.8: Energy savings profile for a Butterfly Fat Tree based NoC (a)λ=1 (b)λ=6.

As seen in Figures 3.6 to 3.8, maximum energy savings are obtained for the Folded-Torus architecture. This occurs due to the fact that Folded-Torus architecture has longer interconnect lengths compared to MESH. Although the upper level links in BFT are longer than those of Folded Torus, the overwhelming majority of the links span the lowest level and those are much shorter [26] [27]. Since the savings increase linearly with the length of the wires, the energy savings in Folded Torus architecture are most pronounced.

3.6.2 Area Overhead

While evaluating the performance of CAC schemes we need to consider the extra silicon area they add to the NoC switch blocks. Through RTL level design and synthesis in 90 nm technology node, we found that the switches, without any coding scheme consist of approximately 30K gates. Here, we consider a two-input minimum-sized NAND structure as a reference gate. In comparison to this the codecs for FOC, FPC and FTC have around 650, 1000 and 770 gates respectively. Consequently the extra area overhead added by the CAC schemes is relatively insignificant.

3.6.3 Timing Requirements

The switches generally consist of multiple pipelined stages. The number of intraswitch pipeline stages can vary with the design style and the features incorporated within the switch blocks. As shown in [27] in one of the possible implementations the switches may consist of three stages: (1) input arbitration, (2) routing and (3) output arbitration. It is already shown in [7] that each intraswitch stage's delay can be made less than this target clock period in a particular technology node. In presence of CAC there will be additional pipelined stages corresponding to encoder and decoder blocks, as shown in Figure 3.9.

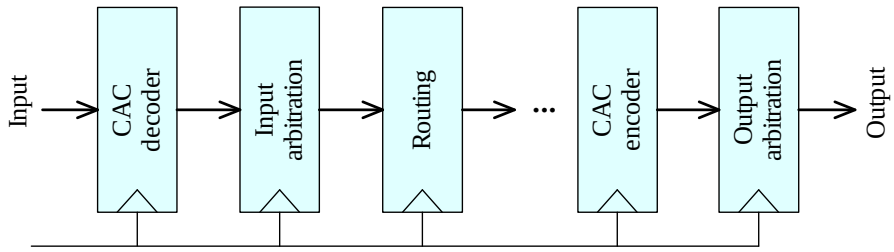


Figure 3.9: Pipelined intra-switch stages in presence of coding

Through RTL design and synthesis using Synopsys synthesis tools, we obtain the delays

along the critical paths of each encoder and decoder for all the coding schemes. The delay values corresponding to all the coding schemes are shown in Table 3.5. It is evident that all the coding schemes achieve the target delay values within the limit of one clock cycle. Consequently they will not affect the data introduction rate.

Table 3.5: Critical path delay of codec blocks

Scheme	Block	Delay (FO4)
FOC	Encoder	0.50
	Decoder	0.25
FPC	Encoder	4.25
	Decoder	3.75
FTC	Encoder	2.75
	Decoder	2.50

In addition to the intra-switch stages, we need to ensure that the delay along the inter-switch wire segments is also within the limit of one clock cycle. We have already demonstrated that the delay along the inter-switch wire segments for the NoC architectures under consideration in this work can be constrained within the limit of one clock cycle [26] [27]. Thus, for the coded system the delay will be even smaller as a result of reduction of switching capacitance in the wires which in turn reduces the delay.

3.7 Modification of the Flit Structure

If the packet structure can be modified in such a way that coding/decoding is needed only at the source and destination nodes, then there will be no extra power dissipation arising out of the codec blocks in the intermediate nodes [24] [31]. If the flit structure is modified so that only the header flits contain the control information, then the payload flits need not be coded/decoded at each intermediate switch node. Eventually, this will help reducing the overall communication

energy dissipation. Only the header flit will be encoded and decoded at each switch stage in the transmission path as shown in Figure 3.10 below.

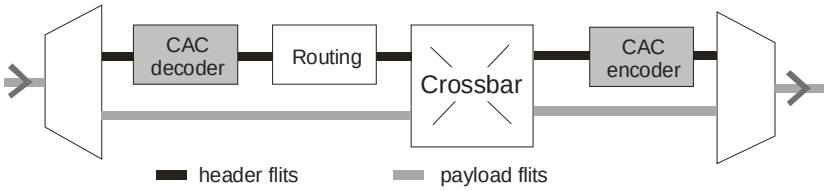


Figure 3.10: CAC coding/decoding for the Header Flits.

3.7.1 Modified Flit Structure

The modifications to the flit structure are made such that the coding and decoding needs to be done only to the header flit. The modified flit structure is shown in Figure 3.11.

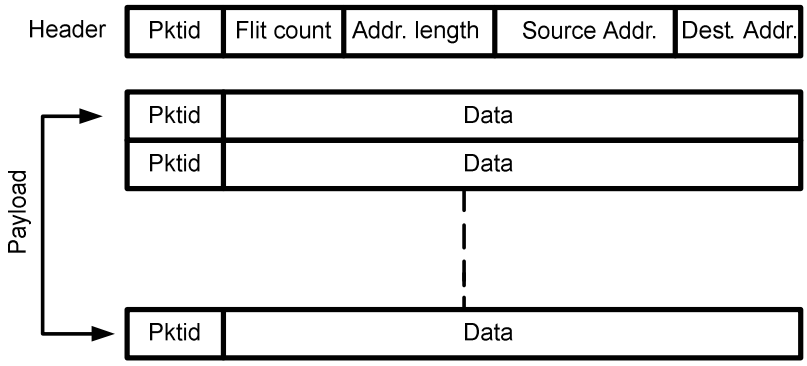


Figure 3.11: Modified Flit Structure

A new field called *flit count* is incorporated in the header flit, which keeps track of the number of payload flits in a packet. The *type* field in the payload flits becomes unnecessary as the switch knows the number of payload flits that follow a header from the *flit count* field in the header. The *pktid* field in the payload flits of Figure 3.10 links each flit to a particular packet. After decoding the header flit the switch knows the number of payload flits to expect from the *flit count* and then systematically routes all the payload flits bearing the same *pktid* along the path set by the header flit. This can be done without decoding the payload flits as CAC encoding

of the *pktid* produces unique identifiers which can be directly used to link the payload flits with a particular header. The switches only need a negligible modification to use the CAC encoded *pktid* bits instead of the original *pktid* for mapping each payload flit to its corresponding packet. The payload flits need not be decoded and encoded at each intermediate switch, thus reducing the codec overhead and making the incorporation of CAC schemes in a NoC communication fabric more energy efficient.

3.7.2 Energy Savings Profile with Modified flit structure

The energy savings can be considerably improved by modifying the flit structure as shown in Figure 3.3. As all the routing and control information is contained only in the header flit and the payload flits only follow the already established path, there is no need to code/decode the payload flits on the fly at every switch. Instead, it is sufficient to code the payload flits at the source and decode at the destination switch. Thus, the coding and decoding overhead is greatly reduced as this process is now done only at the source and destination switches once for all the payload flits. The header flit however, still undergoes coding and decoding at all the switches.

The codec energy will not be included for the body flits when the modified flit structure of Figure 3.10 is used. Thus, for payload flits Equation 3.1 will be modified as follows

$$E_{savings\ ,\ j} = E_{link\ ,uncoded} - E_{link\ ,coded} \qquad (3.7)$$

With this modified flit structure, the energy savings for λ=1 and λ=4 are plotted for a Mesh architecture in Figure 3.12, a Folded-Torus architecture in Figure 3.13 and for a BFT architecture in Figure 3.14.

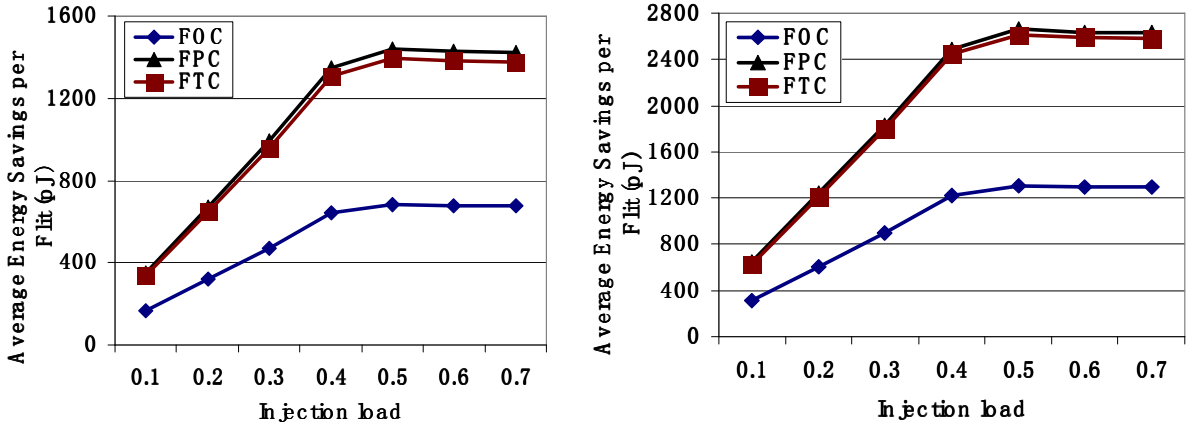


Figure 3.12: Energy savings profile for a Mesh based NoC at λ=1 with modified flit structure at (a)λ=1 (b)λ=6.

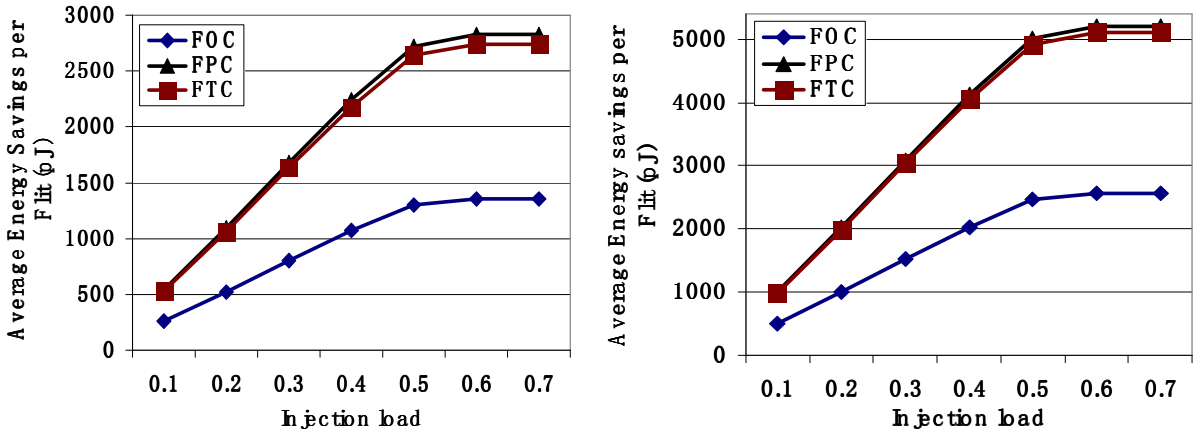


Figure 3.13: Energy savings profile for a Folded-Torus based NoC at λ=1 with modified flit structure at (a)λ=1 (b)λ=6.

It is observed that the energy savings are made more significant by adopting the modified flit structure with negligible increment in the complexity of the switch blocks. Another important point to note here is that the FOC scheme is the least energy efficient one. FTC and FPC have very similar energy savings profile and they are better than FOC. Table 3.6 quantifies the additional gain in energy savings at network saturation by adopting the modified flit structure for λ=6.

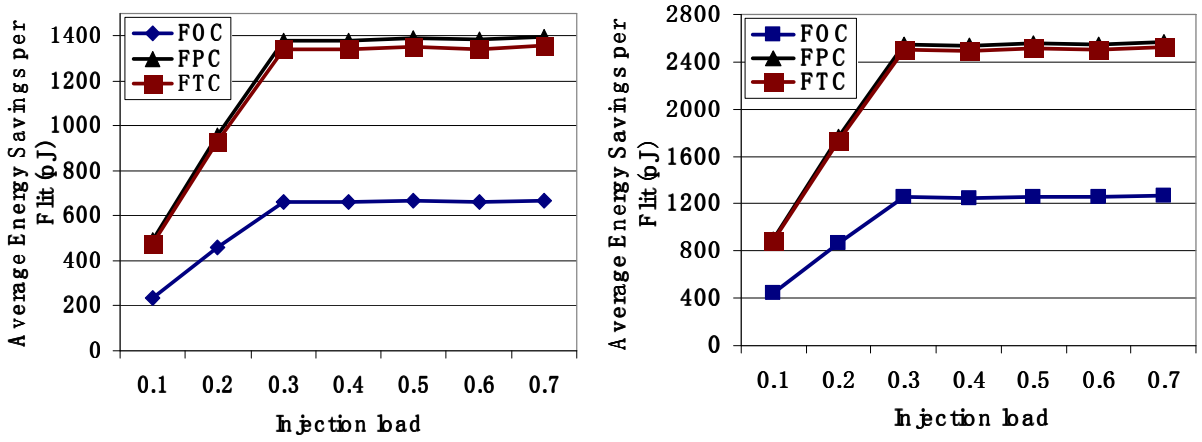


Figure 3.14: Energy savings profile for a Butterfly Fat Tree- based NoC at λ=1 with modified flit structure at (a) λ=1 (b)λ=6.

Table 3.6: Gain in energy savings with modified flit structure

Architecture	CAC scheme	Energy savings with original flit structure (pJ)	Energy savings with modified flit structure (pJ)	Gain in energy savings (%)
Mesh	FOC	982	1307	33.0
	FTC	2134	2614	22.5
	FPC	2282	2664	16.7
Folded-Torus	FOC	2264	2570	13.5
	FTC	4675	5128	9.6
	FPC	4858	5218	7.4
Butterfly Fat Tree	FOC	1108	1261	13.8
	FTC	2291	2517	9.8
	FPC	2382	2562	7.5

3.8 Conclusions

By incorporating Crosstalk Avoidance Codes (CACs) in NoC data stream it is possible to reduce the worst-case coupling capacitance of interswitch wire segments and consequently the energy dissipation in communication. The energy savings arising out of incorporating CACs depend on the distribution of inter-switch wires of different lengths and the packet structure. We

proposed a method of reducing the energy dissipation by eliminating the need for CAC coding/decoding of payload flits at intermediate switches between communicating NoC cores. It is observed that the energy savings is the maximum for Folded Torus architecture as it consists of uniformly distributed long inter-switch wire segments. It is shown how the method of modifying the packet structure and reducing the coding/decoding overhead makes it possible to achieve higher savings in energy in conjunction with crosstalk protection.

Chapter 4

Joint Crosstalk Avoidance and Single Error Correction Coding

The incorporation of Crosstalk Avoidance Codes (CAC's) reduces the mutual switching capacitance of the inter-switch wire segments. Though this helps in reducing the energy dissipation in communication, the reduction is only linear with the capacitance in nature. On the other hand, incorporation of the error correction codes make the system more robust, and consequently, the voltage level driving the system can be reduced without compromising bit error rates. This makes joint crosstalk-avoidance and error correction codes more suitable for lowering the energy dissipation of on-chip communication infrastructures as the energy dissipation on the wires is a quadratic function of the voltage swing. A few Joint Crosstalk Avoidance and Single Error Correction codes (CAC/SEC) were proposed in literature principally targeting traditional bus-based systems, among which Duplicate Add Parity [13], Boundary Shift Code [14], and Modified Dual Rail Code [15] provide single error correction in conjunction with crosstalk avoidance. All of these coding schemes reduce the crosstalk induced switching capacitance of wires from $(1+4\lambda)C_L$ to $(1+2\lambda)C_L$ [34] where, λ is the ratio of the coupling capacitance to the bulk capacitance and C_L is the load capacitance, including the self capacitance of the wire.

Below the characteristics of the joint crosstalk avoidance and single error correction coding schemes and their implementation principles are discussed in details.

4.1 Duplicate Add Parity and Modified Dual Rail Code

The ***Duplicate Add Parity (DAP)*** code is a joint coding scheme that uses duplication to reduce crosstalk [13]. Duplication results in reducing the crosstalk induced coupling capacitance

from the worst case switching capacitance of a wire segment from $(1+4\lambda)C_L$, to $(1+2\lambda)C_L$. Also, by duplication, we can achieve Hamming distance of two, and with the addition of a single parity bit, the Hamming distance [32] increases to three. Consequently, DAP has single error correction capability. The DAP encoder and decoder are shown in Figures 4.1(a) and (b) respectively. Encoding involves calculating the parity and duplicating the bits of the incoming word. Similarly, in decoding, the parity bit is recreated from one set of the data flit. As shown in Figure 4.1(b), bit y_8 is the previously-calculated parity, and the other signal entering the exclusive-or gate is the newly-calculated parity of the more significant set (bits y_1, y_3, y_5, and y_7). The new parity is compared with the original parity calculated in the encoder, and the error-free set is chosen. For example, in case of an error in the more significant set, the parities will differ, and the less significant set will be chosen as the decoded flit. On the other hand, if the error occurs in less significant set, the more significant set will be chosen. Thus, considering a link of k information bits, $m = k + 1$ check bits are added, leading to a code word length of $n = k + m = 2k + 1$.

We define the $k + 1$ check bits with the following equations:

$$c_i = d_i, for\ i = 0\ to\ k-1$$
$$c_k = d_0 \oplus d_1 \oplus ..... \oplus d_{k-1}$$

The ***Modified Dual Rail (MDR)*** code is very similar to the DAP [15]. In the MDR code, two copies of parity bit C_k are placed adjacent to the other codeword bits in order to reduce crosstalk.

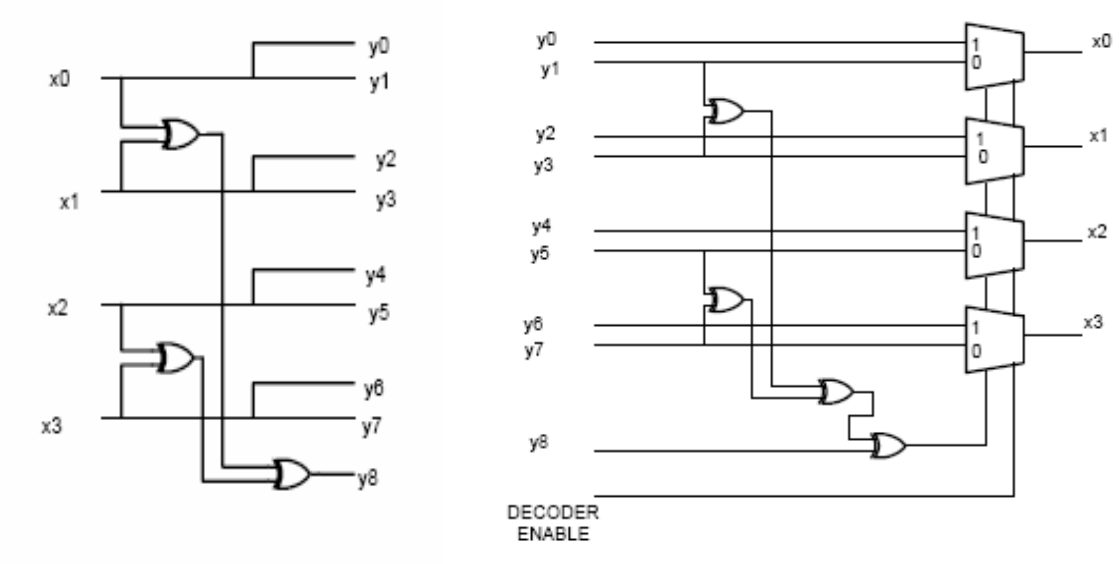


Figure 4.1: (a) Duplicate Add Parity (DAP) encoder (b) decoder

4.2 Boundary Shift Code

The ***Boundary Shift Code (BSC)*** coding scheme attempts to reduce crosstalk-induced delay by avoiding a shared boundary between successive codewords. As shown in [33] this techniques achieves a reduction in the worst case crosstalk induced switching capacitance from $(1+4\lambda)C_L$ to $(1+2\lambda)C_L$. It is very similar to DAP in that it uses duplication and one parity bit to achieve crosstalk avoidance and single-error correction. However, the fundamental difference is that at each clock cycle, the parity bit is placed on the opposite side of the encoded flit. In BSC, the dependent boundaries are the boundaries between encoded bits. Refer to Table 4.1, which shows examples of different code words with parity bits in bold. In clock cycle 1, dependent boundaries exist between bits y_0 and y_1, y_2 and y_3, y_4 and y_5, and y_6 and y_7. Inversely, in the second clock cycle, dependent boundaries are between bits y_1 and y_2, y_3 and y_4, y_5 and y_6, and y_7 and y_8. As can be seen in Table 4, this coding scheme does not allow dependent boundaries in subsequent codewords. Encoding is achieved by duplicating bits and completing a parity calculation as in DAP. However, every second clock cycle will result in a one-bit shift.

Similarly, the decoding structure is equivalent to that of DAP with the addition of a one-bit shift every other clock cycle before the parity check. Figures 4.2(a) and 4.2(b) depict the encoder and decoder respectively.

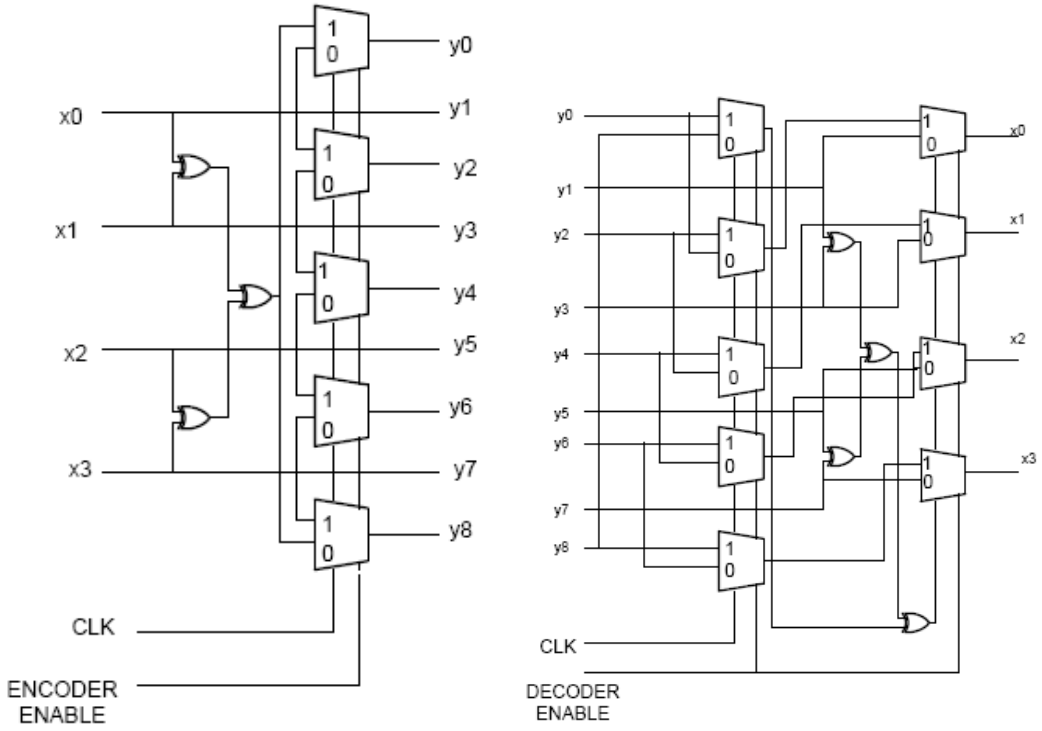


Figure 4.2: (a) BSC encoder, (b) decoder

Table 4.1
Coded flit structure for different coding schemes

Clock Cycle	Flit	BSC	DAP	MDR
1	0010	**1**00001100	**1**00001100	**11**00001100
2	0010	000011001	**1**00001100	**11**00001100
3	1100	**0**11110000	**0**11110000	**00**11110000
4	1010	110011001	**1**11001100	**11**11001100
5	0100	**1**00110000	**1**00110000	**11**00110000
6	0011	000011110	**0**00001111	**00**00001111

One of the principal differences between the CAC schemes and the joint codes is that for the joint codes we do not have to do divide the whole link into different sub-channels and then perform partial coding. We can perform DAP/BSC/MDR coding/decoding on the link as a whole.

4.3 Performance evaluation of the Joint Codes in a NoC platform

To evaluate the performance of the Joint CAC/SEC schemes on different NoC platforms, a system consisting of 64 IP blocks was considered, as in Chapter 2. The performance evaluation is done in terms of three principal metrics: energy savings, area overhead and timing. Messages were injected with a Poisson distribution for the sake of simulation of a real NoC environment. The routing mechanism used for the MESH and Folded Torus architectures was the e-cube (dimension order) routing. Simulations were performed using 90nm technology node parameters. The codec blocks were synthesized with the CMP [29] standard cell libraries. All the three different metrics are discussed in the following subsections.

4.3.1 Energy Savings profiling in a NoC employing joint CAC/SEC codes

The generic communication architecture of any NoC fabric is such that multiple switch blocks exist between a source and destination pair, and the communication takes place in multiple stages [20] [21]. The flits from the source nodes need to traverse multiple hops consisting of switches and wires to reach their destinations [33]. In presence of coding there is additional energy dissipation arising out of the codec blocks and redundant wires. Incorporation of CACs effectively reduces the mutual capacitance of the inter-switch wire segments. Though this helps in reducing the energy dissipation in communication, this reduction is only linear with the change in capacitance. On the other hand, the error correction codes make the system more

robust to noise, and consequently, the voltage level on interconnect can be reduced without compromising bit error rates. The reduction in voltage swing will result in significantly more energy dissipation reduction as energy and voltage swing are quadratically related. For each stage, if the energy savings due to coding is more than the energy added by the codec block and redundant wires, then there will be overall energy savings in communication between multiple cores.

4.3.1.1 Voltage Swing Reduction Due to Increased Reliability

By incorporating the joint coding schemes in a NoC data stream, the reliability of the system is enhanced. Consequently, the supply voltage can be reduced without compromising system reliability. To quantify this possible reduciton in supply voltage, a white Gaussian distributed noise voltage of magnitude V_N and variance or power of σ_N^2 is considered, that represents the cumulative effect of all the different sources of UDSM noise. This gives the probability of bit error, ε, also called the bit error rate (BER) as

$$\varepsilon = Q\left(\frac{V_{dd}}{2\sigma_N}\right) \quad . \qquad (4.1)$$

where, the *Q*-function is given by

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{-\frac{y^2}{2}} dy \quad . \qquad (4.2)$$

The word error probability is a function of the channel BER, ε. If $P_{unc}(\varepsilon)$ is the probability of word error in the uncoded case and $P_{ecc}(\varepsilon)$ *is* the residual probability of word error with error control coding, then it is desirable that, $P_{ecc}(\varepsilon) \leq P_{unc}(\varepsilon)$. Using Equation 4.1, we can reduce the supply voltage in presence of coding to $\hat{V}_{dd}$, given by

$$\hat{V}_{dd} = V_{dd} \frac{Q^{-1}(\hat{\varepsilon})}{Q^{-1}(\varepsilon)} \quad . \qquad (4.3)$$

In Equation 4.3, V_{dd} is the nominal supply voltage in the absence of any coding such that. $P_{ecc}(\hat{\varepsilon}) = P_{unc}(\varepsilon)$ Therefore, to compute the $\hat{V}_{dd}$ for the joint CAC and SEC the residual word error probability of these schemes is computed as explained below.

To compute the residual probability of word error for the DAP scheme let us call the two copies of the original data bits as A and B shown in Figure 4.3. and let us suppose that the parity in the decoder is regenerated from the copy A.

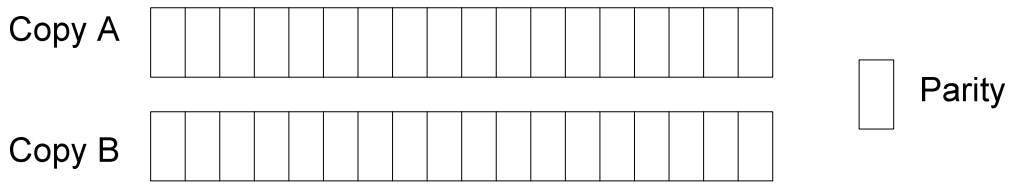


Figure 4.3: DAP encoded flit

Then for error free decoding if A is error free then the parity sent should also be error free to enable correct decoding. So, the probability of error free decoding with no errors in A is given by,

$$P_A = \sum_{i=0}^{k} \binom{k}{i} \varepsilon^i (1-\varepsilon)^{2k+1-i} \qquad (4.4)$$

If on the other hand copy B is error free and has to be selected for correct decoding then the ex-or operation between the received parity and the regenerated parity must be 1 which is possible only when the number of errors occurring in the k+1 bits of A and the received parity is odd. This event has a probability given below as

$$P_B = \sum \binom{k+1}{2i+1} \varepsilon^{2i+1} (1-\varepsilon)^{2k-2i} \qquad (4.5)$$

Therefore, the probability of error is given by

$$P_{DAP} = 1 - P_A - P_B \qquad (4.6)$$

For small probabilities of bit errors, ε the higher order terms are ignored and the residual probability for DAP can be approximated as

$$P_{DAP} \approx \frac{3k(k+1)}{2}\varepsilon^2 \qquad (4.7)$$

The residual word error probability of the other joint schemes considered here can also be shown to be the same as DAP as they essentially have the same decoding mechanism. Using this residual probability of word error the reduction in voltage swing on the interconnects for the joint CAC/SEC codes like DAP can be plotted agianst increasing values of bit error probabilities as shown in Figure 4.4.

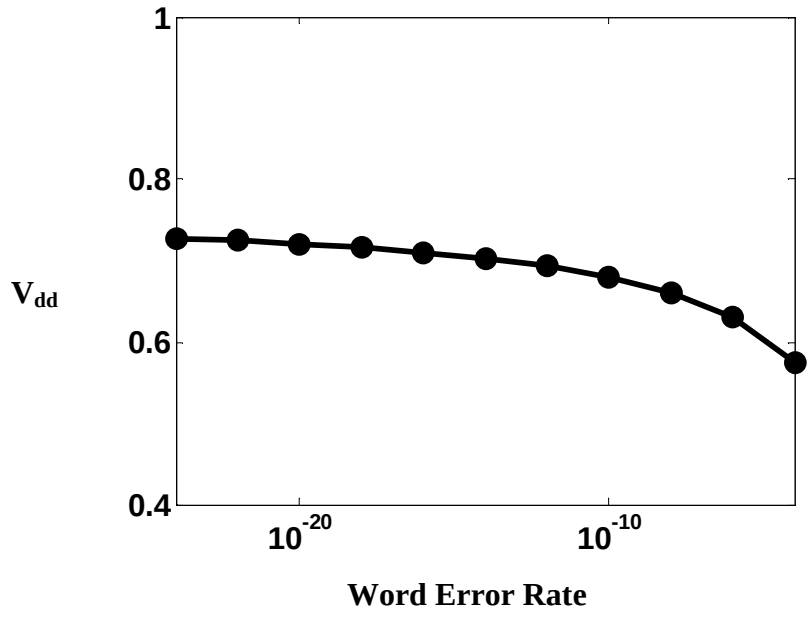


Figure 4.4: Reduction in voltage swing with variation in word error rate

4.3.1.2 Computation of Energy Savings in the Presence od Joint CAC/SEC Codes

The principal underlying the computations for evaluating the savings in energy is the same as

in Chapter 3. Following Equation 3.1 the savings in energy on a particlar interconnect link over the uncoded baseline case is given by

$$E_{savings,j} = E_{link,uncoded} - (E_{link,coded} + E_{codec}) \quad (4.1)$$

Similarly, the energy savings in transporting a single flit, say the i^{th} flit, through h_i hops can be calculated as

$$E_{savings,i} = \sum_{j=1}^{h_i} E_{savings,j} . \quad (4.2)$$

The average energy savings per flit in transporting a packet consisting of P such flits through h_i hops for each flit will be given as,

$$\overline{E}_{savings} = \frac{\sum_{i=1}^{P} \sum_{j=1}^{h_i} (E_{savings,j})}{P} . \quad (4.3)$$

The interconnect lengths and wire capacitances are calculated exactly as shown in Chapter 3 for the different NoC architectures following Equations 3.4 through 3.6.

4.3.1.3 Experimental Results

The energy dissipation and hence savings of each inter-switch wire segment is a function of λ, the ratio of the coupling capacitance to the bulk capacitance. For a given interconnect geometry, the value of λ depends on the metal coverage in upper and lower metal layers [30]. The value of λ is varied in these simulations within the two extremes for the 90nm node between 1 and 6 [30].

The energy savings profile of the same MESH network considered earlier incorporating the joint codes are shown in Figures 4.5 (a) and (b) for the two values of λ respectively.

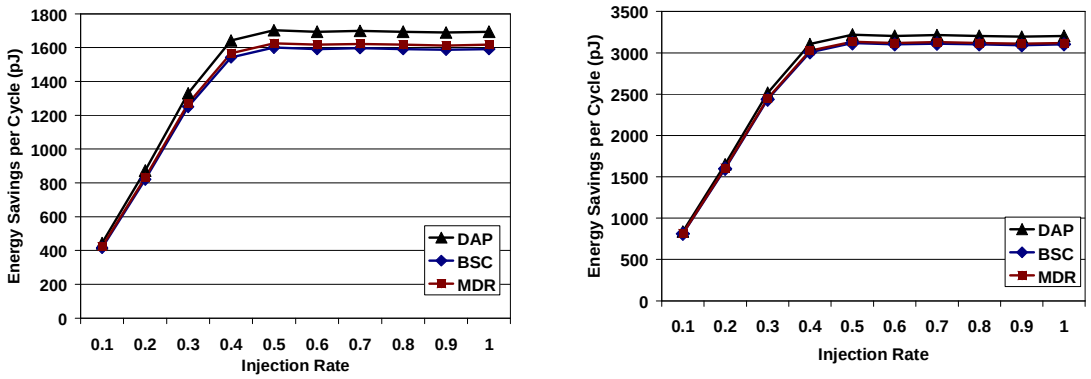


Figure 4.5: Energy Savings Characteristics for Joint Coding schemes in a MESH based NoC for (a) λ=1 and (b) λ=6.

The energy savings profile of the Folded Torus network incorporating joint codes for λ=1 and λ=6 are shown in Figures 4.6 (a) and (b), respectively. It is clear from these figures that the energy savings capability of the joint codes is more than that of the sole CAC's. Even in the λ=1 case, for a MESH-based NoC the joint codes are capable of saving energy.

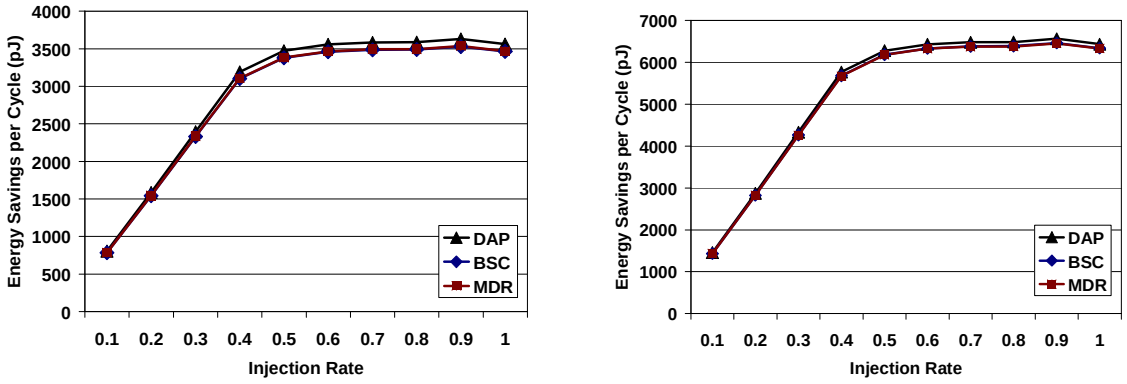


Figure 4.6: Bit Energy Dissipation characteristics for (a) λ=1 and (b) λ=6 in a Folded-Torus based NoC

4.3.2 Timing Characteristics

Following the same methodology as in the previous chapter for maintaining a pipelined communication architecture, we developed VHDL models for all the codec blocks described above and synthesized them using Synopsys' synthesis tool in the CMP [29] CMOS 90 nm

standard cell based technology. We used Synopsys Prime Time to determine the delay along the critical path in all the codec blocks. The results are shown in Table 4.2. To have a technology-independent measure of the delays, we also converted the absolute values obtained from Prime Time timing analysis tool to FO4 delay units.

These results indicate that the delay associated with each encoder and decoder is well within the ITRS suggested limit of 15 FO4, and can therefore be driven by a clock with a period of 15 FO4. So, incorporating codecs in the switch blocks does not disturb the pipelined nature of the communication fabric, though it adds extra stages. Consequently data introduction rate is not bound by the delay of the codec blocks.

TABLE 4.2
DELAY OF THE CODEC BLOCKS

Coding Scheme		Delay of the critical path (FO4)
BSC	Encoder	10.0
	Decoder	12.7
DAP	Encoder	9.6
	Decoder	11.8
MDR	Encoder	9.6
	Decoder	11.8

4.3.3 Area Overhead

While evaluating the performance of the joint coding schemes the extra silicon area the joint coding schemes add both to the NoC switch blocks and to the inter-switch buses need to be considered. Through RTL level design and synthesis in 90 nm technology node, it is found that the switches, inclusive of the network interface (NI) and without any coding scheme consist of approximately 30K gates. Here, a 2-input minimum-sized NAND structure is considered as a reference gate. In comparison to this the codecs for BSC, DAP and MDR have around 842, 679

and 685 gates respectively. This size difference is rather insignificant in overall switch design. This minor area penalty is worth the energy savings.

4.4 Conclusions

Joint Crosstalk Avoidance and Single Error Correction Codes increase the reliability of the NoC communication fabric against transient errors. This increase in reliability can be translated to a savings in energy dissipation on the interconnect links of the NoC. This can be achieved because increasing robustness can tolerate lower noise margins and hence lower voltage swing on the wires. Along with this reduction in voltage swing the reduction in crosstalk induced switching capacitance in the wires also cause a reduction in energy dissipation in communication. However, the codecs dissipate energy which must be considered while evaluating the gains from implementation of such coding schemes. The timing and area overheads are also measured and are found to be justifiable due to the gains in energy savings. Thus we can observe that joint CAC and SEC result in savings in energy on the NoC interconnects without disturbing the pipelined structure of the communication fabric.

Chapter 5

Joint Crosstalk Avoidance and Multiple Error Correction Coding

With shrinking device dimensions, the joint crosstalk avoidance and single error correction codes (CAC/SEC), discussed in chapter 4 are not sufficient to meet the high reliability requirement of Networks on Chip designed in ultra deep sub-micron (UDSM) technology. Compared with Hamming codes, standard double error correction codes like BCH codes are computationally complex. Thus, these kind of coding schemes are not very efficient from the perspective of energy and area overhead. Also, these schemes do not have any inherent crosstalk avoidance properties and being non-linear in nature crosstalk avoidance coding and multiple error correcting codes like BCH codes can not be appended in series without disturbing the properties of either of them. In this chapter a novel joint crosstalk avoiding double error correction coding scheme called Crosstalk Avoidance Double Error Correction code (CADEC) is proposed [35]. We investigate the performance of CADEC in comparison with the various existing joint CAC/SEC schemes in different NoC architectures. One point worth noting here is that, according to [12] the sole error detection followed by retransmission is a more energy efficient scheme than the error correction. To establish the performance benchmark for the CADEC scheme, we compare its performance with sole error detection (ED) codes also.

5.1 Crosstalk Avoidance Double Error Correction Code

The Crosstalk Avoidance Double Error Correction Code (CADEC) is a joint coding scheme that performs crosstalk avoidance and double error correction simultaneously. It achieves crosstalk avoidance by duplication of the bits. The same technique also increases the minimum hamming distances between codewords enabling a higher error correction capability.

5.1.1 CADEC Encoder

The encoder is a simple combination of Hamming coding followed by DAP or BSC encoding to provide protection against crosstalk. As shown in Figure 5.1(a), the incoming 32-bit flit is first encoded using a standard (38, 32) shortened Hamming code, and then each bit of the 38-bit Hamming codeword is duplicated and appended with a parity. The (38, 32) Hamming code has a Hamming distance of 3 between adjacent code words. On duplication this becomes 6 and after adding the extra parity bit this distance becomes 7. A Hamming distance of 7 enables triple error correction, but at a somewhat higher complexity cost than the double-error correcting schemes considered here. Consequently as a first step we considered only the double error correction capability. The extra parity bit, which is a part of DAP or BSC schemes, is added to make the decoding process very energy efficient as explained below.

5.1.2 CADEC Decoder

The decoding procedure for the CADEC encoded flit can be explained with the help of the flow diagram shown in Figure 5.2. The decoding algorithm consists of the following simple steps:

(i) The parity bits of the individual Hamming copies are calculated and compared with the sent parity;

(ii) If these two parities obtained in step (i) differ, then the copy whose parity matches with the transmitted parity is selected as the output copy of the first stage.

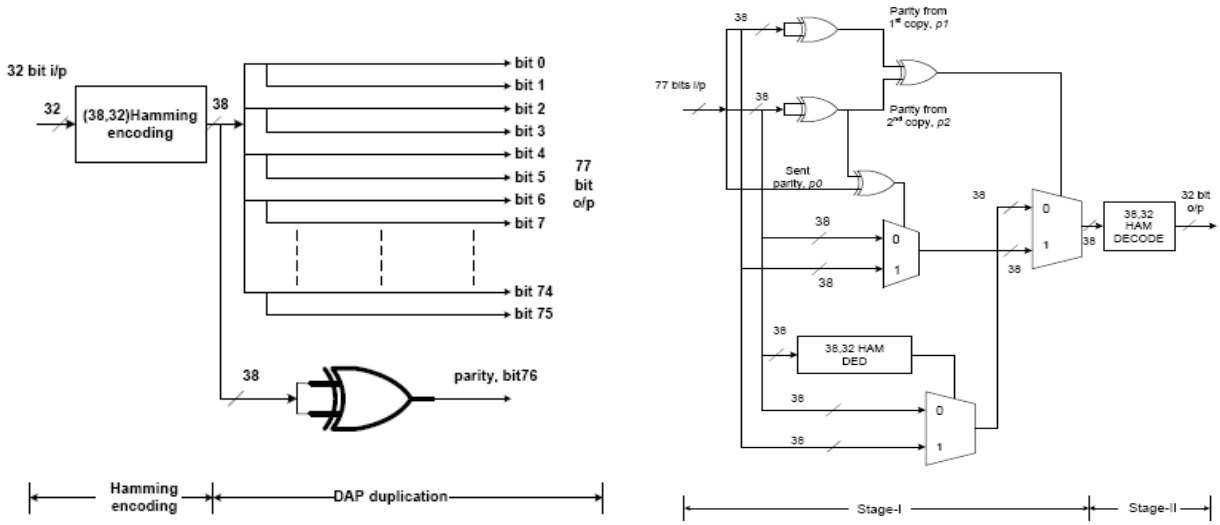
(iii) If the two parities are equal, then any one copy is sent forward for double error detection (DED) by the (38, 32) Hamming Syndrome detection block.

(iv) If the syndrome from the DED block obtained for this copy is zero then this copy is selected as the output of the first stage. Otherwise, the alternate copy is selected.

(v) The output of the first stage is sent for (38, 32) single error correcting Hamming decoding, finally producing the decoded CADEC output

The circuit implementing the decoder is schematically shown in Figure 5.1(b).

The use of the DAP or BSC parity bit actually makes the decoder more energy efficient, compared to a scheme without the parity bit, which always requires a syndrome to be computed on both copies. When the parity bits generated from individual Hamming copies fail to match, the DED-syndrome block need not be used at all, thus on average making the overall decoding process more energy efficient. This situation arises when there is single error in either one of the two Hamming copies, which, generally, will be the most probable case. We note that the circuit diagram of Figure 5.1(b) and the flowchart of Figure 5.2 show only the logic for error correction.



(a) **(b)**

Figure 5.1: (a) CADEC Encoder. (b) CADEC Decoder

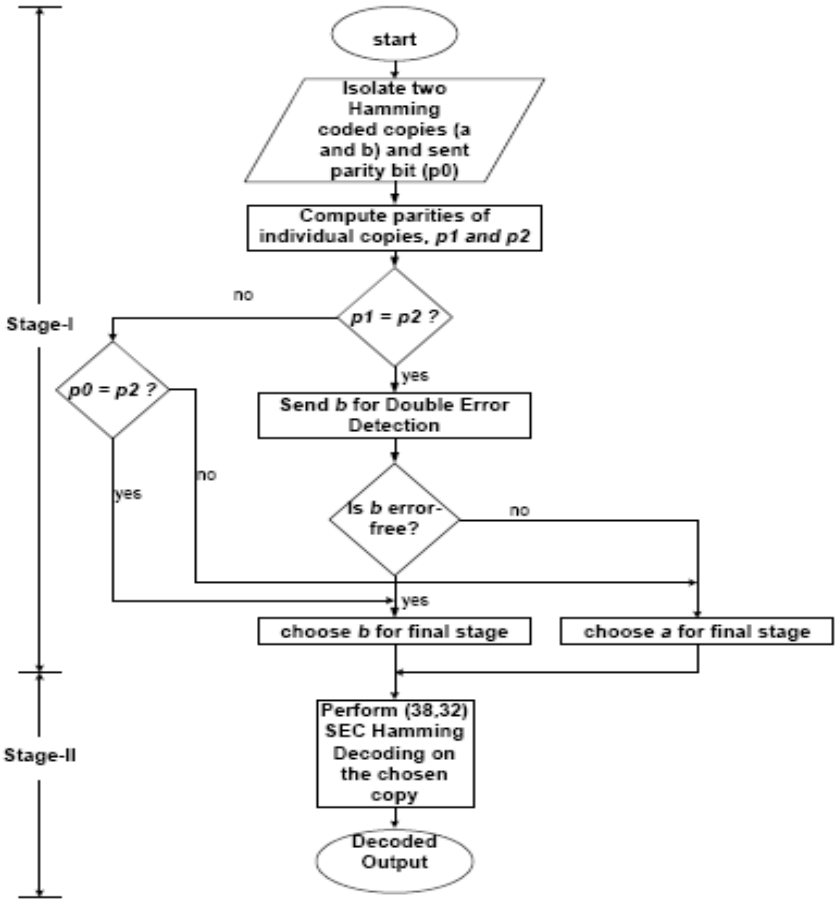


Figure 5.2: CADEC decoding algorithm

5.2 Error Detection Scheme

This scheme implements Hamming code for error detection and retransmits if the scheme detects that the flit is in error [12]. As an example, the (38,32) Hamming code implemented for a 32 bit wide flit has double error detection capability and it can reliably detect but not correct, up to two errors in the flit. The ED scheme only detects the errors; on detection of any error pattern, it sends an automatic repeat request (ARQ) signal for retransmission of the flit. The encoder is essentially only a (38, 32) Hamming encoding block. The decoder is also a standard syndrome decoder for the Hamming encoded flit. Evidently, this scheme does not have any crosstalk

avoidance properties.

5.3 Voltage Swing Reduction and Residual Probability of Word Error

In DSM NoC paradigm, reliability and energy dissipation can not be decoupled. Enhancing reliability by performing coding invariably increases the energy overhead due to the codec blocks and redundant wires. But due to increased reliability, the voltage level driving the interconnect wires can be reduced without increasing the probability of residual word error as the reduction in noise margin can be compensated by the increased error resilience [12] [13]. Considerable energy savings can be achieved by reducing the voltage level on the interconnects, since the energy dissipation depends on the square of the voltage.

5.3.1 Noise Modeling and Voltage Swing Reduction

To quantify these gains, consider a Gaussian distributed noise voltage V_N with variance σ_N^2 which models the cumulative effect of all the transient DSM noise sources as mentioned before. This gives the probability of bit error, ε, also called the bit error rate (BER) as

$$\varepsilon = Q\left(\frac{V_{dd}}{2\sigma_N}\right) \quad . \qquad (5.1)$$

Where, the *Q*-function is given by

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{-\frac{y^2}{2}} dy \quad . \qquad (5.2)$$

The residual word error probability is a function of the channel BER ε. If $P_{unc}(\varepsilon)$ is the probability of word error in the uncoded case and $P_{ecc}(\varepsilon)$ *is* the residual probability of word error with error control coding, then it is desirable that, $P_{ecc}(\varepsilon) \le P_{unc}(\varepsilon)$. Using Equation 5.1, we can reduce the supply voltage in presence of coding to $\hat{V}_{dd}$, given by

$$\hat{V}_{dd} = V_{dd} \frac{Q^{-1}(\hat{\varepsilon})}{Q^{-1}(\varepsilon)} \quad . \qquad (5.3)$$

In Equation 5.3, V_{dd} is the nominal supply voltage in the absence of any coding. To compute the $\hat{V}_{dd}$ for various schemes we find the residual word error probability for each of the schemes investigated in this thesis.

5.3.2 Residual Word Error Probability for CADEC

The probability of correct decoding can be found by considering each of the cases where the decoder can correctly decode flits despite errors. The cases where the decoder can correctly decode words with more than two errors also need to be considered. The complement of the set of correctly decoded words constitutes the set of undetected errors. This probability is given by $P_{CADEC}(\varepsilon)$. So, we have the relation:

$$P_{CADEC}(\varepsilon) = 1 - P_{correct} \qquad (5.4)$$

In the following derivation the width of the original flit is denoted by k, where *k* is 32, which is first Hamming coded to 38 bits, denoted by *n*. Each bit of the n-bit Hamming codeword is duplicated and an overall parity bit is appended. All possibilities of correct decoding are broadly divided into three categories:

(i) *Error-free transmitted parity bit:*

One of the copies has no error while the other has anywhere from zero to all bits in error. This can be correctly decoded similarly as in the DAP scheme which is integrated into the novel CADEC scheme.

(ii) *Single bit error in each copy:*

There is a single error in both copies, irrespective of the parity-bit being in error or not.

(iii) *Erroneous transmitted parity bit: There are multiple cases under this scenario*

- no errors in either copy;
- up to one error in one copy and an even number of errors in the other starting from 2 to *n* errors;
- a single error in one copy and an odd number of errors in the other.

The complete probability of correct decoding, $P_{correct}$ is given by the sum of the probabilities corresponding to the above mutually exclusive cases. In the limit of small channel BER [10], this can be expressed as

$$P_{correct} = 1 - n^2(n-4)\varepsilon^3 \qquad (5.5)$$

From Equations 5.4 and 5.5, the word error probability is

$$P_{CADEC}(\varepsilon) = n^2(n-4)\varepsilon^3 \quad . \qquad (5.6)$$

5.3.3 Residual Word Error Probability of the sole ED scheme

As pointed out in [23], any *(n,k)* linear code can detect $2^n - 2^k$ error patterns of length *n*. The probability of undetected error for any (*n*,*k*) linear code can be computed from the weight distribution polynomial of the code, *A*(*z*), given by

$$A(z) = A_0 + A_1 z + \ldots + A_n z^n \quad . \qquad (5.7)$$

where A_k is the number of codewords with weight (i.e., the number of 1s in the codeword) equal to *k*. The dual of the linear code also has an associated weight distribution, *B*(*z*), given by

$$B(z) = B_0 + B_1 z + \ldots + B_n z^n \qquad (5.8)$$

The weight distribution of the original code and its dual code are related by [23][27]

$$A(z) = 2^{-(n-k)}(1+z)^n B\left(\frac{1-z}{1+z}\right). \qquad (5.9)$$

The probability of undetected word error $P_{ED}(\varepsilon)$ for an error detection scheme using a linear code with dual weight distribution $B(z)$ is [32] [36]

$$P_{ED}(\varepsilon) = 2^{-(n-k)} B(1-2\varepsilon) - (1-\varepsilon)^n \quad , \quad (5.10)$$

where, $B(1\text{-}2\varepsilon)$ is given by $$B(1-2\varepsilon) = \sum_{i=0}^{n} B_i (1-2\varepsilon)^i \quad . \quad (5.11)$$

The ED scheme proposed in [20] uses the (38,32) shortened Hamming code for error detection, so the coefficents B_i in Equation 5.11 are obtained by using the H-matrix of that code. Using Equation 5.10, the probability of undetected error for the ED code, for small values of BER ε, turns out to be

$$P_{ED}(\varepsilon) = (n-k)\varepsilon^2 \quad (5.12)$$

where n=38 and k=32 for the (38,32) shortened Hamming code.

5.3.4 Voltage Swing as a Function of Increasing Bit Error Rate

Using Equation 5.3, along with Equations 5.6, 5.12, and 4.7 from the last chapter for the undetected word error probabilities for the different coding schemes, the tolerable voltage swing reduction can be computed against varying values of BER ε. The plot of voltage swing versus BER is shown in Figure 5.3. The nominal voltage at the 90 nm technology node is assumed to be $V_{dd} = 1.0V$.

As can be seen from Figure 5.3, the voltage swing is lower than the nominal voltage for all the coding schemes. The CADEC scheme provides maximum voltage reduction as it can correct and also detect more errors than the others. For the purpose of simulations the voltage swings for different coding schemes corresponding to the channel BER of 10^{-20} is used.

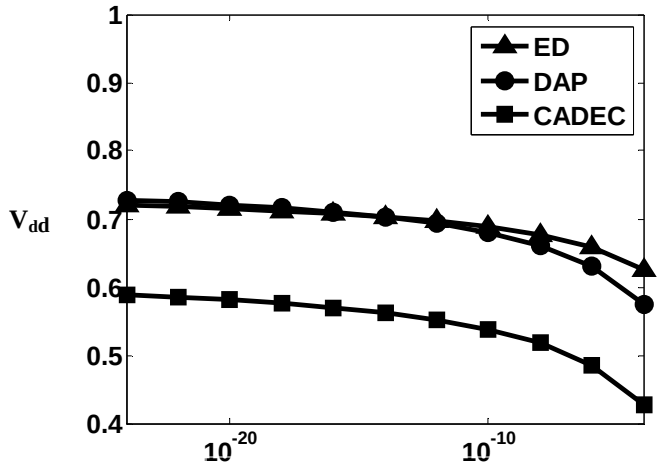


Figure 5.3. Variation of achievable voltage swing with bit error rate for different coding schemes

5.4 Expected Energy Dissipation in Presence of Errors

The schemes investigated here implement corrective intelligence either in the form of joint crosstalk avoidance and forward error correction or error detection followed by retransmission. In the error detection (ED) scheme, whenever an error is detected, the receiving switch asks for retransmission from the previous one. In contrast, the joint crosstalk avoidance and single/multiple error correcting codes ask for retransmission only when the number of errors in a flit exceeds their correction capability. An interesting study is to compare the expected energy dissipation per bit for each of the schemes, given that there is an error in the flit when it is transmitted for the first time. In the following derivations the coded flit length *m* is assumed to be 38 for the ED scheme, 65 for DAP, BSC and MDR, and 77 for CADEC.

The retransmission mechanism used for each of the schemes to avoid data loss, is a switch-to-switch, flit level retransmission. If the number of errors in a flit is more than the correction capability of the coding scheme then an automatic repeat request (ARQ) is sent and the erroneous flit is retransmitted. The ED scheme sends ARQ in presence of even a single error. This necessitates adequate buffering at the switches for the flits already transmitted. So, there is

an additional energy expenditure associated with the retransmission buffers [20]. The energy dissipation associated with the ARQ signal needs to be considered as well.

5.4.1 Error Detect and Retransmit Scheme-ED

The probability of the flit having an error in the first transmission is given by the following equation, in which the last equality assumes small BER ε:

$$P_{error} = P(\geq 1) = 1-(1-\varepsilon)^m = m\varepsilon \quad . \qquad (5.13)$$

Let the event that there is an error in the first transmission be *B*, and the event that the i^{th} transmission is the first error free transmission after i-1 erroneous transmissions be *A*. Then the conditional probability for event *A* given event *B* has occurred can be computed as

$$P(A/B) = \frac{P(A \bigcap B)}{P(B)} \qquad (5.14)$$

As *A* is the event that the first (*i-1)* transmissions have errors and *B* is the event that the very first transmission has at least a single error we can observe that event *A* implies event *B.* Thus we may say that $A \cap B$ equals only *A.* Now, the probability of *i* repeated transmissions is given by the probability of *i*-1 transmissions with at least one error and the i^{th} transmission without any error which is $[P(\geq 1)]^{i-1}(1-P(\geq 1))$. So, the conditional probability of *i* repeated transmissions given an error in the first transmission is

$$P_i = P(A/B) = \frac{[P(\geq 1)]^{i-1}(1-P(\geq 1))}{P_{error}} \quad . \qquad (5.15)$$

Hence the expected energy dissipation is given by the following infinite sum, which accounts for all possible transmissions:

$$Ex[E_{bit,ED}/Error] = \sum_{i=2}^{\infty} P_i \cdot i \cdot E_{ED} \quad . \qquad (5.16)$$

In Equation 5.16, the number of transmissions i starts from 2 as that is the least number of transmissions needed if the first transmission always has an error, and $E_{ED} = E_{bit,ED} + E_{bit,buf} + E_{ARQ}$. Here, $E_{bit,ED}$ is the energy dissipated per bit in a inter-switch link in case of the sole ED scheme. The energy factor also includes the energy per bit for the buffer storage, $E_{bit,buf}$ and the energy dissipation for the ARQ bit, E_{ARQ}. Thus $i \cdot E_{ED}$ is the energy dissipated per bit in *i* repeated transmissions for the ED scheme. This gives the expected energy dissipation for the ED scheme as

$$Ex[E_{bit,ED} / Error] = \frac{(2 - m\varepsilon)}{(1 - m\varepsilon)} E_{ED} . \quad (5.17)$$

where *m* is the total number of bits in the coded flit. For small ε the above equation simplifies to

$$Ex[E_{bit,ED} / Error] = [2 + m\varepsilon]E_{ED} . \quad (5.18)$$

It is evident from Equation 5.18 that the expected value of energy dissipation in the ED scheme is more than twice that of a single transmission in presence of errors.

5.4.2 DAP, BSC and MDR coding schemes:

If the DAP, BSC and MDR schemes were enhanced using a retransmission mechanism, then we would expect the energy dissipation to depend on the retransmission probability. The difference between the joint CAC/SEC schemes and the ED scheme is that the joint code will send an ARQ only when there is more than one error in the flit. For any single error the schemes will correct the flit on the fly. Once again, let *A* be the event that there are *i-1* transmissions with more than one error, which necessitated retransmission for *i-1* times, while the last i^{th} transmission has one or less errors. Also, let *B* be the event that the first transmission had at least

one error. As in the case of the ED scheme, we are interested in determining P(A/B). As before, $A \cap B = A$ as A is a subset of B. The conditional probability of having $i>1$ repeated transmissions, given an error in the first transmission, follows from Equation 5.15 and is given by

$$P_i = \frac{P(\geq 2)^{i-1} P(< 2)}{P_{error}} \quad . \qquad (5.19)$$

Here P_{error} is obtained from Equation 5.14, $P(<2)$ is the probability of having less than two erroneous bits in the flit, and $P(\geq 2)$ is the probability of having two or more errors in the flit which is given by $1 - P(< 2)$. Now, for i=1, the flit had exactly one error and hence was correctable; this probability is given by

$$P_{i=1} = \frac{P(1)}{Perror} = \frac{m\varepsilon(1-\varepsilon)^{m-1}}{m\varepsilon} \approx 1-(m-1)\varepsilon \qquad (5.20)$$

The expected value of the energy dissipation is given by the following sum similar to Equation 5.17

$$Ex[E_{bit,DAP} / Error] = \sum_{i=1}^{\infty} P_i \cdot i \cdot E_{DAP} \quad , \qquad (5.21)$$

where $E_{DAP} = E_{bit,DAP} + E_{bit,buf} + E_{ARQ}$ and $E_{bit,DAP}$ is the energy dissipated per bit in a inter-switch link in case of the DAP scheme. As before, the retransmission buffer energy and the ARQ energy are also included. Equation (26) can be simplified for small values of ε as

$$Ex[E_{bit,DAP} / Error] = [1 + \frac{m(m-1)^2}{4} \varepsilon^3] E_{DAP} . \qquad (5.22)$$

Equation 5.22 also gives the expected value of energy dissipation per bit (given an initial error) for BSC and MDR, since they have the same error correction capability as DAP. From Equation 5.22, the expected energy dissipation per bit when an error has occurred is less in the case of DAP, BSC or MDR codes than in the case of ED, as they send an ARQ only when there

is more than a single error which happens less often than a single error occurring in the transmitted flit.

5.4.3 CADEC scheme:

In CADEC, the expected energy per bit will be less than in ED, as CADEC retransmits only when there are three or more errors compared to ED which retransmits even when there is a single error.

For CADEC, the event *A* will be *i*-1 transmissions with more than two errors and the last transmission with two or less errors. The event *B* as before will be the case when the first transmission is in error. Follwing similar arguements as in the case of ED and DAP, $A \cap B = A$. Hence, the conditional probability of *i* repeated transmissions, where *i*>1, given that the first transmission has an error, is given by

$$P_i = \frac{P(\geq 3)^{i-1} P(< 3)}{P_{error}}, \qquad (5.23)$$

where *P(<3)* is the probability of having 0, 1 or 2 errors in the flit and $P(\geq 3)$ is the probability of having more than two errors and equals $1 - P(< 3)$.

However, if the first transmission has two or less errors then there will be no retransmissions and this event has the probability

$$P_{i=1} = \frac{P(1)}{P_{error}} + \frac{P(2)}{P_{error}} \approx 1 - \frac{(m-1)}{2}\varepsilon, \qquad (5.24)$$

where *m* is the number of bits in the coded flit.

Similar to the other schemes the expected value of the energy dissipation in this case is given by

$$Ex[E_{bit,CADEC} / Error] = \sum_{i=1}^{\infty} P_i \cdot i \cdot E_{CADEC} \qquad (5.25)$$

where $E_{CADEC} = E_{bit,CADEC} + E_{bit,buf} + E_{ARQ}$ and $E_{bit,CADEC}$ is the energy dissipation per bit for the CADEC scheme. The energy dissipation per bit for the retransmission buffer, $E_{bit,buf}$ and that for the ARQ bit, E_{ARQ} are also considered in Equation 5.25.

The final expected value of the energy dissipation given there is an error in the flit in presence of CADEC coding simplifies (in the limit of small [13]) to

$$Ex[E_{bit,CADEC}/Error] = [1 - \frac{(m-1)}{2}\varepsilon]E_{bit,CADEC}. \quad (5.26)$$

From the above analysis, it is evident that in the event of an error the ED scheme on an average dissipates about two times more energy than the CADEC scheme per bit, ignoring the ε term which is much less than unity.

An important point worth mentioning here is that $E_{bit,DAP} > E_{bit,CADEC}$ and $E_{bit,ED} > E_{bit,CADEC}$. This is because the voltage reduction owing to enhancement in reliability is more for the CADEC scheme compared to the other two as seen in Figure 5.3. The effective switching capacitance of adjacent wires in presence of crosstalk avoidance coding in CADEC is less than that for the ED scheme which does not guard against crosstalk. Though the coupling capacitances in DAP, BSC and MDR are same as that in CADEC, they need a higher voltage level due to their lower error correction capability. As these two factors, namely, voltage swing and switching capacitance, are the primary contributing factors towards energy dissipation, the energy expenditure per bit per hop is much less for CADEC compared to the other.

5.5 Performance Analysis of the CADEC scheme

As in the previous chapters, the performance analysis of the CADEC scheme is done based on the three important metrics of energy dissipation, timing requirements and area overhead. The analysis is done on a 64-IP NoC platform implementing two of the most commonly used NoC

architectures like MESH and FOLDED-TORUS. As the characteristics of the joint single error correction codes are very similar and it is shown in the last chapter that DAP is the most efficient of those codes, here only DAP is used for the purpose of comparison with CADEC. For the purpose of simulation messages were injected with a Poisson distribution. The routing mechanism used throughout the simulations was *e-cube* (dimension order) routing [21]. Simulations were performed assuming 90nm technology node parameters exactly like in the previous two chapters.

5.5.1 Energy Savings in an NoC by employing CADEC

Following the same principles as in the previous chapters the savings in energy dissipation is studied as a function of the network dynamics. As the energy dissipation shows a saturating trend with increasing injection rate the energy savings profile also shows similar tendencies. There are several factors to be considered while evaluating the savings in energy like voltage scale reduction due to increase in reliability, reduction in crosstalk capacitance on the wires and additional energy dissipation due to the codec blocks implementing the coding schemes.

Taking all factors into consideration the metric for comparison of energy savings takes into account the savings in energy due to the reduced voltage swing and crosstalk, additional energy dissipated in the extra redundant wires and the codecs. The savings in energy per flit per hop is given by,

$$E_{savings,\,j} = E_{link,uncoded} - (E_{link,coded} + E_{codec}) \qquad (5.27)$$

where $E_{link,\,uncoded}$ and $E_{link,coded}$ are the energy dissipated by the uncoded flit and the coded flit in each inter-switch link respectively. E_{codec} is the energy dissipated by each codec. The energy savings in transporting a single flit, say the i^{th} flit, through h_i hops can be calculated as

$$E_{savings,i} = \sum_{j=1}^{h_i} E_{savings,j} \ . \qquad (5.28)$$

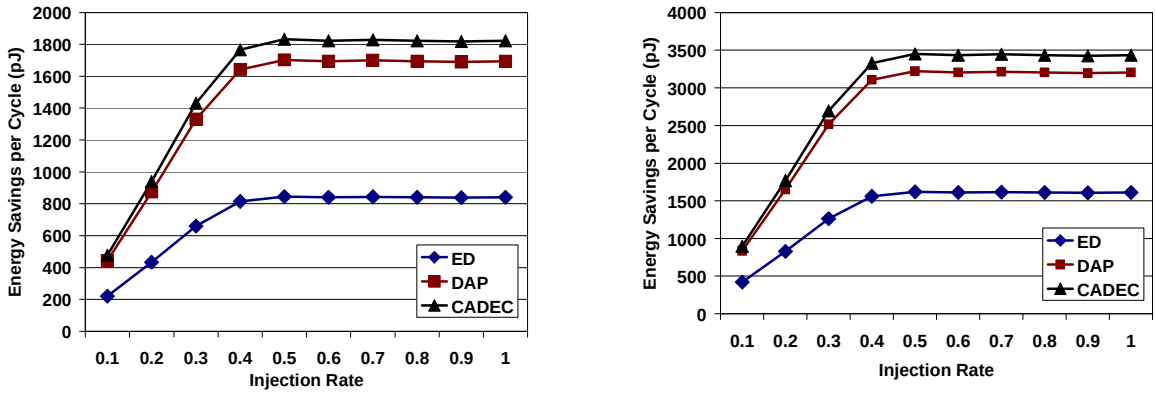
The average energy savings per flit in transporting a packet consisting of P such flits through h_i hops for each flit will be given as,

$$\overline{E}_{savings} = \frac{\sum_{i=1}^{P} \sum_{j=1}^{h_i} (E_{savings,j})}{P} . \qquad (5.29)$$

Once again, the metric $\overline{E}_{savings}$ is independent of the specific switch implementation, which may vary based on the design.

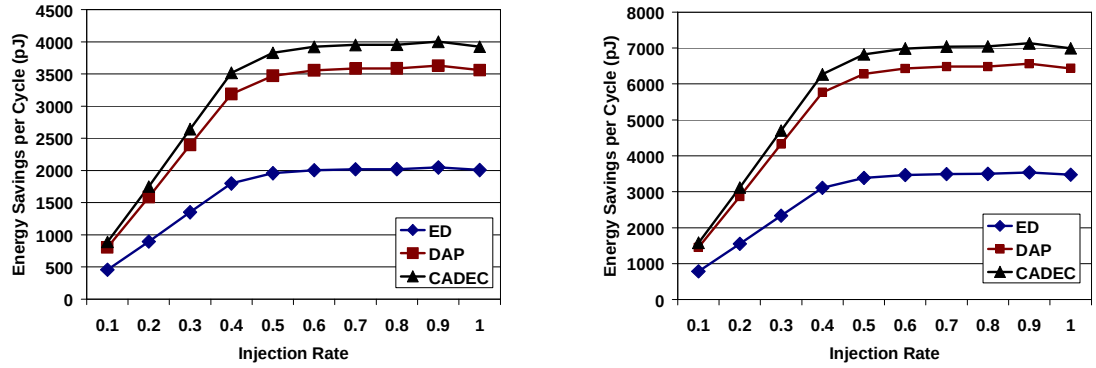
In order to quantify the energy savings profile for a NoC interconnect architecture, we determine the energy dissipated in each codec, E_{codec} by running Synopsys™ Prime Power on the gate-level netlist of the codec blocks implemented using the CMP [29] library in the 90nm Technology. To determine the inter-switch link energy in presence and absence of coding, that is, $E_{link,coded}$ and $E_{link,uncoded}$ respectively.

The actual energy dissipation and hence the savings of each inter-switch wire segment is a function of λ, the ratio of the coupling capacitance to the bulk capacitance. For a given interconnect geometry, the values of λ depends on the metal coverage in upper and lower metal layers. At the 90 nm technology node, the two extreme value of λ are 1 and 6 respectively [30]. The figures below show the energy savings profile for the Mesh and Folded-Torus architectures for two representative values of λ for the 90nm technology node 1 and 6.



(a) **(b)**

Figure 5.4. Average energy savings for all the schemes for MESH-based NoC at (a) λ=1 and (b) λ=6



(a) **(b)**

Figure 5.5. Average energy savings for all the schemes for FOLDED TORUS-based NoC at (a) λ=1 and (b) λ=6

As can be inferred from Figures 5.4 and 5.5, the energy savings is much more pronounced in case of the Folded-Torus network architecture. This is because the interconnect lengths are double in the case of a Folded-Torus NoC fabric as compared to that in a Mesh. Hence the savings are more as they only occur on the wires and are proportional to the length of the link.

5.5.2 Timing Requirements

Following the same principle as for the other coding schemes if the encoder and the decoder of the CADEC scheme have critical path delays less than one clock cycle or 15 FO4 the system

can be operated without any penalty on the clock cycle time or the throughput of the system. The critical path delays of teh all the joint coding schemes considered in this work are listed in Table 5.1 including that for the ED scheme.

All of these codecs have delay less than a single clock cycle, even CADEC. Thus all the schemes including CADEC can enable the entire NoC to operate at the same throughput as without the coding system and in effect only increases the depth of teh pipeline which influences only the latency of the NoC.

Table 5.1. Critical Path Delays for the Codec Blocks

Coding Scheme		Delay (FO4)
ED	Encoder	8.2
	Decoder	13.3
DAP	Encoder	9.6
	Decoder	11.8
BSC	Encoder	10.0
	Decoder	12.7
MDR	Encoder	9.6
	Decoder	11.8
CADEC	Encoder	13.1
	Decoder	14.0

5.5.3 Area Overhead

For the sake of complete comparisons the silicon area required by the codec blocks for each of the coding schemes must also be reported. Through RTL level design and synthesis in Synopsys^{TM} Design Analyzer the silicon area consumed by each codec was obtained as shown in Table 5.2. The figures are expressed in units of a minimum sized 2-input NAND gate,.

Table 5.2. Area Overhead of the Coding Schemes

Coding Scheme	Area (2-input NAND gate)
ED	816
DAP	678
BSC	842
MDR	684
CADEC	1357

The switches along with the Network Interface (NI) consist of approximately 30K minimum sized NAND gates. Consequently, the area overhead arises due to all the coding schemes is not significant. This small overhead is a small price to pay for the enhanced reliability and high gains in energy savings from incorporating the coding schemes. Another extra area overhead arises from the retransmission buffers. Following [20] for full throughput operation these buffers account for around 1200 two input NAND gates per switch port. This additional area overhead can be avoided by adopting a coding scheme with higher error correction capability. As shown in (14), the word error probability and hence the probability of retransmission is proportional to ε^3 for the CADEC scheme. Assuming a typical bit error rate, ε, of 10^{-20} , the probability of retransmission is extremely low. Consequently, even without provision of retransmission the probability of data loss will be negligible. This suggests that higher order error correcting codes will be more area efficient than retransmission-based mechanisms.

5.6 Conclusions

By incorporating joint *crosstalk avoidance and double error correction coding*, it is possible to simultaneously enhance the reliability of the NoC's and lower the energy dissipation, despite the associated redundant wires and codec logic requirements. As verified through detailed analysis and simulations, the proposed CADEC scheme lowers the energy dissipation compared

to all other existing schemes studied here. The principal sources of energy savings arises from two factors, namely, the possibility of lowered voltage swing, and reduction of mutual switching capacitance of the inter-switch wire segments. From the analysis carried out in this work, it can be concluded that coding schemes with higher order correction capability outperforms sole retransmission-based mechanisms interms of enrgy and area overhead.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

Shrinking device dimensions and dense packing of interconnect wires in the current and future technlogy nodes makes signal integrity issues alarming in the design of Networks-on-Chip (NoC). Corrective measures should be adopted at the design level to address transient errors issues. In this work it is shown that by incorporation of coding schemes on the data to be transmitted on NoC interconnects it is possible to achieve increase in transient error resilience. We have seen that Crosstalk-Avoidance-Codes can be implemeted on the data-stream to guard against worst-case crosstalk in adjacent wires. This not only results in reduction of crosstalk but also enables lower energy dissipation in the NoC interconnect fabric due to reduced coupling capacitance among the wires. As a development on that concept it is shown that implementation of joint crosstalk avoidance and single error correction schemes like DAP, MDR and BSC can be used to reduced crosstalk as well as simultaneously correct a single transient error in the data stream. These coding schemes had an advantage over the sole CAC's as they allowed a reduction in the voltage swing driving the interconnects due to increased tolerance to transient noise. Thus by allowing a lower noise margin the joint codes were able to achieve a higher savings in energy dissipation compared to the sole CAC schemes.

The major contribution of this work is the development of a novel coding scheme that combines the advantages of both crosstalk avoidance as well as forward error correction techniques. The name of the scheme is Crosstalk Avoidance Double Error Correction scheme or CADEC. As the name suggests this code has forward error correction capability of upto two

errors along with the best crosstalk avoidance capacity. As a result this scheme can tolerate even lower noise margins and can operate with the same error rate at lower voltage swings driving the interconnect. Thus the energy savings obtained with CADEC is more than any other coding schemes existing in the NoC pardigm.

6.2 Future Directions

The research performed for this thesis work has several far reaching directions as discussed below:

6.2.1 Extension of the CADEC scheme

The CADEC scheme can be extended to a family of Joint Crosstalk Avoidance Multiple Error Correction and Detection scheme which can correct and detect multiple errors at the same time. The CADEC encoder is such that the minimum Hamming distance any adjacent code words is 7. This enables up to triple error correction and quadruple error detection. One interesting point is that, by transmitting an extra parity bit for both the Hamming codes to make both copies (39,32) codes each with d_{min} = 4, we can achieve triple error correction and quadruple error detection simultaneously. In addition to design of the new family of codes comparisons have to be made with other coding schemes like BCH and Hamming to establish proof of the efficeincy of this methodology.

A comparison of coding methodologies in general to other circut level reliability methodologies like radiation hardened circuits, Triple Modular Redundancy methods need to be made to estabish our method as a viable alternative to such schemes.

6.2.2 Carbon Nanotube Interconnects

Beyond the 32nm Technology node the interconnects will change drastically as predicted by ITRS. It can be shown that nano wires can be engineered to outperform copper interconnects in

the future technology generations. Interconnects will be made of carbon nanotubes and nanowires. Manufacture of such nanoscale structures usually follow a methodology called self-assembly. This process is extremely unreliable and error prone. The defect rate for these wires is predicted to be in the 1% to 15% range. Hence reliability issues will be a major challenge in nano technology too. New even more robust schemes need to be designed to address the increased concerns of transient error resilience. The applicability and advantages of the CADEC scheme developed here can also be investigated in that technology. It can be conjectured that handling the signal integrity issues associated with nanowires will only be effectively achieved using design-stage solutions in addition to the solutions available in manufacturing and post-design stages. We therefore propose to extend the coding methodology proposed in this work to the nano domain.

6.2.2 Three Dimensional NoC

Three dimensional (3D) Network on Chip (NoC) has recently attracted researchers' attention. 3D NoC's are capable of achieving better system throughput and lower latency compared to the corresponding 2D implementations. To fully exploit the performance benefits of 3D architectures, it is imperative to address signal integrity issues in the design phase and its implications on energy dissipation. My near future research direction will be investigating the applicability and efficiency of the designed coding methods in different 3D NoC architectures. The scenario for the 3-D NoC's is a little different than in a planar NoC as the vertical wires there are usually much shorter in the order of a few hundred microns. Hence, the savings on the vertical wires might not be so well pronounced. However, I expect that since the vertical wires will be used only for a fraction of times the planar interconnects are used the coding methodologies will still have considerable advantage over an uncoded case.

6.2.3 Burst Error

Sometimes due to inadvertent faults in the chip or some drastic transient phenomena burst errors may be caused in a particular flit. Among other causes, this can happen due to a wire laterally crossing a bus or due to a surge in the power supply. Crosstalk is also a cause of burst errors. A possible extension of the research described in this thesis can be to explore various causes of burst errors in on-chip environments and design of smart low-latency and low memory burst error correction codes.

6.3 Summary

NoC has emerged as an enabling solution for integration of huge number of embedded IP cores on a single die. In this communication centric paradigm reliability issues assume alarmingly large significance. Smart methodologies have to be adopted at the design phase to address transient failures to enable proper functionality of the system. Through efficient code design higher reliability and lower energy dissipation can be achieved while keeping the overheads within acceptable limits.

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Appendix A

Publications

Following is a list of publications published in reputed conferences during the course of this research.

Conference:

1. Amlan Ganguly; Partha Pande; Benjamin Belzer; Cristian Grecu, “Addressing Signal Integrity in Networks on Chip Interconnects through Crosstalk-Aware Double Error Correction Coding”, IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2007, May, 2007.

2. P.P. Pande. A. Ganguly, B. Feero, C. Grecu, “Applicability of Energy Efficient Coding Methodology to Address Signal Integrity in 3D NoC Fabrics”, IEEE International ON-line Test Symposium (IOLTS), July, 2007.

3. Pande, P.P.; Ganguly, A.; Feero, B.; Belzer, B.; Grecu, C "Design of Low Lower & Reliable Networks on Chip through Joint Crosstalk avoidance and forward error correction coding", Defect and Fault Tolerance in VLSI Systems, 2006. DFT '06. 21st IEEE International Symposium on Oct. 2006 Page(s):466 – 476.

4. Pande, P.P.; Haibo Zhu; Ganguly, A.; Grecu, C, “Energy Reduction through Crosstalk Avoidance Coding in NoC Paradigm", Digital System Design: Architectures, Methods and Tools, 2006. DSD 2006. 9th EUROMICRO Conference on 2006 Page(s):689 – 695.

5. Partha Pratim Pande; Haibo Zhu; Amlan Ganguly; Grecu, C.; "Crosstalk-aware Energy Reduction in NoC Communication Fabrics", International SOC Conference, 2006 IEEE Sept. 2006 Page(s):225 – 228.

Journal:

1. A. Ganguly; P.P. Pande; B. Belzer; C. Grecu, "Design of Low power & Reliable

Networks on Chip through joint crosstalk avoidance and multiple error correction coding"; Journal of Electronic Testing: Theory and Applications. (Communicated)

2. P.P. Pande; H. Zhu; A. Ganguly; C. Grecu, “Energy Reduction through Crosstalk Avoidance Coding in Networks on chip"; Journal of System Architecture. (Communicated)