DESIGN OF A NEW TRANSFORMER ISOLATED ANALOG ACQUISITION SYSTEM HAVING GREATLY REDUCED TRANSFORMER SIZE AND WEIGHT WHILE ACHIEVING HIGH ACCURACY

By

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To the Faculty of Washington State University:

The members of the Committee appointed to examine the thesis of TIMOTHY MICHAEL MINTEER find it satisfactory and recommend that it be accepted.

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Chair

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Abstract

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The design of a new transformer isolated analog acquisition system greatly reduces the size, weight, and cost of the isolation transformer. The concept of pulsing the isolated analog signal only for the portion of time needed for A-D conversion is developed. High accuracy of the isolated analog signal is achieved using an operational amplifier with a feedback winding from the isolation transformer. The additional use of the isolation transformer for an isolated switched mode power supply is also developed. The implementation of the isolation transformer using a small E-E ferrite core and printed circuit windings is described.

A SPICE (Simulation Program with Integrated Circuit Emphasis) model is developed for the E-E ferrite core, printed circuit board winding transformer used in the Isolated Analog Selector circuit. SPICE models for the part-to-part and temperature extreme variations identify the design constraints of the isolation transformer. SPICE models of the electronic control circuitry used in the new isolated analog acquisition system help identify, measure, and improve the stability and accuracy of the design.

An FEA (Finite Element Analysis) tool is used to determine the accuracy of the isolation transformer of the isolated analog acquisition system. The FEA tool assists in improving the isolation transformer's coupling accuracy by identifying the optimum placement of traces for the printed circuit board windings. The test results of a prototype circuit incorporated into an existing digital protective relay product are presented.

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Chapter 1 Introduction

Analog acquisition systems are common in digital protective relays (used throughout the power industry), SCADA (Supervisory Control and Data Acquisition) and a vast number of other control and data acquisition systems found in the automotive, industrial and medical fields (to name a few).

A new approach to a transformer isolated analog acquisition system is desirable to reduce the volume and weight of the acquisition components and circuits while maintaining or improving the circuit quality, performance, and cost. The Isolated Analog Selector circuit presented is a significant step towards achieving these goals.

The Isolated Analog Selector circuit greatly reduces the transformer size and weight for a digital protective relay sampling 60 Hz current and voltage signals. The reduction is accomplished by only transforming the analog signal across the isolation barrier for the portion of time needed by the A-D converter for proper conversion to digital sampled data. Instead of requiring an isolation transformer to support the full 60 Hz signal, the isolation transformer only needs to support a limited "snapshot" of the waveform for A-D conversion every sampling interval. High accuracy is achieved even with the reduction in transformer size and weight.

The isolation transformer and other circuitry used in the Isolated Analog Selector are cost effectively implemented and easily assembled using the reliable and high quality printed circuit board processes. Design details and accuracy analysis of the Isolated Analog Selector circuit are presented.

Prototype Isolated Analog Selector circuits were built and tested in a digital protective relay. Test results and performance improvements are also presented for prototype implementation.

1.1 Background

Most acquisition systems require some form of isolation between the analog signal to be sampled and the digital control system/computer itself. The isolation is generally needed for safety reasons as well as protection of the digital control system from damage during transients. Digital protective relays, for example, require 2.5 kV of isolation (@ 60 Hz) between the CT (current transformer) and VT (voltage transformer) signals and the digital circuitry of the digital protective relay [1].

Typically, isolation is achieved with an isolation transformer. The transformer consists of a primary winding and a secondary winding that are insulated from each other to meet the isolation requirements. The transformer must be designed to support the current or voltage range of the analog signal as well as the low frequency (50 or 60 Hz) of the analog signal. By design, the transformer secondary analog signal should be a linear representation of the primary analog signal. In other words, the secondary (isolated) analog signal should have the same frequency, a proportional magnitude and a constant phase delay with respect to the primary signal.

Digital protective relays typically use a transformer with an iron-based core (with E-I laminates) to isolate the 60 Hz CT or VT signal. The transformer core is physically big enough to support the largest waveform that is to be measured. The isolation transformer for the CT signal has many known drawbacks. First, for large fault currents (which can have a fully decaying dc offset), the isolation transformer may saturate. Secondly, for

low CT signals, the transformer may become very non-linear. And third, the phase through the isolation transformer is not consistent from part to part or over the entire range of the CT signal.

The construction of iron-based core transformers is a manual labor-intensive process. The Es and Is of the core laminates are manually placed into bobbins (the last few usually being forced). Insulation tape is manually added between primary and secondary magnetic wire layers. The magnetic wires are manually soldered to lead wires or binding post to provide the interface for crimp terminals or wave soldering on a printed circuit board. The transformer is typically impregnated or dipped in varnish to protect the magnetic wires from the environment. These manual steps in the construction of a transformer impact the quality and reliability of the component.

Another issue with iron-based core isolation transformers is the size and weight they add to a device. Digital protective relays, for example, may have twelve isolation transformers that weigh approximately 2/3 pound each for a total of 8 pounds, constituting a significant portion of the relay's size and weight. Each transformer has dimensions of around 1.5" x 1.5" x 2", and cost in the $5 to $8 range.

If the analog signal is extremely low frequency (for example various power, frequency, and temperature transducers), conventional isolation transformers cannot be used to isolate the analog signal. Typically, for these types of signals, non-galvanic isolation is achieved with a differential amplifier circuit or galvanic isolation is achieved with an isolation amplifier. Both methods have known drawbacks. The differential amplifier, in addition to not providing galvanic isolation, may have poor common mode

rejection (depending on how closely matched the resistances are). Isolation amplifiers typically are costly and require power supplies on both sides of the isolation module.

Some isolation amplifiers actually convert the analog signal to digital, cross the isolation barrier with the digital data and then convert the digital data back to an analog signal. An acquisition system based on this approach would be more sensibly implemented by leaving the data in digital form and bringing it directly into the digital processor of the control system (i.e. not converting it back to analog first). This would require an A-D converter for each channel located on the input analog signal side of the isolation barrier.

Many acquisition systems require high accuracy for the sampled isolated analog signals. For example, some digital protective relays incorporate a 16 bit A-D converter and need precision of the metered current or voltage to within ±0.1% of the metered value. For a current or voltage near the lower limit of the specified input range, ±0.1% may be a few to a small number of counts of the 16 bit A-D converter. It is also important that this accuracy is maintained over operating temperature extremes of the acquisition system circuitry (i.e. –40 to 85 °C).

Conventional differential amplifiers and isolation amplifiers either do not have the necessary precision or are too costly. For a digital protective relay, this type of isolation amplifier may cost many times the conventional iron core CT or VT signal isolation transformer. A key aspect of an analog signal isolation system is high accuracy at a low cost.

Most acquisition systems, for economy of scale purposes, have a single A-D converter that sequentially samples every analog signal (or channel) in the system in a

round-robin type fashion. For example, a digital protective relay that has six CT (IAW, IBW, ICW, IAX, IBX, and ICX) and six VT (VAY, VBY, VCY, VAZ, VBZ, and VCZ) input signals, may sequentially sample IAW, IBW, ICW, IAX, IBX, ICX, VAY, VBY, VCY, VAZ, VBZ, and VCZ every 125 μs, or 8 kSPS (kilo samples per second) per channel.

An acquisition system with a single A-D converter requires an analog multiplexer to individually select only one of the channels for conversion by the A-D converter. In addition, as with any sampling acquisition system, a LPF (Low Pass Filter) is required for each channel to prevent aliasing from occurring due to the sampling process.

There are many advantages to reducing the bulkiness of the isolation transformers: reduction in shipping costs (for both the individual transformers as well as the digital protective relay), ease of handling, and reduction in the space requirements for mounting and installation.

The new transformer isolated analog acquisition system significantly reduces the size (1/40 the volume), weight (1/50 the mass), and cost (1/10) of the isolation transformer compared to the traditional digital protective relay CT and VT signal transformers. For a typical digital protective relay, a 2/3 pound isolation transformer can be replaced with a transformer having an E-E ferrite core of around 0.2 ounces, utilizing printed circuit board traces as windings. As discussed in the next section, the reduced transformer size is realized by transformer isolating the CT and VT signal content at a higher switching frequency. The reduction is analogous to switched mode power supply isolation transformers being greatly reduced in size, weight, and cost compared to older style, 50/60 Hz isolation transformers used in linear power supplies.

As with switched mode power supplies, the bulky, single component 50/60 Hz transformer is replaced with a smaller, high frequency, multi-winding transformer plus many additional electronic components for controlling the switching action and providing stability and accuracy to the control circuitry. Although the cost of the transformer is greatly reduced, the additional electronic components have a similar cost compared to the traditional 50/60 Hz transformer. The real advantage is therefore size and weight reduction.

There is a trade off between the isolation transformer size and weight reduction advantages and the greater complexity of the control and support circuitry. The additional electronic components utilize the automated printed circuit board assembly process, which has perceived reliability and quality advantages over the hand assembled, hand soldered traditional CTs and VTs. The greater complexity of the control and support circuitry necessitates a greater attention be given to the design and analysis details of the circuitry as well as the isolation transformer to achieve high accuracy of the sampled data.

1.2 Thesis Scope and Content

The purpose of this thesis is to 1) introduce the Isolated Analog Selector circuit used in the new transformer isolated analog acquisition system; 2) describe the overall design concept of the Isolated Analog Selector used in the analog acquisition system of a typical digital protective relay; 3) analyze the accuracy of the Isolated Analog Selector circuit and 4) present the test results of a prototype Isolated Analog Selector circuit incorporated into an existing digital protective relay product.

An important performance goal of the new transformer isolated analog acquisition system is to achieve a ±0.1% ±60 ppm/°C (parts per million per degrees Celsius) accuracy for the VT and CT analog signals being measured. This thesis concentrates on the accuracy analysis of the Isolated Analog Selector, specifically: 1) the stability, settling, and accuracy of the electronic control circuitry used, and 2) the magnetic coupling accuracy of the isolation transformer. The accuracy of the remaining components (signaling resistors, LPF, analog multiplexer, A-D conversion, etc.) are not addressed in this thesis.

Some design details of the new transformer isolated analog acquisition system are not given in this thesis (including input transient protection, signaling resistor requirements, LPF, analog multiplexer, A-D converter). These design details are all aspects of existing digital protective relay products and are not key to the novelty of this new transformer isolated analog acquisition.

There are a few blocks, within the Isolated Analog Selector circuitry itself, where design details are also not provided (including the isolated power supply and triggering or timing circuitry). Although these are important blocks with specific requirements, the design details do not influence the accuracy of the acquired analog data. Therefore, these blocks are only briefly discussed and are assumed to be functioning as required.

The thesis is divided into the following chapters:

Chapter 1: Introduction. The remainder of this chapter provides a concept overview of the control circuitry and multi-winding isolation transformer design (Isolated Analog Selector circuit) for the new transformer isolated data acquisition system.

Chapter 2: Isolated Analog Selector Circuit Design Highlights. Highlights of the Isolated Analog Selector circuit design are provided. An overall block diagram is described and the modes of operation of the new acquisition system are presented.

Chapter 3: Isolation Transformer Construction Details. Details for the isolation transformer construction used in the Isolated Analog Selector circuit are provided.

Chapter 4: Isolation Transformer SPICE Modeling. A SPICE (Simulation Program with Integrated Circuit Emphasis) model is developed for the E-E ferrite core, printed circuit board winding transformer used in the Isolated Analog Selector circuit. SPICE models for the part-to-part and temperature extreme variations identify the design constraints of the isolation transformer.

Chapter 5: Compensation Operational Amplifier Circuit Performance. SPICE models of the electronic control circuitry used in the Isolated Analog Selector help identify, measure, and improve the stability and accuracy of the design.

Chapter 6: Isolation Transformer Magnetic Coupling Accuracy. An FEA (Finite Element Analysis) tool is used to determine the accuracy of the isolation transformer of the Isolated Analog Selector. The FEA tool assists in improving the isolation transformer's coupling accuracy by identifying the optimum placement of traces for the printed circuit board windings.

Chapter 7: Prototype Testing and Results. The test results of a prototype Isolated Analog Selector circuit incorporated into an existing digital protective relay product are presented.

Chapter 8: Conclusions

1.3 Isolated Analog Selector Circuit Overview

The new transformer isolated data acquisition system employs an Isolated Analog Selector circuit for each analog input channel. The purpose of the Isolated Analog Selector circuit is to produce a high accuracy voltage output signal for the corresponding analog input channel, through an isolation transformer, for the portion of time needed for proper A-D conversion.

1.3.1 *Concept*

A traditional digital protective relay may have six VT (voltage transformer) and six CT (current transformer) analog input channels that are sampled at 8000 samples/second using a single A-D converter [2]. A block diagram of the acquisition system for this digital protective relay is shown in Figure 1-1.

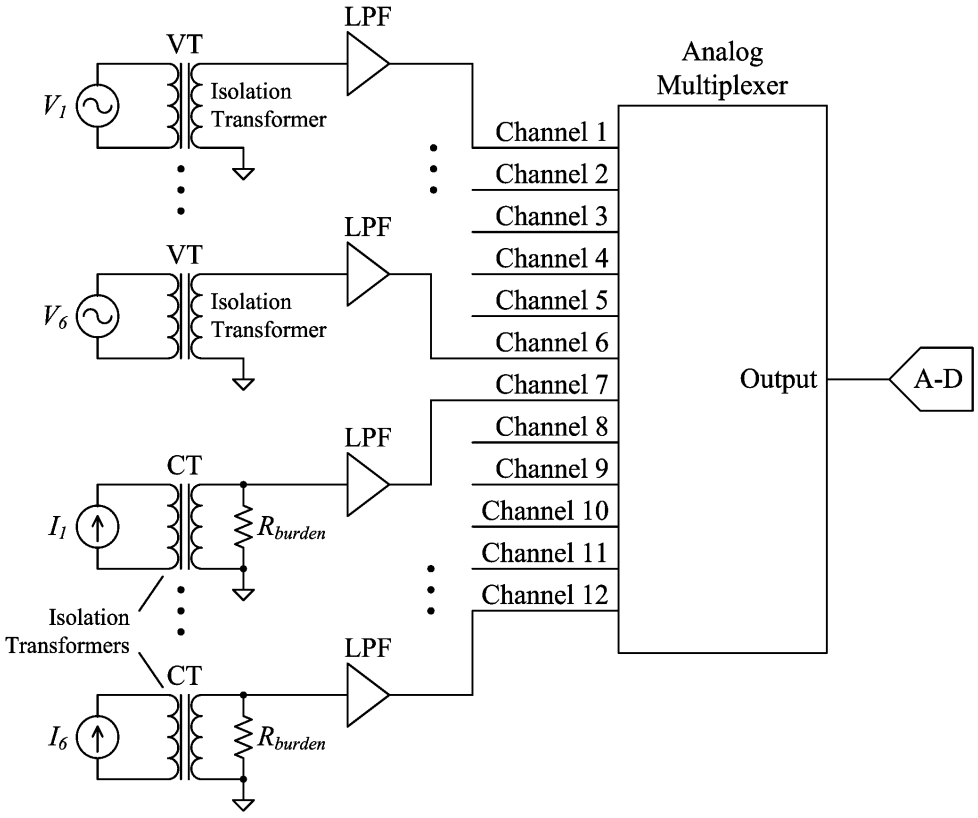

Figure 1-1: Block diagram of a traditional acquisition system for a digital protective relay with six VT and six CT channels.

The VTs of Figure 1-1, in addition to providing 2.5 kV isolation, also step down the voltage to a level that is within the range of the A-D converter. The magnetic flux density, *B*, of the VT core is related to the integral of the voltage waveform, *V(t)*, applied to the VT [3]:

$$B(t) = \frac{1}{NA_e}\int V(t)dt\,, \tag{1-1}$$

where N is the number of turns and A_e is the effective cross sectional area of the core.

To avoid transformer core saturation (i.e. extreme non-linear behavior), the magnetic flux density must stay below the magnetic flux density saturation level, B_{sat}. From (1-1), transformer core saturation occurs, for a positive voltage waveform, when the volt-time product (i.e. integration of the voltage waveform) reaches $B_{sat}NA_e$. Therefore the

transformer must be designed (i.e. have a magnetic flux density saturation, B_{sat}, effective cross sectional core area, A_e, and number of turns, N) to support the applied volt-time product. For example, if the range of the A-D converter is ±3 Vdc, then a symmetrical, full scale, 50 Hz voltage signal requires the transformer to support approximately ±9 V·ms (integration of the 3 V_p waveform).

The CTs of Figure 1-1, in addition to providing 2.5 kV isolation, step down the current to a level such that the voltage across the burden resistor, R_{burden}, (due to the output current of the CT) is within the range of the A-D converter.

Since the A-D converter is sampling at 8000 samples/second, the acquisition system is capable of measuring harmonics of the 50 or 60 Hz signals up to the 16th harmonic. The lower harmonics are important for some digital protective relay algorithms and harmonics up to the 16th can be used to infer power quality of the VT and CT signals.

The anti-aliasing LPFs (Low Pass Filters) are necessary to remove high frequency components and prevent them from aliasing to the low-pass band [4]. For the sampling rate of 8 kHz, the low-pass band should be less than the folding frequency of 4 kHz (1/2 the sampling frequency). A 2nd order LPF with a corner frequency around 2 kHz does a good job of passing the 16th harmonic while attenuating any frequency above 4 kHz that may fold back by at least 20 dB.

The A-D converter, completing a conversion approximately every 5.5 µs, sequentially samples the 12 channels at a sampling rate of 8 kHz (i.e. each channel is sampled every 125 µs). The A-D converter only has 'access to' any given channel's analog signal for 5.5 µs every 125 µs.

As an illustrative example, a full scale 60 Hz ac voltage signal is applied to V_1. If the signals from the other channels are ignored, or blanked out, the voltage signal at the output of the analog multiplexer (connected to the A-D converter) is portrayed in Figure 1-2. During the remainder of the 125 μs interval (depicted in the expanded oval of Figure 1-2), the A-D converter is sampling Channel 2 through Channel 12, monitoring other analog quantities, and idle for the remainder of time.

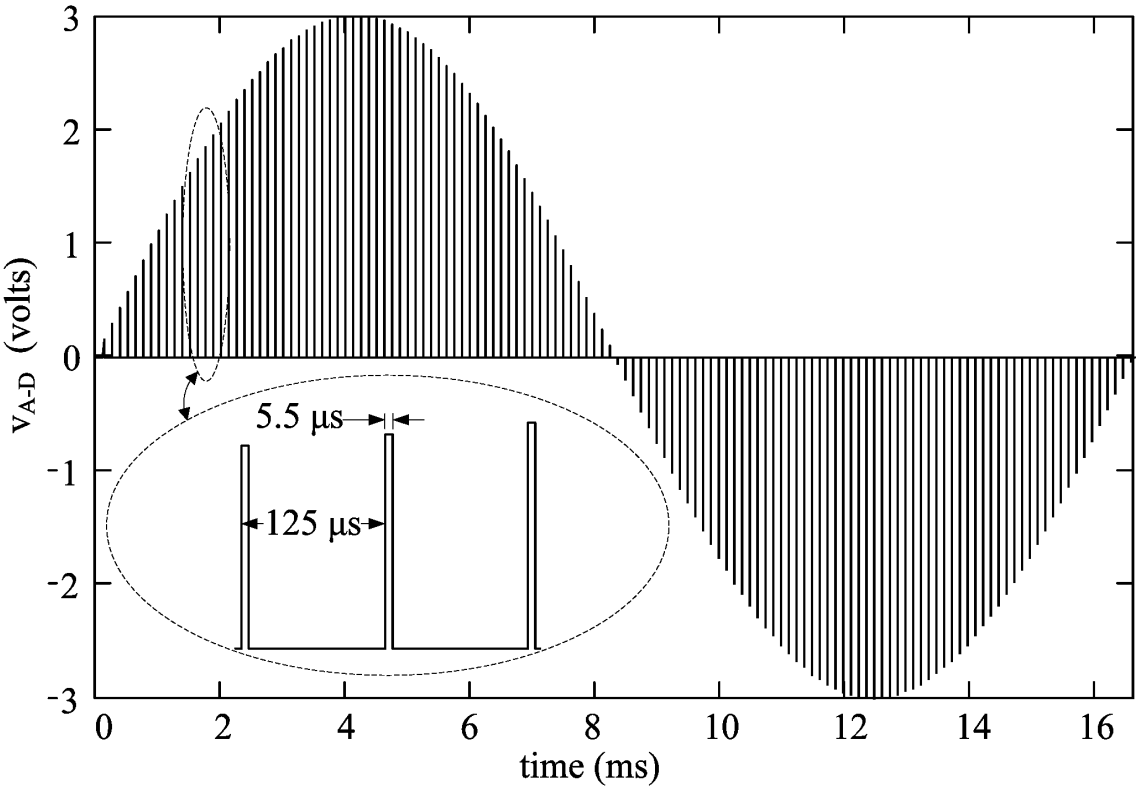

Figure 1-2: Voltage signal at the A-D converter, with a 60 Hz ac voltage signal on Channel 1 and the signals from the other channels blanked out.

Since the A-D converter only utilizes Channel 1's signal for 5.5 µs every 125 µs, there is no system requirement to bring the entire 60 Hz signal across the isolation barrier. It is this reduced requirement that drives the design of the new transformer isolated analog acquisition system.

If the isolated voltage signal is applied only for the portion of time needed for proper A-D conversion, then the volt-time requirement of the isolation transformer can be greatly reduced. For example, if the A-D converter (with the ± 3 Vdc range mentioned earlier) has a conversion time of around 2.5 µs (plus another 8 µs for the signal to settle before A-D conversion begins), then the volt-time requirement of the isolation transformer can be reduced to around 31 V·µs (i.e. nearly 1/300 of the volt-time is needed).

Conceptually, the anti-aliasing LPF is moved to the other side of the isolation barrier and the isolation transformer is only driven at the appropriate time for proper A-D conversion of the channel. A concept block diagram of this new transformer isolated data acquisition system is shown in Figure 1-3. Two basic building blocks of the 'Isolated Analog Selector' circuit are the analog switch and isolation transformer as shown in Figure 1-3.

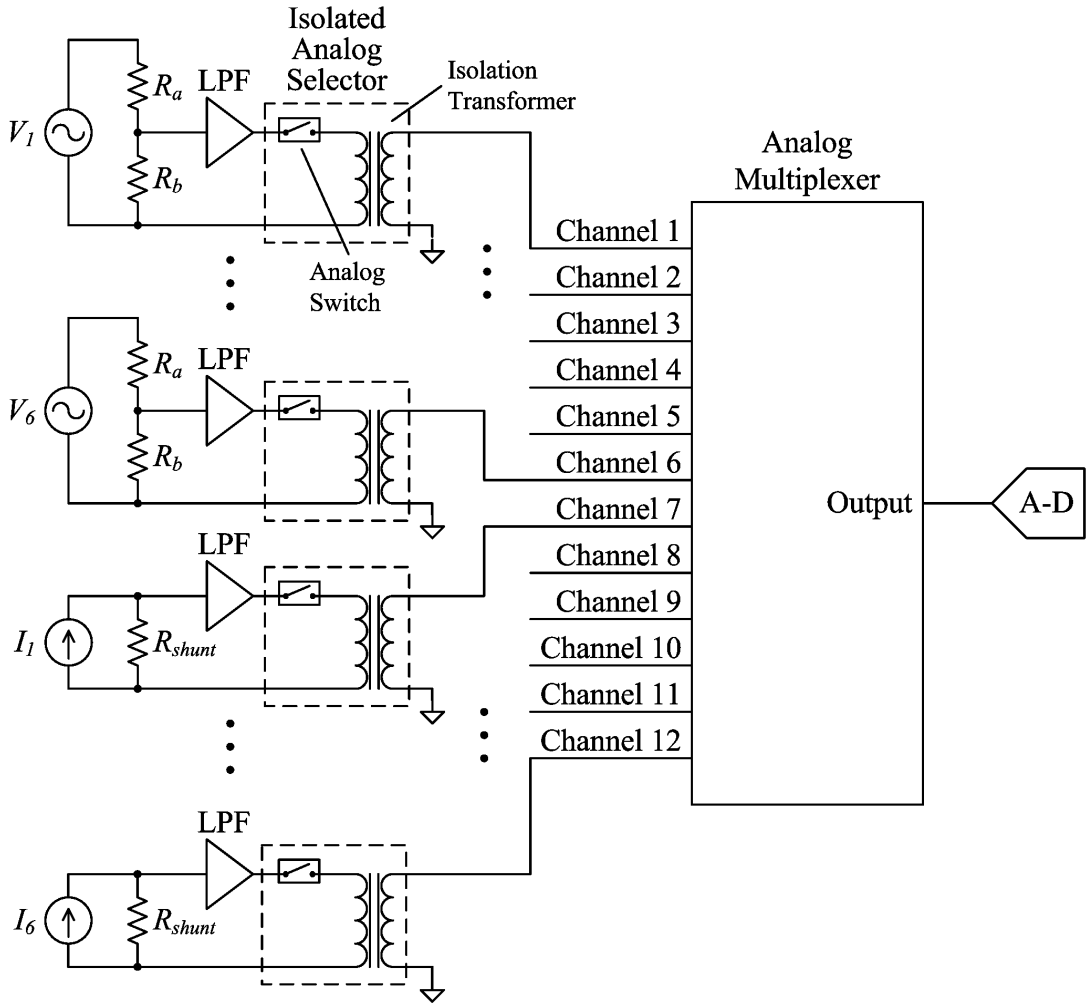

Figure 1-3: Concept block diagram of a new transformer isolated data acquisition system.

A resistor divider, R_a and R_b, divides down the voltage to a level within the range of the A-D converter for the voltage channel inputs shown in Figure 1-3. A shunt resistor, R_{shunt}, converts the input current to a voltage level also within the range of the A-D converter for the current channel inputs shown in Figure 1-3.

The analog switch, in a given Isolated Analog Selector, closes approximately 5 µs prior to the corresponding channel being selected by the analog multiplexer, allowing the switching transients to settle before the signal is multiplexed to the A-D converter. Once the A-D conversion is complete, the analog switch then opens. The result is that the

channel analog signal presented to the A-D converter (depicted in Figure 1-2 for Channel 1) are essentially the same for this new transformer isolated data acquisition system (shown in Figure 1-3) compared to a traditional acquisition system (shown in Figure 1-1).

The opportunity to reduce the isolation transformer's core size is also recognized in the frequency domain. The turning on and off of the analog switch, in the Isolated Analog Selector of Figure 1-3, in effect multiplies the LPF output voltage signal by a unity amplitude square wave pulse train (pulse width, τ = 10.5 μs) with a period of T = 125 μs. The spectral content of this pulse train is the well known $\sin(\pi f\tau)/\pi f\tau$ envelope, with zero crossings at multiples of $1/\tau$, and discrete spectral content at multiples of 1/T = 8 kHz [5]. Due to the on and off action of the analog switch, the spectral content of the LPF output signal is convolved with the spectral content of the on/off analog switch action [6].

The actual spectral content that the isolation transformer is subjected to must also include the voltage signal that occurs after the analog switch is opened. Any energy in the core causes the transformer winding voltage to reverse polarity (i.e. flyback) when the analog switch opens. The flyback voltage is clamped to a supply rail until the core energy is depleted (i.e. the core is reset). Further details of the core reset are provided later in Chapter 2. Therefore, the on/off action that the transformer is subjected to can be approximated by the unity amplitude square wave pulse (mentioned above) followed by a negative unity amplitude pulse of the same width.

The approximated spectral content of the transformer on/off switching action (positive pulse followed by a negative pulse) convolved with the spectral content of a typical LPF output voltage signal, V_{LPF} (60 Hz system), is shown in Figure 1-4 (normalized to the rms fundamental of V_{LPF}).

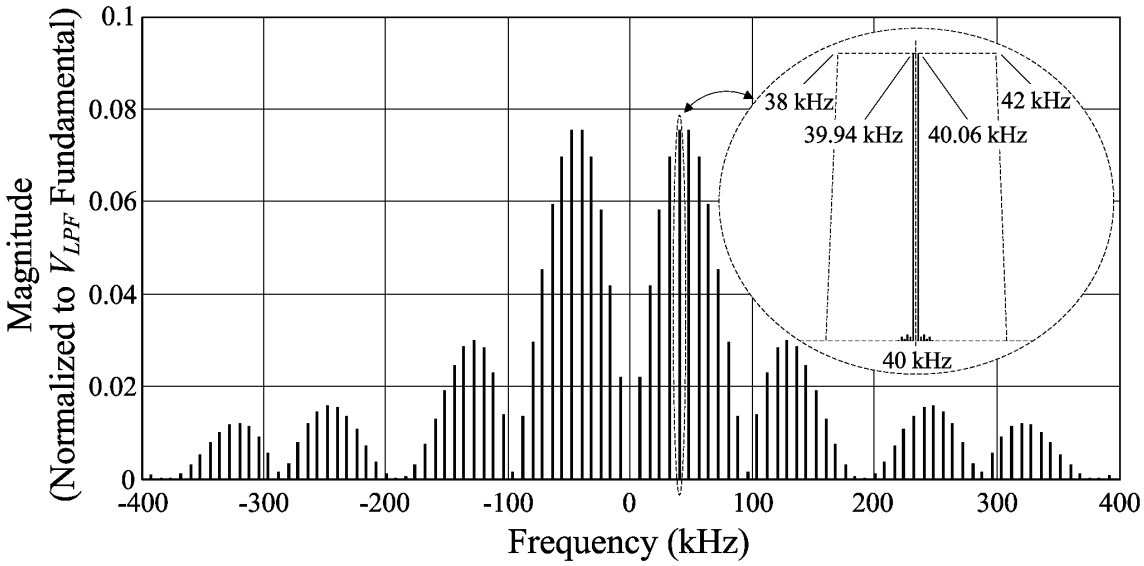

Figure 1-4: Approximated spectral content of the transformer on/off switching action convolved with the spectral content of a typical LPF output voltage signal, V_{LPF} (normalized to the rms fundamental of V_{LPF}).

Due to convolution in the frequency domain, the spectral content of the typical LPF output voltage signal is present at each multiple of 8 kHz as depicted in the expanded oval of Figure 1-4. The dashed trapezoid in the expanded oval shows the pass band characteristic of the LPF with corner frequency around 2 kHz (roll off purposely exaggerated).

As shown in Figure 1-4, there is no dc content to the isolation transformer's voltage spectrum. The lowest frequency content is at 6 kHz. The on/off action of the analog switch converts the voltage spectrum that was at 50 or 60 Hz (plus any harmonics present through the 16th harmonic) to a voltage spectrum that is spread out above 6 kHz. Similar to switched mode power supplies, the isolation transformer only needs to support the higher frequencies and therefore can be reduced in size.

The new transformer isolated acquisition system significantly reduces the volt-time requirement of the isolation transformer (from 9 V·ms to 31 V·µs for the voltage channel

input). The reduced volt-time product can easily be supported with a small E-E ferrite core. This has the advantage of significantly shrinking the size and weight of a digital protective relay that has 12 transformers. However, with the reduced core size comes a similar reduction in the magnetizing inductance. The challenges of the diminished magnetizing inductance are addressed next.

1.3.2 *Design Challenges and Design Progression*

As with any transformer design, the effect of the magnetizing inductance, L_m, introduces an error in the transformed voltage signal (i.e. the secondary voltage does not exactly match the expected ratio of the primary voltage). This error is predominantly a result of the magnetizing current flowing through the primary winding resistance and primary leakage inductance [7].

A first approximation circuit model for the isolation transformer of Figure 1-3 is shown in Figure 1-5 (ignoring the primary leakage inductance).

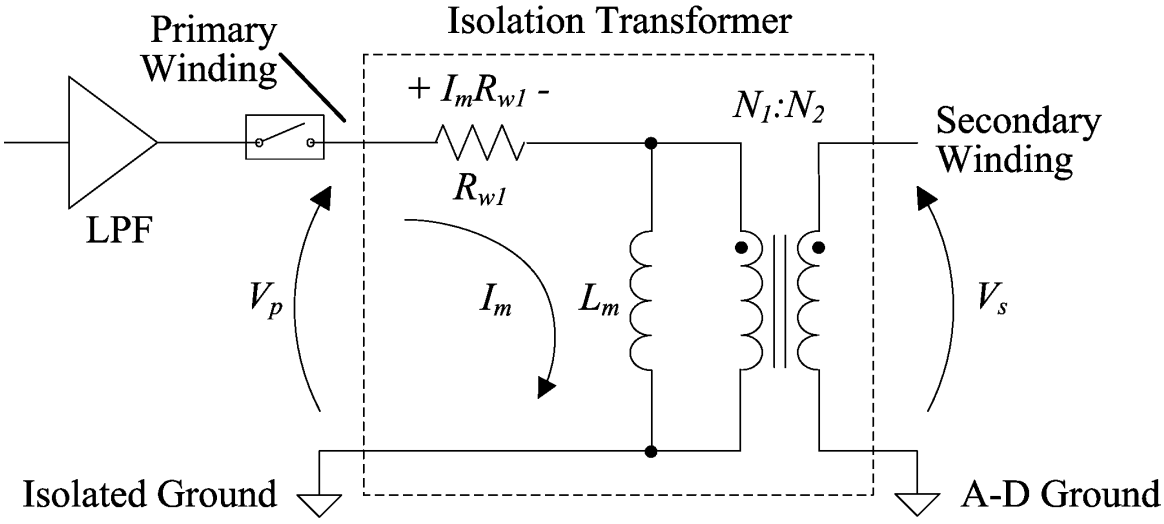

Figure 1-5: First approximation circuit model for the isolation transformer.

If at time, t = 0, the analog switch closes and a dc voltage, V_p, is applied to the primary winding of the isolation transformer, the magnetizing current, I_m (initially 0 A), rises and settles in an exponential fashion to a final value of V_p/R_{w1}:

$$I_m(t) = \frac{V_p}{R_{w1}}\left(1 - e^{-tR_{w1}/L_m}\right). \qquad (1\text{-}2)$$

When the analog switch first closes, the current can be linearly approximated with a ramp (as long as the input voltage, V_p, remains constant):

$$I_m(t) \cong \frac{V_p t}{L_m} \qquad (t << L_m/R_{w1}). \qquad (1\text{-}3)$$

From (1-3), smaller cores (i.e. smaller magnetizing inductance, L_m), result in the magnetizing current, I_m, ramping up quicker when a dc primary voltage is first applied. This ramping magnetizing current will produce a ramping voltage drop across the winding resistance, R_{w1} (as shown in Figure 1-5), and causes the secondary voltage to droop (in error):

$$V_s(t) = \left(V_p - I_m(t)R_{w1}\right)\frac{N_2}{N_1}. \qquad (1\text{-}4)$$

The error of (1-4) increases as time progresses. For the reduced size, E-E ferrite core (used in the isolation transformer of the Isolated Analog Selector) the typical magnetizing inductance, L_m, is around 250 μH and the resistance of the printed circuit board trace primary winding is around 1.3 Ω. After 10 μs, this gives an error in the secondary voltage of nearly 5 %. This is too much error since the overall required accuracy of the analog

acquisition system is ±0.1 %. Since the inductance of the E-E ferrite core is non-linear, a simple gain adjustment/calibration is ineffective.

Orders of magnitude reduction in the error due to the magnetizing current is achieved by adding a compensating operational amplifier circuit. A third, sense winding is also added to the transformer to provide feedback to the compensation operational amplifier as shown in the Isolated Analog Selector circuit concept block diagram of Figure 1-6.

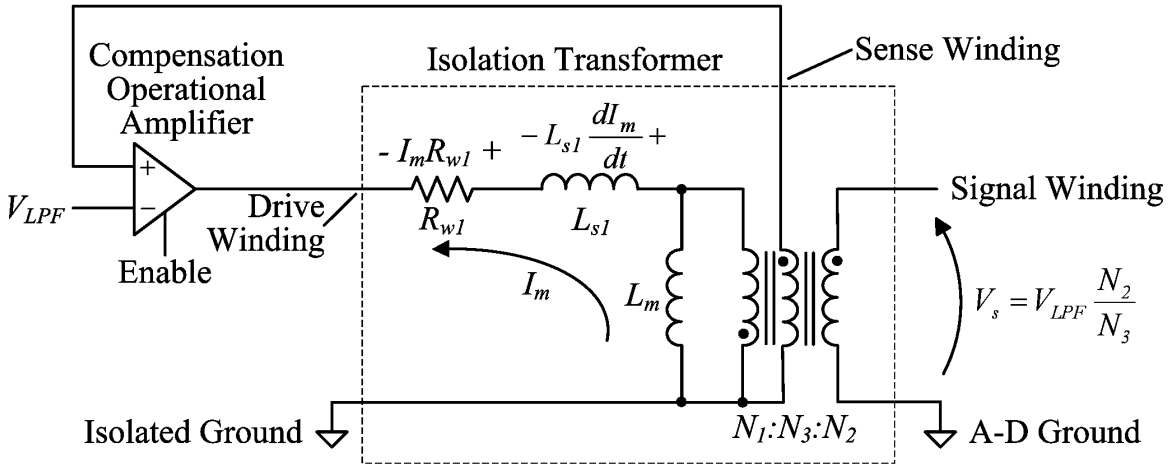

Figure 1-6: Isolated Analog Selector circuit concept block diagram.

The compensation operational amplifier has an output enable feature (similar role as the analog switch of Figure 1-5). When the compensation operational amplifier is enabled, the output drives the drive winding. The sense winding provides feedback to the compensation operational amplifier. Even though the sense winding is connected to the positive input terminal of the compensation operational amplifier, it is negative feedback since the drive winding has an opposite polarity with respect to the sense winding.

With this compensation operational amplifier circuit, the voltage drops of the primary winding resistance, R_{w1}, and leakage inductance, L_{s1}, do not result in an error at the secondary voltage, V_s. If a positive dc voltage is at V_{LPF} when the compensation

operational amplifier is enabled, the output of the compensation operational amplifier will adjust negative and continue to ramp down in order to maintain the sense winding voltage (at the positive terminal of the operational amplifier) at a nearly equivalent level to V_{LPF} (at the negative terminal of the operational amplifier).

To a first approximation, the output voltage on the signal winding, V_s, is equal to the LPF voltage, V_{LPF}, adjusted by the turns ratio N_3:N_2. This, of course, assumes that there is no load on the secondary of the isolation transformer and that the operational amplifier is ideal. In reality there is some secondary output loading and the operational amplifier has some finite gain and some input impedance and other non-ideal characteristics.

The compensation operational amplifier is a key component to the Isolated Analog Selector control system, shown in the block diagram of Figure 1-6. The control system circuitry must be designed with adequate stability, loop gain, and settling characteristics in order to achieve high accuracy.

Additionally, the LPF, compensation operational amplifier, and other active circuitry on the primary side of the Isolated Analog Selector (i.e. left side of the isolation transformer of Figure 1-6) need power supply rails. These power supply rails must be isolated from the secondary side (i.e. isolated from the right side or signal winding of the isolation transformer of Figure 1-6). Therefore, the Isolated Analog Selector circuit must also contain an isolated power supply.

Finally, the compensation operation amplifier must be enabled for an adequate amount of time (for signal settling and proper A-D conversion) at the right time (just prior to the A-D conversion of the corresponding channel). The controlling of the enable for the compensation operational amplifier must originate from the signal winding side,

and therefore must cross the isolation barrier (2.5 kV isolation required between isolated ground and A-D ground of Figure 1-6).

The details of the compensation operational amplifier circuit (stability, settling and accuracy) are given in Chapter 5. The next chapter gives some highlights of the Isolated Analog Selector circuit design.

Chapter 2 Isolated Analog Selector Circuit Design Highlights

Other circuit components (not shown in Figure 1-6) are required around the compensation operational amplifier for stability and improved accuracy. When the Isolated Analog Selector circuit is not driving the voltage signal across the isolation barrier (i.e. the compensation operational amplifier of Figure 1-6 is not enabled), the isolation transformer is further utilized for:

1. A forward converter switched mode power supply to generate isolated power rails for the LPF and compensation operational amplifier circuitry. The forward converter is driven by FETs connected to the signal winding.
2. Transferring a trigger signal across the isolation barrier that enables the compensation operational amplifier of Figure 1-6 at the appropriate time for proper A-D conversion. The trigger signal is generated by the same FETs used for the forward converter switched mode power supply.

A block diagram for the Isolated Analog Selector circuit is shown in Figure 2-1. The output of the LPF, V_{LPF}, is the input to the Isolated Analog Selector (left/primary side of Figure 2-1) and is referenced to isolated ground. The output of the Isolated Analog Selector (right/secondary side of Figure 2-1) connects to the analog multiplexer and is referenced to A-D ground. The circuit block diagram of Figure 2-1 shows the details of the Isolated Analog Selector blocks of Figure 1-3.

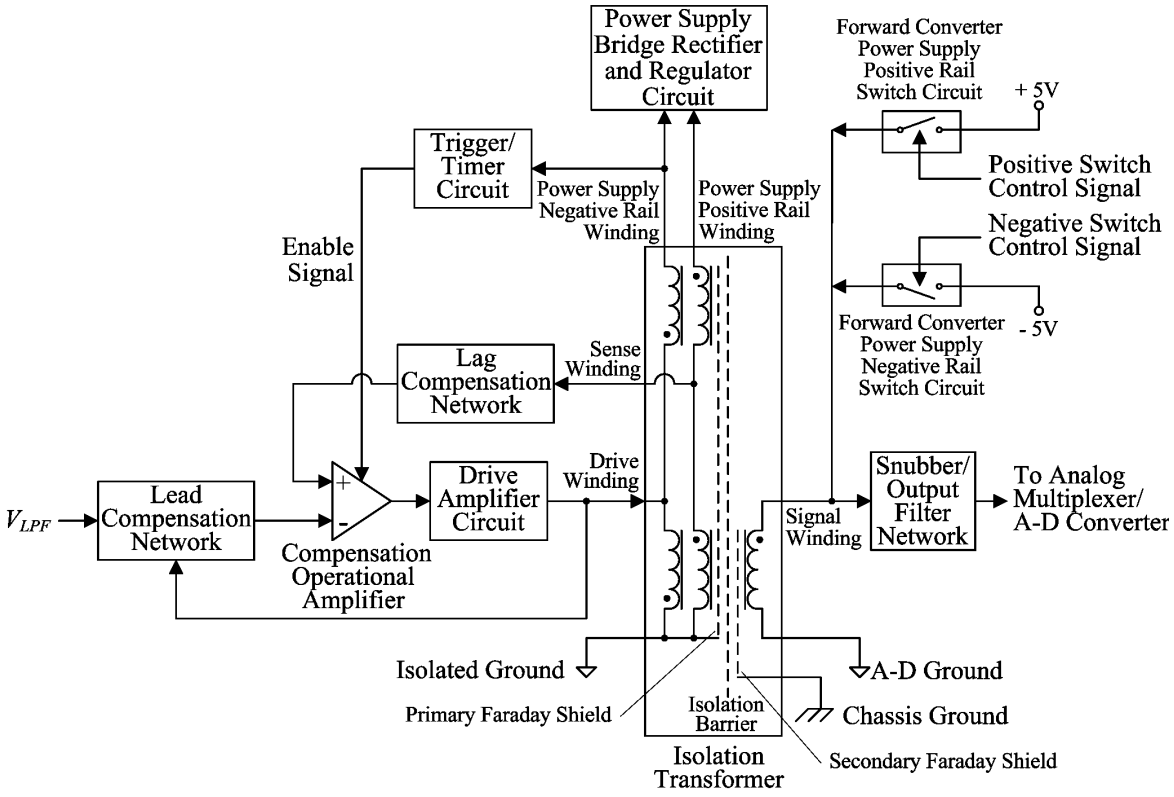

Figure 2-1: Isolated Analog Selector circuit block diagram.

The lead compensation network, lag compensation network, drive amplifier circuit, and snubber/output filter network blocks of Figure 2-1 are all necessary for the stability and accuracy of driving the signal across the isolation barrier when the compensation operational amplifier is enabled. The details of these blocks are given in Chapter 5.

The isolation transformer consists of an E-E ferrite core with printed circuit board traces for the drive, sense, signal, and power supply windings. The primary and secondary Faraday shields along with the construction details of the isolated transformer are given in Chapter 3.

The forward converter power supply positive rail and negative rail switch circuits in the upper right of Figure 2-1 contain FETs that are used for a forward converter/push-pull switched mode power supply. When the compensation operational amplifier is disabled,

the FETs alternately drive the signal winding (between + 5 Vdc and – 5 Vdc) producing alternating feed forward voltages across the isolation barrier on the power supply positive and negative rail windings. These power supply windings provide energy to the power supply bridge rectifier and regulator circuit block of Figure 2-1 which produces the isolated power supply rails for the LPF, compensation operational amplifier, drive amplifier circuit, and trigger/timer circuit.

The FETs in the forward converter power supply positive rail and negative rail switch circuits are also used to send a trigger signal across the isolation barrier to the trigger/timer circuit block of Figure 2-1. When the trigger/timer circuit block detects the trigger signal, it pulses the enable signal for approximately 12 μs. This gives ample time to allow the compensation operational amplifier and drive amplifier circuit to drive the drive winding and have the signal winding settle before and during A-D conversion.

A timing diagram of the four modes of the Isolated Analog Selector circuit (for Channel 1) is given in Figure 2-2. The positive and negative switch control signals are used to control these four modes and originate from the digital controller/processor controlling the analog acquisition system.

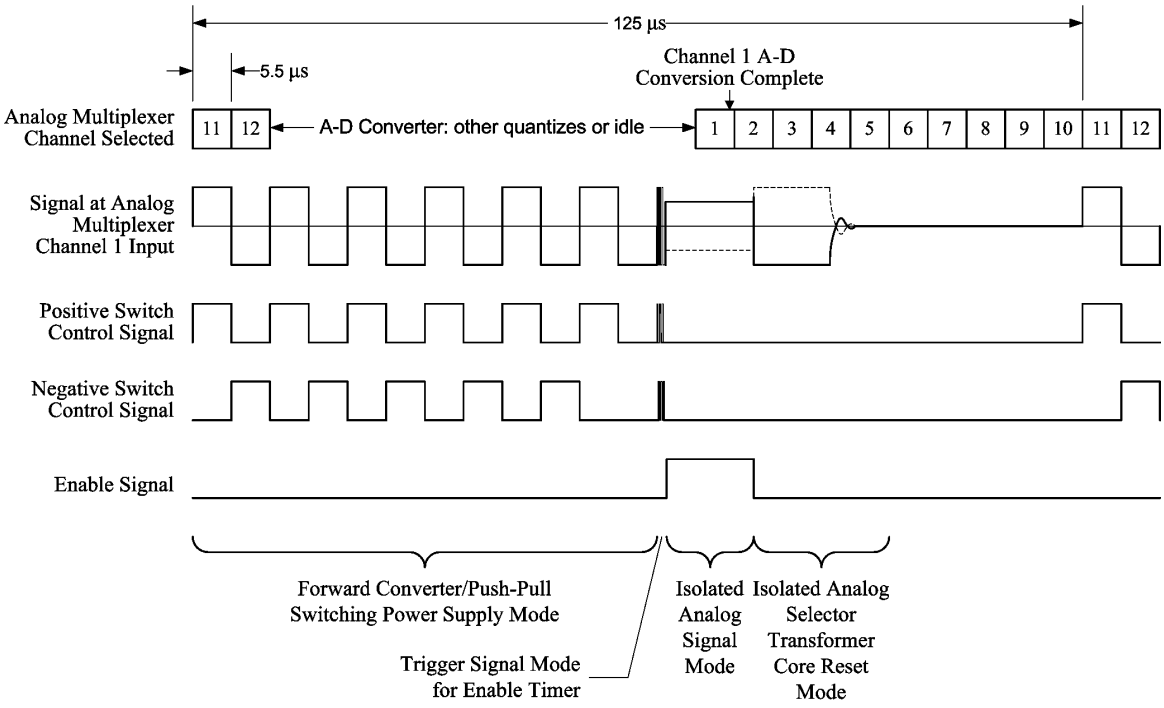

Figure 2-2: Isolated Analog Selector Channel 1 Timing Diagram.

The first operation mode shown in Figure 2-2 is the forward converter/push-pull switching power supply mode. During this mode (for Channel 1), the A-D converter happens to be sampling Channels 11 and 12 as well as other analog quantities and then remains idle. In this operation mode, the positive and negative FETs (switches in the upper right of Figure 2-1) are alternately switched back and forth to drive the push/pull forward converter switched mode power supply. During the first mode of operation, energy is fed into the power supply bridge rectifier and regulator circuit block of Figure 2-1. This energy is used to provide the isolated power supply rails for the LPF, compensation operational amplifier, drive amplifier circuit, and trigger/timer circuit of Figure 2-1.

When the positive switch control signal (of Figure 2-2) is high (for around 5.5 µs), the forward converter power supply positive rail switch (of Figure 2-1) turns on and +5

Vdc is applied to the signal winding, producing a positive voltage on the power supply positive rail winding and a negative voltage on the power supply negative rail winding of Figure 2-1. Likewise, when the negative switch control signal is high (for around 5.5 µs), the forward converter power supply negative rail switch turns on and –5 Vdc is applied to the signal winding, producing a negative voltage on the power supply positive rail winding and a positive voltage on the power supply negative rail winding of Figure 2-1.

Storage capacitors in the power supply bridge rectifier and regulator circuit block (of Figure 2-1) maintain the isolated power supply rails during the remaining modes of operation.

The second mode of operation, trigger signal mode for enable timer (shown in Figure 2-2), occurs approximately 5.5 µs prior to Channel 1 being selected by the analog multiplexer. During this mode, the positive switch control signal and negative switch control signal are rapidly turned on and off (125 ns pulses) alternately for three times as shown in Figure 2-3.

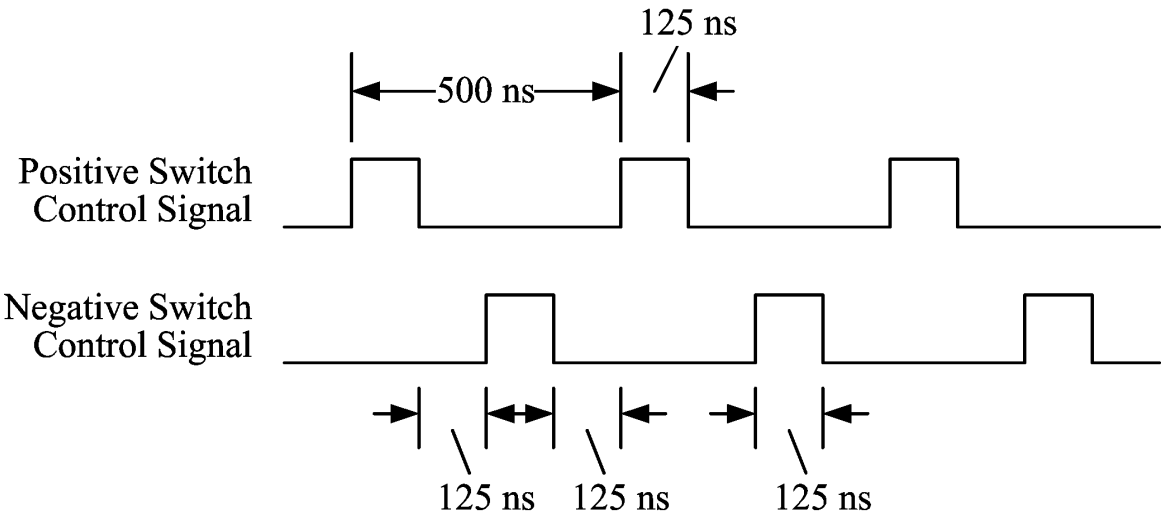

Figure 2-3: Trigger signal timing diagram.

The trigger/timer circuit of Figure 2-1 detects this rapid pulse action of the power supply negative rail winding and activates a timer (for approximately 12 μs) that is used to generate the compensation operational amplifier enable signal shown in Figure 2-1 and Figure 2-2.

When the enable signal is high, the Isolated Analog Selector circuit is in the third mode of operation (isolated analog signal mode as shown in Figure 2-2). The compensation operational amplifier output (of Figure 2-1) is activated by the high level of the enable signal in this operation mode, as shown in Figure 2-2. The compensation operational amplifier adjusts its output level until the signal at the sense winding (of Figure 2-1) matches the input voltage signal from the LPF (input to the Isolated Analog Selector circuit).

Once the circuitry has settled, the output voltage signal presented to the analog multiplexer/A-D converter (output of the Isolated Analog Selector circuit) is a proportionately accurate representation of the LPF signal across the isolation barrier. As shown in Figure 2-2, the enable signal is high well before the analog multiplexer Channel 1 is selected. The A-D conversion of Channel 1 is complete near the end of the selection period for Channel 1 as shown in the top of Figure 2-2.

The solid signal trace at the analog multiplexer Channel 1 input shown in Figure 2-2 during the isolated analog signal mode represents a full-scale positive voltage from the LPF output. When the enable signal transitions low, any energy that is in the core causes the voltage signal to flyback to the negative rail. The dashed signal trace represents a full-scale negative voltage from the LPF output. Energy that is in the core, when the enable signal transitions low, causes the voltage signal to flyback to the positive rail.

The fourth and final operation mode of Figure 2-2, is the Isolated Analog Selector transformer core reset mode, shown occurring from the middle of analog multiplexer Channel 2 selection through the end of Channel 5 selection. During this time, there is no circuitry actively driving the transformer and any energy that is trapped/stored in the isolation transformer's core dumps into the power supply bridge rectifier and regulator circuit of Figure 2-1. When the core energy is depleted, the voltage signal at the analog multiplexer Channel 1 input will ring and dampen to 0 V.

The four modes are repeated every 125 µs as shown in Figure 2-2. There are 11 other similar timing diagrams for the remaining 11 channels. The point at which the corresponding enable signal is high, lines up with the appropriate analog multiplexer channel selection (i.e. Channel 2's positive and negative switch control signals are shifted to the right approximately 5.5 µs, etc.).

The compensation operational amplifier, feedback sense winding, and supporting control circuitry play a key role in achieving an accurate representation of the LPF output voltage signal across the isolation barrier. Another very important component is the isolation transformer.

The isolation transformer is also designed to provide 2.5 kV of isolation and to provide accurate coupling between the drive-sense and drive-signal windings, in addition to supporting the necessary volt-time product (when the compensation operation amplifier is enabled). The transformer must also have a common mode rejection ratio of at least -100 dB @ 60 Hz, referred to V_1 of Figure 1-3. When a common mode voltage is present between the isolated ground and A-D ground of Figure 2-1, the capacitive

coupling that occurs between the primary circuitry and secondary circuitry must be minimized to maximize the common mode rejection.

The next chapter addresses the construction design details of the isolation transformer. The requirements of 2.5 kV isolation, common mode rejection performance, and accurate coupling between the drive-sense and drive-signal windings dictate the design of the isolation transformer.

Chapter 3 Isolation Transformer Construction Details

A schematic of the isolation transformer is shown in Figure 3-1. The primary side windings (referenced to isolated ground) consists of the drive, sense and power supply windings. The secondary side winding (referenced to A-D ground) consists of the signal winding.

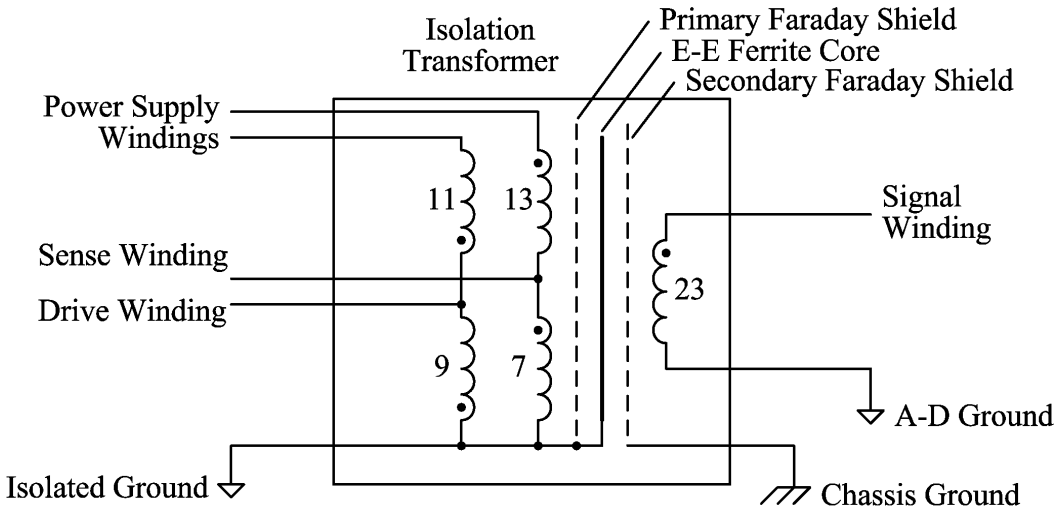

Figure 3-1: Isolation transformer schematic.

The primary and secondary Faraday shields nearly eliminate the capacitive coupling from the secondary circuit to the primary windings and from the primary circuit to the secondary winding, respectively. The A-D ground is connected to chassis ground near the A-D converter. The direct chassis ground connection of the secondary Faraday shields (for each of the 12 channels) provides a low impedance path for common mode transients without impacting the acquisition system ground.

The placement of the drive, sense, and signal windings (to achieve high accuracy coupling), is controlled by realizing the transformer windings as traces on a printed circuit board. In order to achieve the 2.5 kV isolation, the primary windings are located on a primary printed circuit board and the secondary winding is located on a secondary

printed circuit board. The two boards overlap such that the E-E core halves can be placed about the two printed circuit boards as shown in Figure 3-2.

The primary and secondary printed circuit boards have four layers. The Faraday shields are planes on the top and bottom outer layers as well as guard traces on the edge of the inner two layers. The windings are traces on the inner two layers that are routed around the center leg of the E-E ferrite core. For the cross sectional view of Figure 3-2(c), a winding turn goes into the page through the left E-E core window, around the back side of the center leg of the E-E core, out of the page through the right E-E core window, and completes the turn around the front of the center leg of the E-E core.

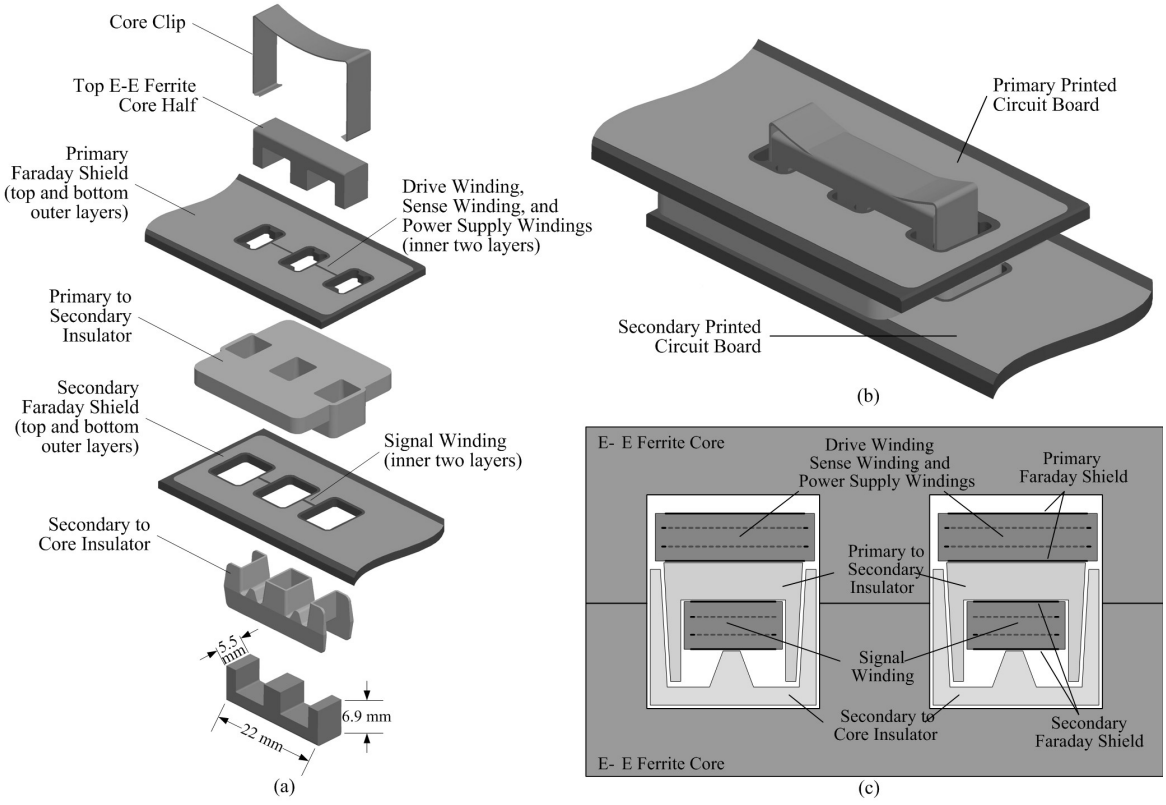

Figure 3-2: Isolation transformer construction using an E-E ferrite core and printed circuit board traces for windings: (a) expanded component view, (b) assembled view (c) cross sectional view.

Two plastic insulators provide isolation (proper creepage and clearance distance for 2.5 kV isolation) between the primary and secondary printed circuit boards and between the secondary printed circuit board and the E-E core. The E-E core halves are held together with the core clip and the E-E core is constrained from movement by the plastic insulators.

The 23 signal winding turns barely fit on the two inner layers of the secondary printed circuit board (5 mil traces with 5 mil spacing). Figure 3-3 shows 11 turns of the signal winding on one of the inner printed circuit board layers. The inside and outside of the 11 turns are surrounded by guard traces that are part of the secondary Faraday shield.

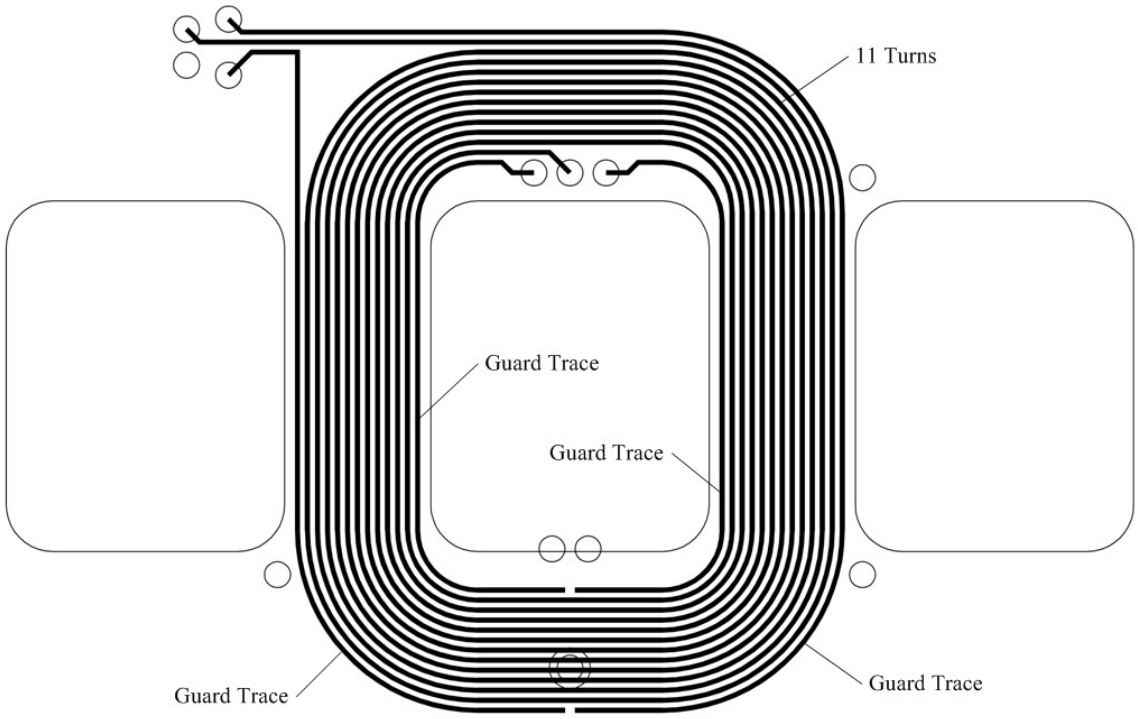

Figure 3-3: Signal winding, 11 turns on one of the inner printed circuit board layers.

The 9 drive winding turns, 7 sense winding turns and remaining 24 power supply winding turns also barely fit on the two inner layers of the primary printed circuit board, but are free to be arranged in any location.

The accuracy of the isolation transformer is a function of how well the sense winding and signal windings are magnetically coupled with respect to the drive winding. As such, the locations of the power supply windings are irrelevant to the accuracy analysis. The advantage of using printed circuit board traces as windings is that the locations of the traces are fixed. Each isolation transformer constructed will have nearly the same magnetic coupling characteristics between the windings.

Chapter 6 identifies the coupling between the drive-sense windings and drive-signal windings and optimizes the location of these windings to achieve maximum coupling accuracy.

Chapter 4 Isolation Transformer Modeling

To analyze the electronic circuit performance and the magnetic coupling error of the Isolated Analog Selector transformer it is necessary to properly model the nonlinear E-E core. Modeling the E-E core defines the design constraints of the volt-time product and the minimum inductance of the isolation transformer. The purpose of this chapter is to identify a circuit model for the isolation transformer. This circuit model is used in Chapter 5 to analyze the stability, settling, and accuracy of the compensation operational amplifier circuitry.

A SPICE model is constructed from the datasheet of the E-E core. Various SPICE models are generated for the E-E core representing the typical, minimum and maximum inductance at room temperature as well as the minimum and maximum inductance at temperature extremes (i.e. –40 °C and 100 °C).

Section 4.1 develops the SPICE model for the B-H characteristics of the core material. The SPICE core model is based on the Jiles-Atherton model [8]. Section 4.2 develops the SPICE model for the E-E core. The effective cross sectional area and the effective magnetic length of the core is specified in the SPICE model according to the E-E core's datasheet. And finally, the appropriate gap size is calculated to achieve the specified inductance of the E-E core's datasheet. A small gap always exists between the two E-E core halves. The physical gap is a function of the cutting/grinding process of the ferrite E-E core. Once the gap is calculated, it is used in the SPICE model for the E-E core and the Finite Element Analysis modeling of Chapter 6.

Section 4.3 defines the printed circuit board winding resistance used in the SPICE model for the isolation transformer. Section 4.4 defines the printed circuit board winding leakage inductance and winding capacitance used in the SPICE model for the isolation transformer. Section 4.5 presents the SPICE model for the isolation transformer used for the used to analyze the stability, settling, and accuracy of the compensation operational amplifier circuitry in Chapter 5.

4.1 Typical B-H Characteristic of the Core Material

The E-E core used for the Isolated Analog Selector transformer is a Tomita 2G1-EE-22X13.8B. The core material is a ferrite based, Mn-Zn (manganese zinc) compound. The 2G1 material has an initial relative permeability of μ_i = 7000 and a magnetic flux density saturation level of B_s = 410 mT. The typical B-H characteristic at 20 °C, from the manufacture's datasheet, is shown in Figure 4-1 (Courtesy Tomita Electric Co.) [9].

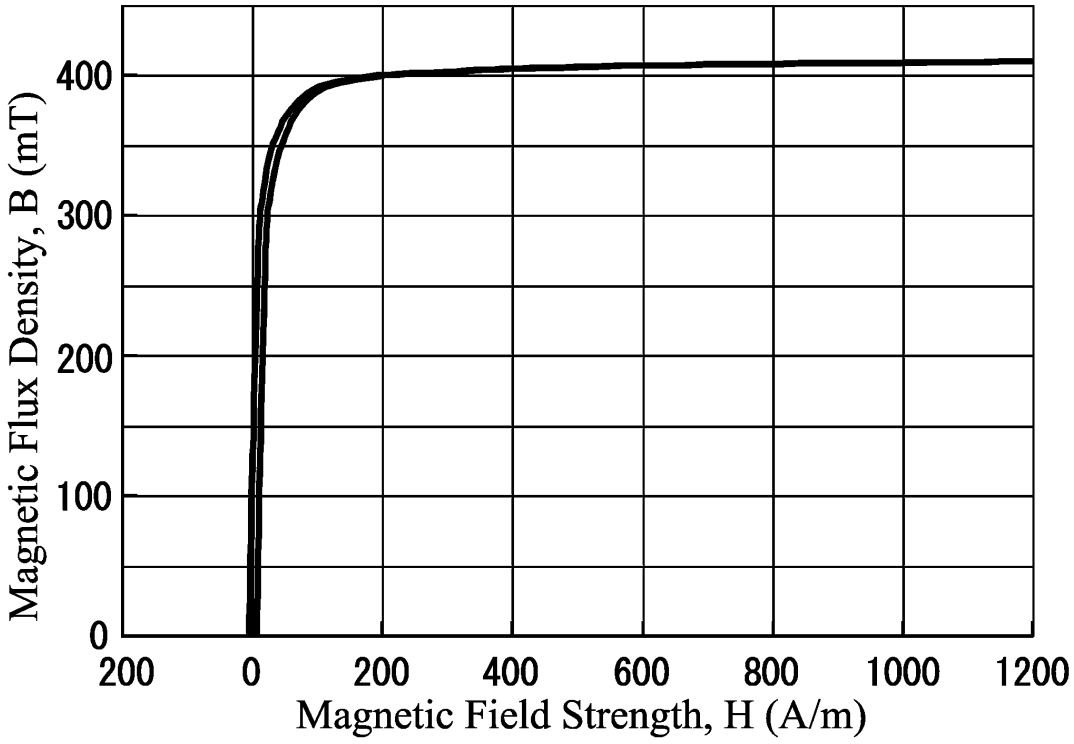

Figure 4-1: Tomita 2G1 material B-H characteristic (Courtesy Tomita Electric Co.).

The Jiles-Atherton model requires four parameters to be assigned: 1) MS (Saturation Magnetization parameter), 2) A (Thermal energy parameter), 3) K (Domain anisotropy parameter) and 4) C (Domain flexing parameter). The MS parameter is initially set to B_s/0.01257 (B_s is the saturation level in Tesla). The A parameter is initially set to 1 and then increased until the slope of the B-H curve matches the datasheet. The K parameter is initially set to 0 and then increased until the B-H loop opening matches the datasheet. And finally, the C parameter is initially set to 0.2 and then increased until the initial slope (at 10 mT) matches the initial permeability.

Assigning the proper values for the four parameters of the Jiles-Atherton model is an iterative process. The process involves setting the four parameters and then running the SPICE transient analysis to obtain a plot of the B-H characteristic. The four parameters can then be appropriately adjusted based on the observation of the differences in the SPICE and the datasheet's B-H characteristic.

The SPICE model schematic for plotting the B-H characteristic is shown in Figure 4-2. The current source, I1, starts from 0, ramps up to a positive saturation current level, ramps down to a negative saturation current level and then ramps up again to a positive saturation current level. The actual saturation current level and ramp time does not matter as long as the current level forces the core into deep saturation. The saturation current level can easily be calculated from the maximum magnetic field strength, H (A/m), of the datasheet's B-H characteristic: $I_{sat} = Hl_e/N$ (where l_e is the effective magnetic path length). For the core material of Figure 4-1, and for the N = 1 turn of Figure 4-2, I_{sat} = (1200 A/m)(3.81 cm)/1 = 46 A.

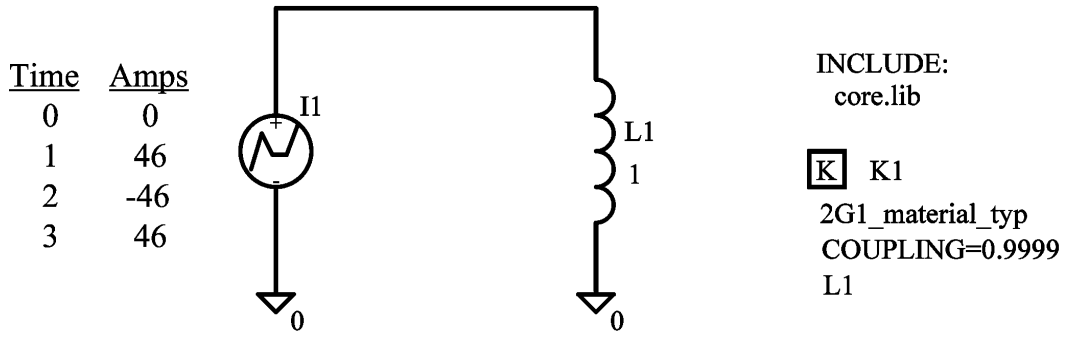

Figure 4-2: SPICE model schematic for plotting the B-H characteristic.

The B-H characteristic from SPICE for the typical core model at room temperature is shown in Figure 4-3. This closely resembles the datasheet B-H characteristic of Figure 4-1.

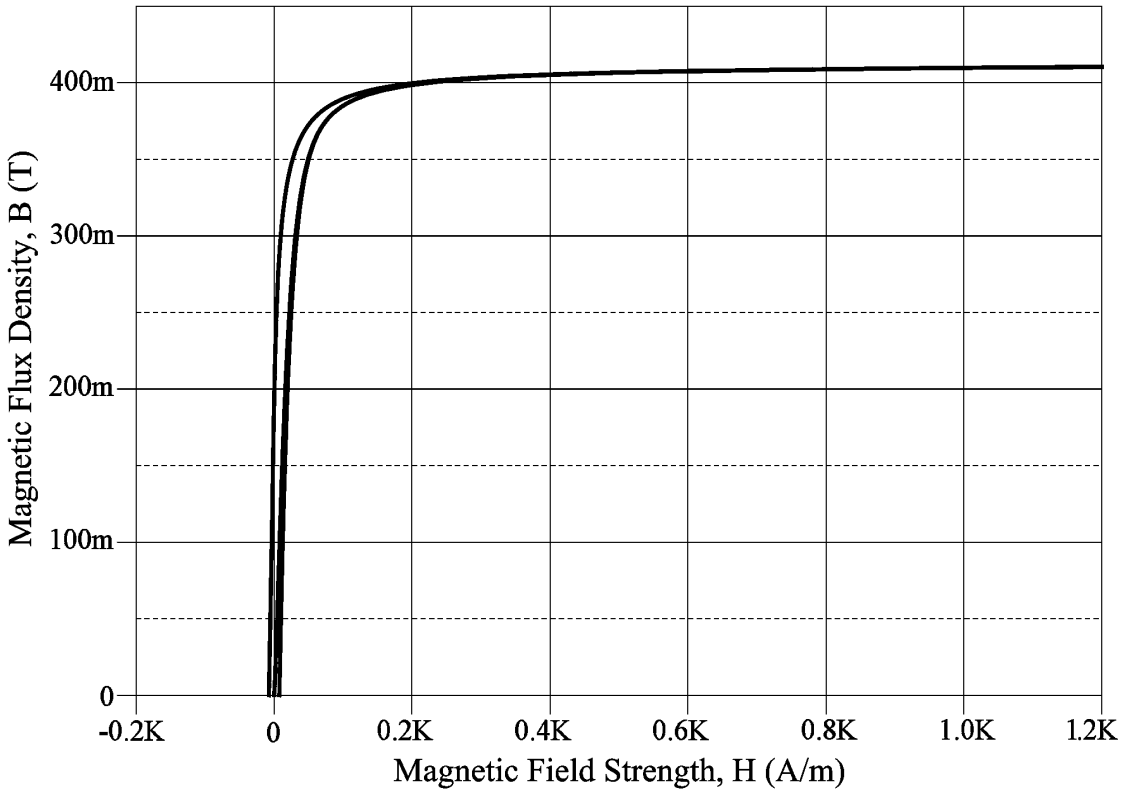

Figure 4-3: Material B-H characteristic plot from SPICE.

The B-H characteristic is a model for the nonlinear core material. This material model is only valid for one-piece, non-gapped cores (e.g. toroid). For cores with two

pieces (e.g. an E-E core), a small gap is added to the core model to account for the seam between the two halves.

4.2 Typical B-H Characteristic of the E-E Core

Once the typical core material B-H characteristic at room temperature is modeled, a small gap is included to properly model the interface between the two E-E core halves. The gap size is determined by matching the typical inductance of the datasheet (A_L = 3100 nH/N^2) with the SPICE results.

The inductance per turns squared of the datasheet, A_L, is tested at 1 mA with N = 100 turns (arbitrarily at 1 kHz). This is very close to the initial permeability level of the core material, therefore a good starting place for the gap size can be calculated by solving the equation relating the inductance, L, to the reluctance, $\mathcal{R}$: $L = N^2/\mathcal{R}$. The reluctance is the series combination of the reluctance of the core and the reluctance of the air gap. For one turn, A_L, is calculated as:

$$A_L = \frac{1}{\frac{l_e}{\mu_o \mu_i A_e} + \frac{l_{gap}}{\mu_o A_e}}. \tag{4-1}$$

The first term in the detonator of (4-1) is the reluctance of the core at initial relative permeability, μ_i, (where A_e is the effective cross section of the core) and the second term is the reluctance of the gap. Solving for l_{gap} gives:

$$l_{gap} = \frac{\mu_o A_e}{A_L} - \frac{l_e}{\mu_i}. \tag{4-2}$$

From the datasheet for the E-E core, μ_i = 7000, A_L = 3100 nH/N^2, A_e = 0.249 cm^2, and l_e = 3.81 cm, giving l_{gap} = 4.65x10^{-4} cm. The actual gap required is determined by first driving the inductor core model with a 1 mA current source at 1 kHz with N = 100 turns

and calculating the resulting inductance, A_L and then iteratively adjusting the gap until a value of A_L = 3100 nH/N^2 is achieved. The gap size required to achieve this value of A_L is l_{gap} = 4.94x10^{-4} cm.

Once the core material and gap are properly modeled, the B-H characteristic for the actual E-E core can be plotted as shown in Figure 4-4. As the current (in the SPICE model of Figure 4-2) ramps up from 0 to 46 A, the B-H characteristic follows the path inside the loop starting at $B = H = 0$.

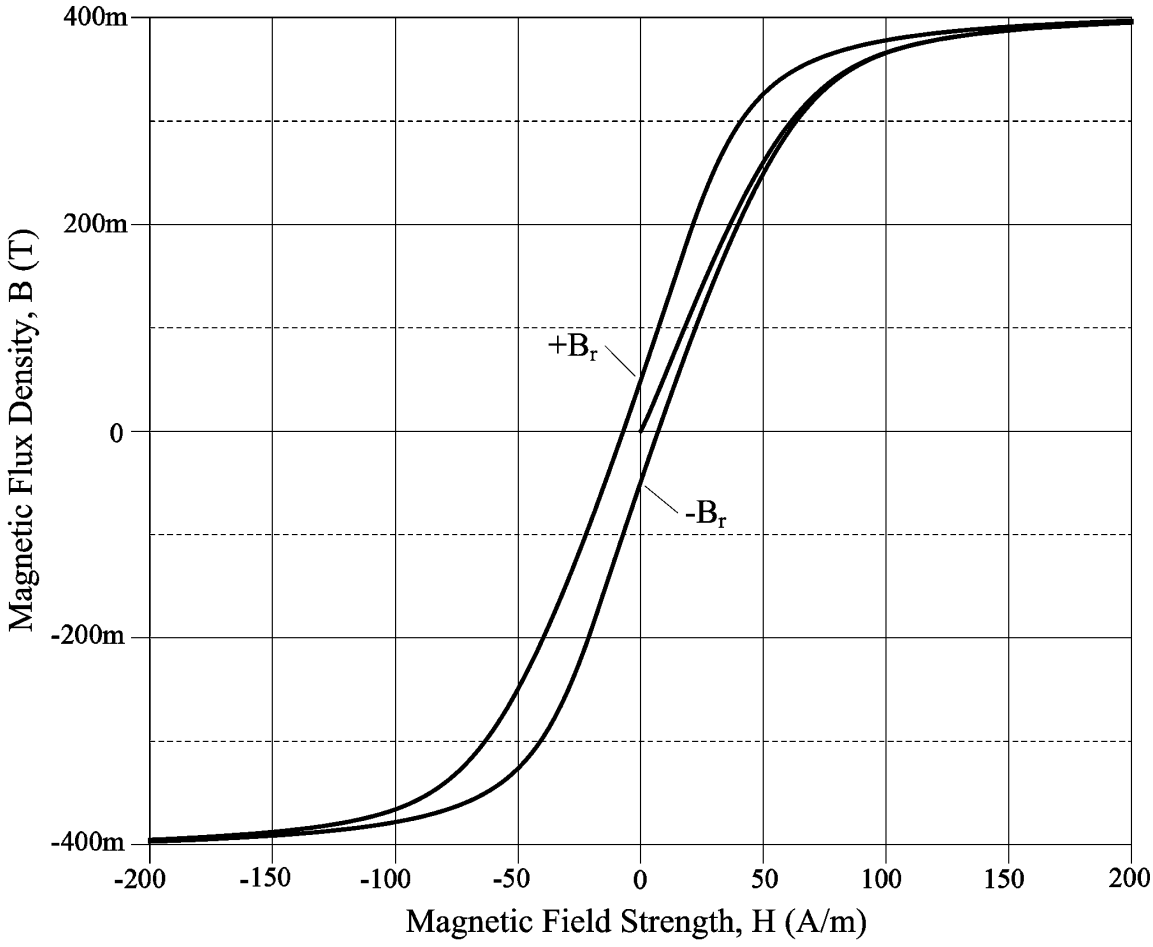

Figure 4-4: E-E core B-H characteristic plot from SPICE.

As the current ramps from 46 to –46 A, the B-H characteristic follows the path on the left, passing through the positive remanence point, $+B_r$. Finally, as the current ramps back

up from –46 to 46 A, the B-H characteristic follows the path on the right, passing through the negative remanence point, $-B_r$.

For any core, when current no longer flows in any of the windings (i.e. the magnetic field strength, $H = 0$), the magnetic flux density, B, can reside anywhere between the positive remanence point, $+B_r$, and the negative remanence point, $-B_r$, (shown in Figure 4-4) depending on how the current in the windings actually settled to zero.

At any point in the B-H characteristic, the relative permeability, μ_r, can be calculated given the magnetic flux density and magnetic field strength levels: $\mu_r = B/\mu_o H$. From Figure 4-4, one can recognize that μ_r is not constant (μ_r varies with the magnetic field strength level) and the relationship between B and H is non-linear. In addition, μ_r is dependent on the past history of the magnetic field strength. For a given magnetic field strength level, μ_r can take on an infinite number of values depending on the B-H characteristic path being taken (within the bounds shown in Figure 4-4).

If μ_r were constant (i.e. there were a linear relationship between B and H), then the inductance per squared turns of the ideal core could be calculated in a similar fashion to (4-1). In fact, (4-1) assumes linearity, which is a good assumption for a very small sinusoid centered on $B = H = 0$, since the B-H characteristic path is approximately a straight line with slope μ_i.

Since the core is non-linear, the inductance is a function of the magnetic flux density level, B, as well as the B-H characteristic path being taken. From Faraday's law, the voltage induced in an N turn winding about the core is:

$$V = NA_e \frac{dB}{dt}, \tag{4-3}$$

where A_e is the effective cross section of the core.

Since the dimensions of the E-E core are electrically small (i.e. the largest dimension is less than 1/10 of the signal wavelength [10]), Ampere's law, $\oint \vec{\mathbf{H}} \cdot \mathrm{d}\vec{\ell} = I_{enclosed}$, applies (i.e. the quasi static approximation of Maxwell's equations). From Ampere's law, the magnetic field strength due to current in an N turn winding about the core is:

$$H = \frac{NI}{l_e}, \tag{4-4}$$

where l_e is the effective magnetic path length.

From circuit analysis, the relationship between the inductance, voltage, and current, $V = LdI/dt$ can be combined with (4-3) and (4-4) to give [11]:

$$L = \frac{V}{dI/dt} = \frac{N^2 A_e}{l_e}\frac{dB}{dH}. \tag{4-5}$$

The inductance is proportional to the instantaneous slope (dB/dH) of the B-H characteristic path taken at any particular point in time.

Using SPICE, the inductance (referred to the $N = 9$ turn drive winding) for the B-H characteristic path from $B = H = 0$ to saturation (the center path shown in Figure 4-4) is plotted as a function of the magnetic flux density, B, in Figure 4-5.

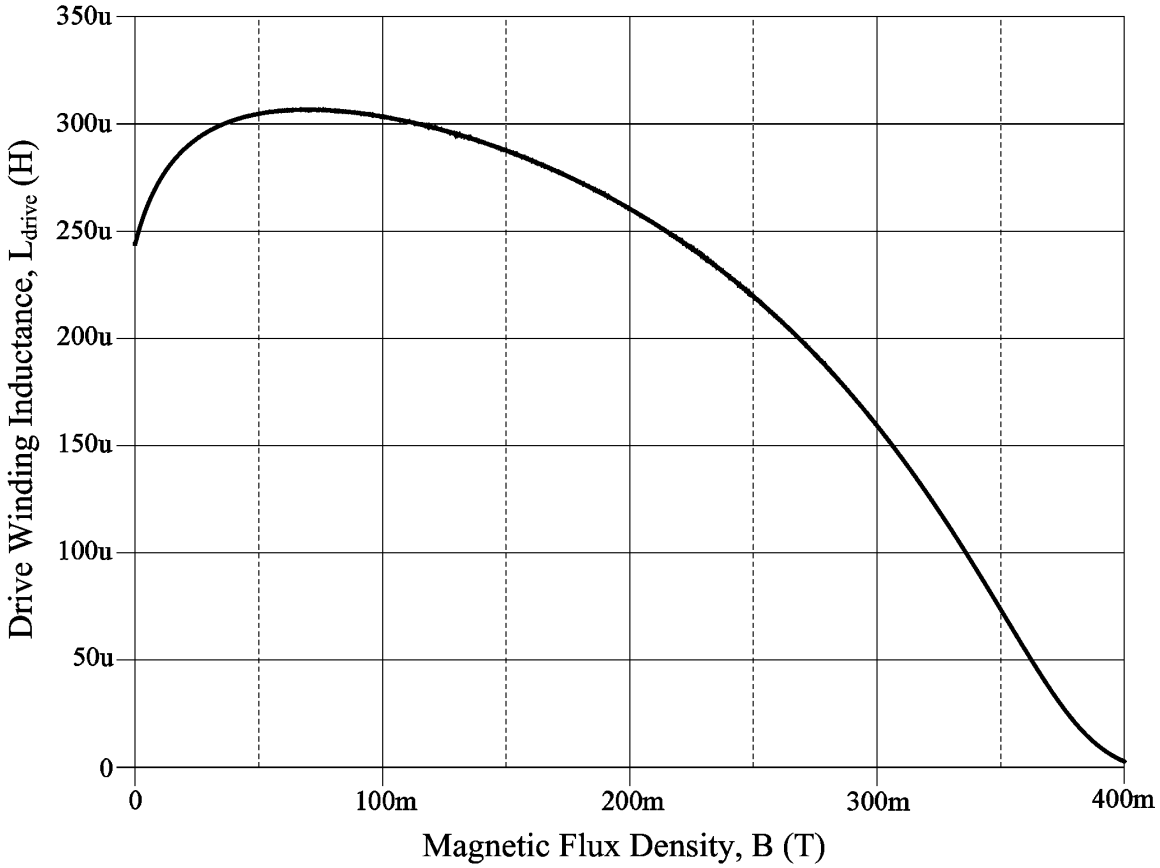

Figure 4-5: Inductance for the N = 9 turn drive winding as a function of magnetic flux density for the B-H characteristic path from B = H = 0 to saturation.

For the Isolated Analog Selector, the drive winding is driven at a fairly constant voltage for approximately 12 µs (while the compensation operational amplifier is enabled). Prior to the compensation operational amplifier driving the drive winding, the magnetic flux density in the core is basically somewhere between the positive and negative remanence points, $+B_r$ and $-B_r$.

If the magnetic flux density is at the negative remanence point when the compensation operational amplifier is enabled and driving a positive voltage, the B-H characteristic path taken is from the $-B_r$ point and up the right side of Figure 4-4. For this case, the inductance will tend to be higher than the level shown in Figure 4-5 since it is

following the outside right path, which has a steeper slope compared to the inside path of Figure 4-4.

If the magnetic flux density is at the positive remanence point, then the B-H characteristic path will start at $+B_r$ point and progress upward and to the right (beginning from the left B-H path, moving towards the right B-H path as it rises). For this case, the inductance will tend to be lower than the level shown in Figure 4-5.

Similarly, if the compensation operational amplifier is driving a negative signal, starting at the positive or negative remanence points will result in a larger or smaller inductance compared to Figure 4-5. Figure 4-6 shows three inductance curves (again, using SPICE) as a function of volt-time. The upper curve shows the inductance if the magnetic flux density starting point is $-B_r$ and the compensation operational amplifier is driving positive (or the magnetic flux density starting point is $+B_r$ and the compensation operational amplifier is driving negative).

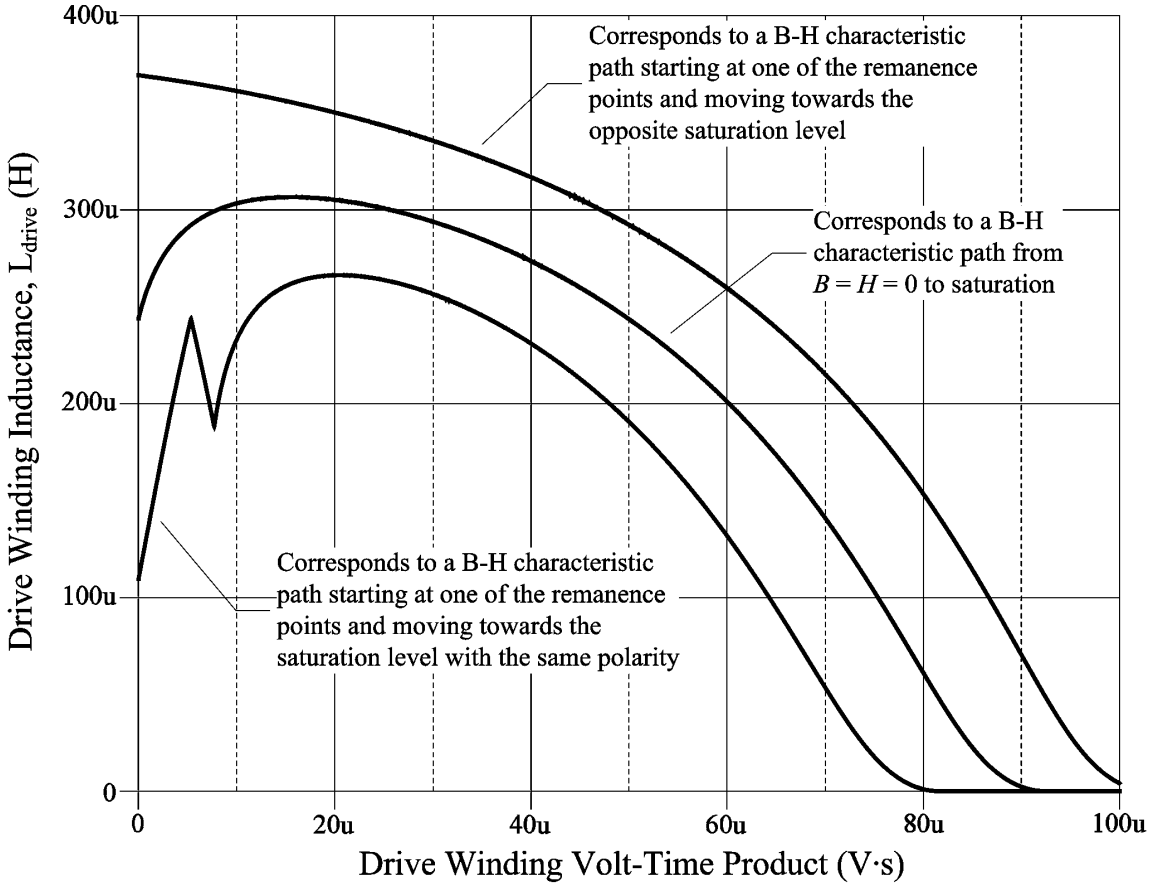

Figure 4-6: Inductance for the $N = 9$ turn drive winding as a function of the applied volt-time product.

The center curve of Figure 4-6 is the same as Figure 4-5 (for the center B-H characteristic path shown in Figure 4-4). The lower curve of Figure 4-6 shows the inductance if the magnetic flux density starting point is $+B_r$ and the compensation operational amplifier is driving negative (or the magnetic flux density starting point is $-B_r$ and the compensation operational amplifier is driving positive). The anomaly on the lower curve (abrupt change around 5 V·µs) is not real and is merely an anomaly in the SPICE implementation of the Jiles-Atherton model.

If the core is reset (i.e. no current is flowing in any of the windings), the actual inductance, as a function of the volt-time product, can be anywhere between the bounds of the upper and lower curves of Figure 4-6. Figure 4-6 provides a visual representation

of how the inductance changes as time progresses (when a dc voltage is applied to the drive winding) as well a clear insight into the volt-time product supported by the isolation transformer. The transformer is nearing saturation as the inductance drops below 50 μH..

The inductance curves of Figure 4-6 only capture the typical core characteristics at room temperature. The low signal inductance specified by the manufacture, A_L = 3100 nH/N^2, has a part-to-part variance of ±25%. Using the methods previously described, two other E-E core SPICE models are developed corresponding to the minimum and maximum part-to-part variance about the typical model.

Using the minimum, typical, and maximum room temperature models, the inductances, as a function of the volt-time product, are plotted using SPICE and shown in Figure 4-7. There are three sets of curves in Figure 4-7 (each set corresponds to the particular starting magnetic flux density level, similar to Figure 4-6). The upper, middle, and bottom curve in each set correspond to the maximum, typical, and minimum core models, respectively.

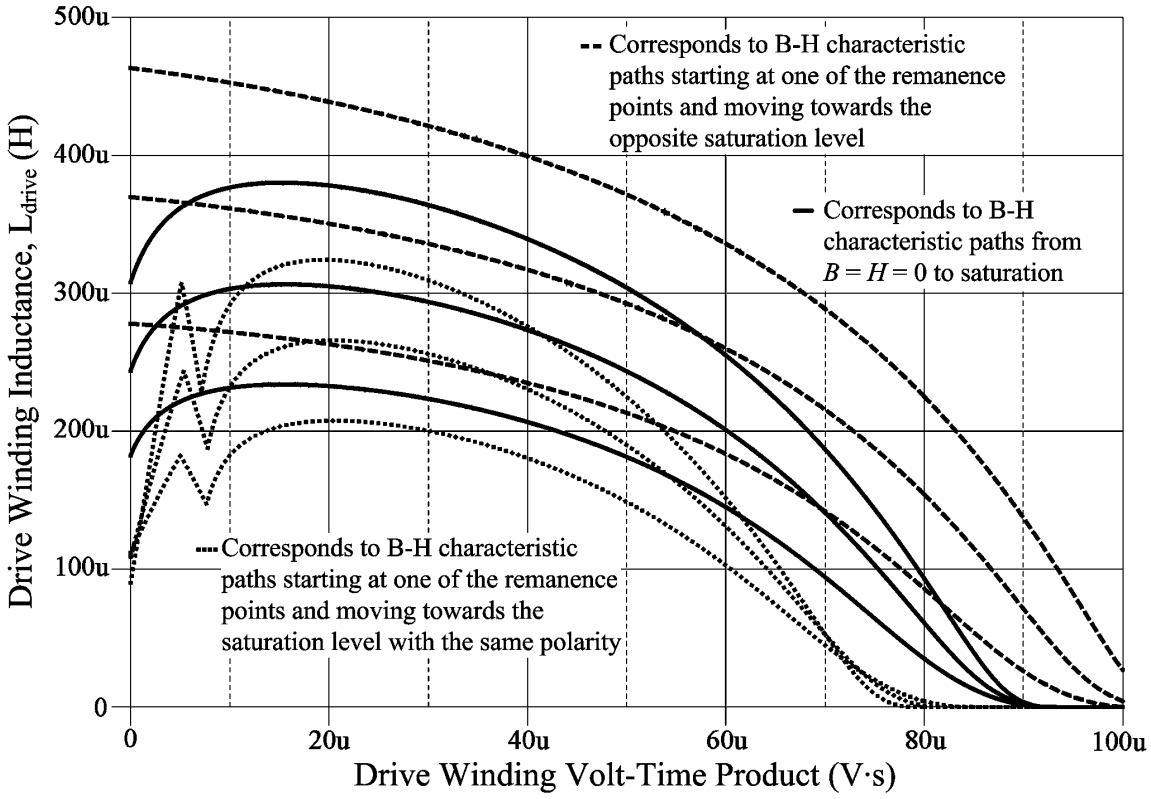

Figure 4-7: Minimum, typical and maximum inductance (at room temperature) for the N = 9 turn drive winding as a function of the applied volt-time product.

Figure 4-7 provides an excellent visual insight into the part-to-part and application variance of the E-E core, isolation transformer for the Isolated Analog Selector circuit at room temperature. The inductance variation is of little consequence to the compensation operational amplifier circuitry. The important consideration to the Isolated Analog Selector circuit design is the minimum inductance and volt-time product bounds.

In order to fully understand and model the compensation operational amplifier circuitry, the performance of the isolation transformer over the operating temperature range from –40 °C to 100 °C must be determined. The B-H characteristic of the E-E core also changes with temperature. Using the methods previously described and information about saturation and permeability changes with temperature (from the manufacture's datasheet), six other E-E core SPICE models are developed.

These additional six models correspond to the typical, minimum and maximum part-to-part variance at the temperature extremes of –40 °C and 100 °C. The Jiles-Atherton parameters used for the nine versions of the E-E core SPICE models are shown in Table 4-1.

E-E Core SPICE Model	MS	A	C	K	GAP (cm)
Typical @ 25 °C	327K	6	0.147	10.5	4.94e-4
Minimum @ 25 °C	327K	10.4	0.2	10.5	6.63e-4
Maximum @ 25 °C	327K	3.6	0.107	10.5	3.89e-4
Typical @ 100 °C	183K	1.3	0.081	4.2	4.94e-4
Minimum @ 100 °C	183K	2.55	0.124	4.2	6.63e-4
Maximum @ 100 °C	183K	0.65	0.049	4.2	3.89e-4
Typical @ -40 °C	384K	36	0.49	11	4.94e-4
Minimum @ -40 °C	384K	51.5	0.545	11	6.63e-4
Maximum @ -40 °C	384K	27.2	0.45	11	3.89e-4

Table 4-1: Jiles-Atherton Parameters for the nine versions of E-E core SPICE models representing the part-to-part variations as well as the temperature extreme variations.

The B-H characteristics for the typical E-E core SPICE models for 25 °C, 100 °C and –40 °C are shown in Figure 4-8. As the temperature increases, the slope of the B-H characteristic increase (i.e. inductance increases), but the saturation level (i.e. volt-time product) decreases. As the temperature decreases, the slope of the B-H characteristic decreases (i.e. inductance decreases), and the saturation level (i.e. volt-time product) slightly increases. See Appendix A.1 for the nine E-E core SPICE models.

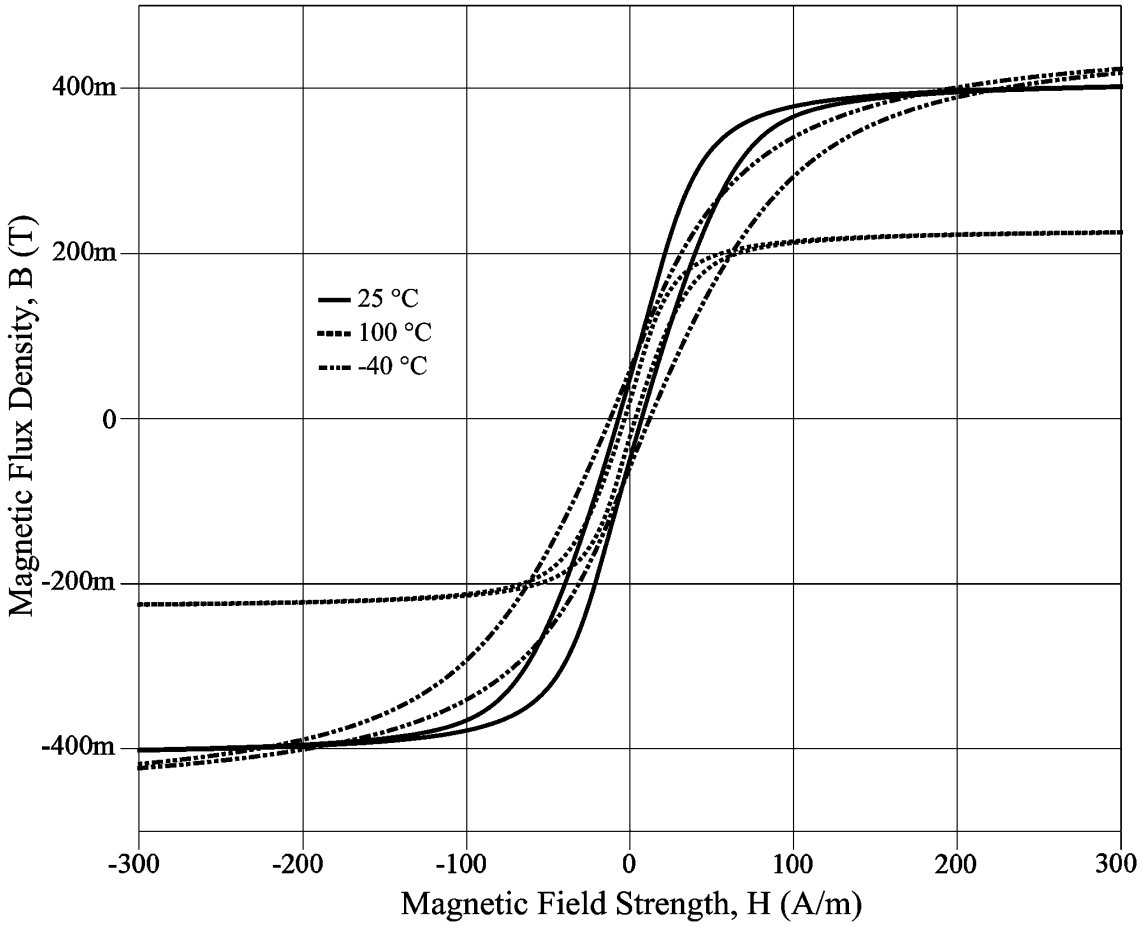

Figure 4-8: B-H characteristics for the typical E-E core SPICE models for 25 °C, 100 °C and –40 °C.

Again, using the minimum, typical, and maximum E-E core SPICE models, the inductances, as a function of the volt-time product, are plotted using SPICE and shown in Figure 4-9. Figure 4-9(a) and Figure 4-9(b) show the part-to-part and application variance of the inductance and volt-time product at the temperature extremes of 100 °C and –40 °C, respectively (similar to the room temperature variance shown in Figure 4-7).

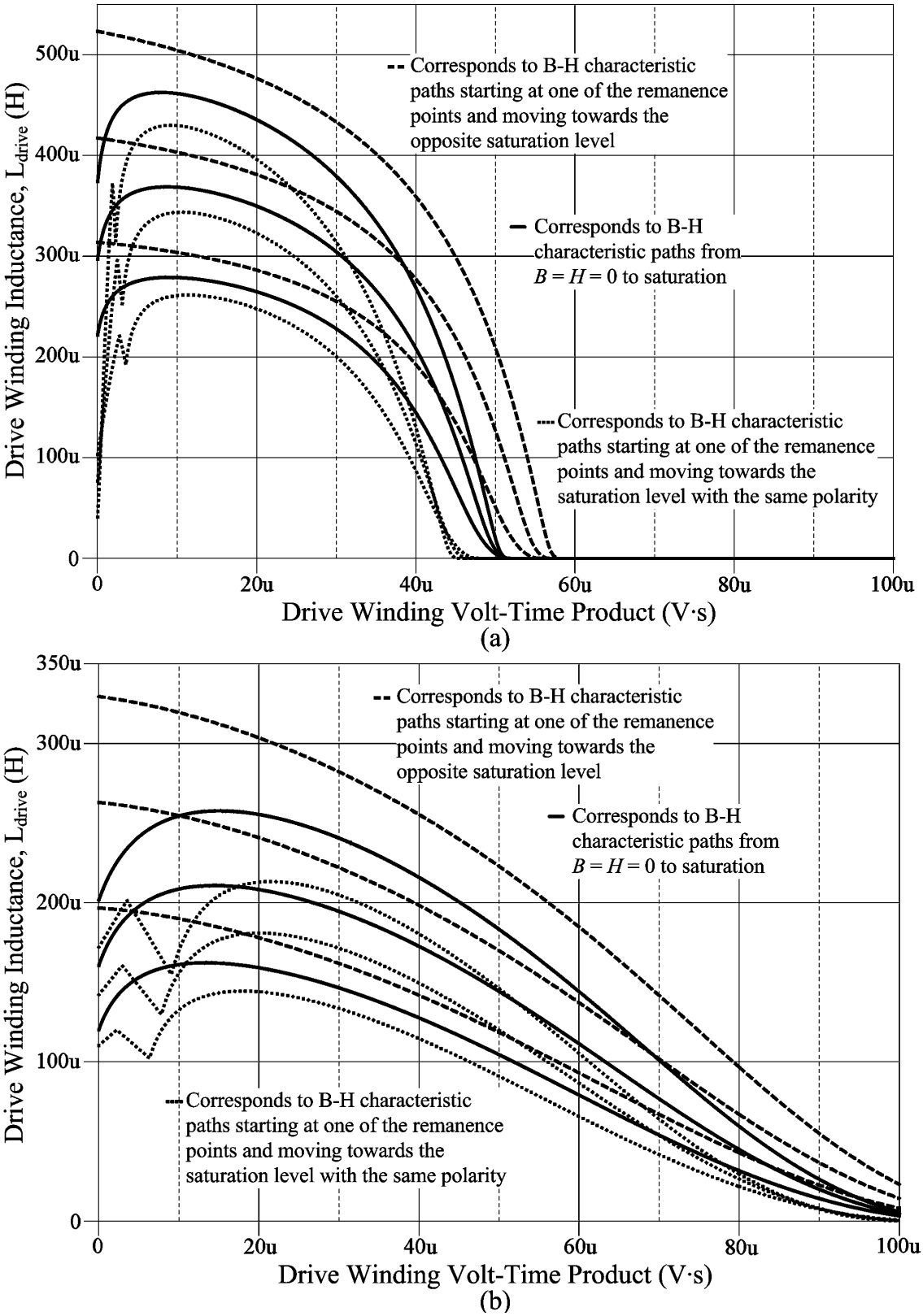

Figure 4-9: Minimum, typical and maximum inductance for the $N = 9$ turn drive winding as a function of the applied volt-time product: (a) at 100 °C and (b) at –40 °C.

The available volt-time product is lowest at the high temperature extreme. An adequate design constraint of the Isolated Analog Selector circuit is to limit the volt-time product of the drive winding to 35 V·µs or less. This design constraint guarantees that the isolation transformer will not saturate at any temperature or with any part-to-part variation.

The inductance is lowest at the cold temperature extreme. An adequate design constraint of the Isolated Analog Selector circuit is to allow for a minimum inductance of 125 µH (approximate average inductance at the cold temperature through 35 V·µs).

The nine E-E core SPICE models capture the part-to-part and temperature variations of the isolation transformer. These models are used to help verify the accuracy, settling and stability of the compensation operational amplifier circuitry.

4.3 Printed Circuit Board Winding Resistance

The windings of the isolation transformer are made with printed circuit board traces. The traces are 5 mil thick with 5 mil spacing on 1 oz copper inner layers (typical trace thickness of 1.38 mil). Due to the etching process used in creating the traces, there is a tolerance of ± 1 mil on the effective width, and the thickness may decrease to 0.98 mil, per the IPC standard [12].

The cross section of the printed circuit board winding trace is typically 3.81×10^{-9} m^2, with a minimum of 2.53×10^{-9} m^2 and a maximum of 5.34×10^{-9} m^2. The conductance of copper, σ_{cu}, is 5.8×10^{7} S/m and the dc resistance of the copper traces changes with temperature (temperature coefficient of around +4000 ppm/°C).

The length of the 9 turn drive winding, 7 turn sense winding, and 23 turn signal winding is approximately 0.28 m, 0.44 m, and 1.04 m respectively. Table 4-2 shows the

variance of the winding dc resistance due to printed circuit board variances and temperature extremes.

Variation	R_{Drive} (Ω)	R_{Sense} (Ω)	R_{Signal} (Ω)
Typical @ 25 °C	1.26	2.00	4.70
Minimum @ 25 °C	0.90	1.42	3.35
Maximum @ 25 °C	1.90	3.01	7.08
Typical @ 100 °C	1.63	2.58	6.08
Minimum @ 100 °C	1.16	1.84	4.33
Maximum @ 100 °C	2.46	3.89	9.15
Typical @ -40 °C	0.94	1.49	3.51
Minimum @ -40 °C	0.67	1.06	2.50
Maximum @ -40 °C	1.42	2.24	5.28

Table 4-2: Variation in winding resistance due to printed circuit board variances and temperature extremes.

The dc resistances in Table 4-2 are also valid for low frequencies where skin and proximity effects are not prevalent. The frequency corresponding to a skin depth, δ, equal to half the thickness of the 1.38 mil printed circuit board copper trace is [13]:

$$f = \frac{1}{\pi \mu_o \sigma_{cu} \delta^2} = 14.2 \text{ MHz}. \quad (4\text{-}6)$$

An FEA (Finite Element Analysis) tool is used to simulate the magnetic coupling between the drive, sense, and signal windings. Chapter 6 describes the use of the FEA tool for modeling and analyzing the isolation transformer used in the Isolated Analog Selector circuit. Using the FEA tool, a sinusoid is applied to the drive winding at various frequencies. Observing the current distribution throughout the cross section of the printed circuit board traces shows that proximity and skin effect are virtually non-existent below 1 MHz.

Although there is some high frequency content to the step response, when the compensation operational amplifier is first enabled, the settling is at a much slower rate after around 1 μs (see the next chapter for further details on the settling of the step response). The main purpose of modeling the compensation operational amplifier circuitry is to analyze the settling, stability, and accuracy after the initial transient is over (during the settling response). Therefore, skin effect and proximity effect can be ignored when modeling the transformer winding resistance and leakage inductance of the isolation transformer.

4.4 Printed Circuit Board Winding Leakage Inductance and Winding Capacitance

The leakage inductance of the drive, sense, and signal windings are easily determined using the FEA tool. The isolation transformer windings are constructed with printed circuit board traces and have virtually no freedom of movement. In addition, the primary and secondary printed circuit boards are fairly fixed relative to each other due to the plastic insulation spacers and the mounting of the printed circuit boards. See Chapter 3 for the details of the isolation transformer construction.

The leakage inductance for each winding can be viewed as a constant. The FEA tool is used to determine the leakage inductance of each winding as shown in Table 4-3. Since the leakage inductance is primarily a function of the physical location of the windings relative to each other, there is virtually no variation from part-to-part or over temperature.

Winding	Leakage Inductance (μH)
Drive	1.3
Sense	0.7
Signal	4.9

Table 4-3: Leakage inductance of the printed circuit board drive, sense, and signal printed circuit board windings.

Winding capacitance is also a function of the physical location of the windings relative to each other and to the Faraday shield/planes of the printed circuit boards. Table 4-4 shows the various capacitances for the printed circuit board windings. These capacitances are calculated using a formula for inner layer printed circuit board traces between two planes [14].

Parasitic Capacitance	Capacitance Value (pF)
Drive to Primary Faraday shield	21
Sense to Primary Faraday shield	33
Drive to Sense	2
Signal to Secondary Faraday shield	78

Table 4-4: Capacitances associated with the printed circuit board windings.

4.5 SPICE Model of the Isolation Transformer

The E-E core modeling combined with the printed circuit board winding resistance, leakage inductance and capacitances make up the SPICE model of the isolation transformer as shown in Figure 4-10.

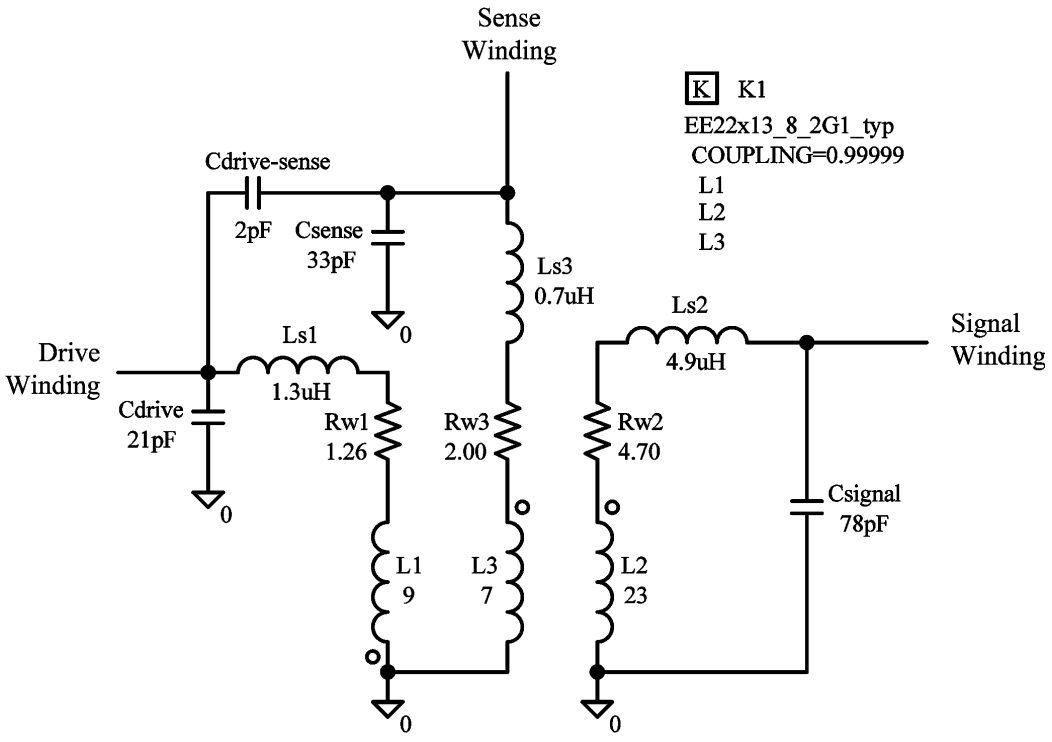

Figure 4-10: SPICE model of the Isolation Transformer.

The 9 turn drive winding, 7 turn sense winding and 23 turn signal winding are all coupled to the E-E core model, K1. The model of the E-E core can be assigned to any of the nine models of Table 4-1, depending on the variance to be simulated. Likewise, the winding resistances can be assigned to any of the corresponding values from Table 4-2 for the same variance and temperature analysis.

The SPICE model of Figure 4-10 can be used to analyze the compensation operational amplifier circuit stability, accuracy and settling. The model is valid for frequency up to 1 MHz. The model assumes the drive, sense, and signal windings are equally coupled to the E-E core model, K1 (i.e. the drive to sense winding coupling is proportional to the drive to signal winding coupling by the appropriate turns ratios). In actuality, there is an error due to a coupling mismatch between the three windings as outlined in Chapter 6.

Chapter 5 Compensation Operational Amplifier Circuit Performance

The compensation operational amplifier circuitry, used in the Analog Selector Circuit of Figure 1-3, plays a key role in the performance and accuracy of the overall transformer isolated analog acquisition system. When enabled to drive the isolated signal through the isolation transformer, the electronic control circuitry (containing the compensation operational amplifier) must be stable and settle to an accurate output voltage level at the moment that the A-D converter samples the corresponding analog channel.

The trigger/timer circuit of Figure 2-1, enables the compensation operational amplifier at least 8 μs prior to the A-D converter's start of conversion. In order to achieve an overall acquisition system accuracy of ±0.1 %, the compensation operational amplifier circuit is constrained to settle within an error of ±0.02 % after 8 μs.

The purpose of this chapter is to show that the compensation operational amplifier circuit yields a stable system, capable of an output voltage signal accuracy of at least ±0.02 %, 8 μs after being enabled. SPICE is used to model the circuitry and measure the stability, settling and accuracy of the output signal.

Stability is analyzed by observation of the SPICE generated, open loop gain/phase plots (frequency response) of the electronic control circuitry. Section 5.1 reviews control loop stability in regards to the open loop gain/phase characteristics. As an introduction to the SPICE generated open loop gain/phase plots and other plots using SPICE, the stability and settling a 2^{nd} order passive low-pass filter is analyzed in section 5.2. These first two sections are presented in order to provide a foundation for understanding and analyzing the SPICE generated plots.

Section 5.3 introduces the SPICE modeling of the compensation operational amplifier configured as a simple voltage follower. Various SPICE plots are generated to validate that the operational amplifier SPICE model is aligned with the manufacture's datasheet. Section 5.4 presents the concept of lead/lag compensation with an operational amplifier. These two sections provide key components to understanding the stability and settling of the actual compensation operational amplifier circuitry as well as the accuracy of the output voltage signal (hereafter referred to as simply "accuracy").

The design challenges and design progression of the compensation operational amplifier circuitry are presented in section 5.5. The method chosen to convey the need and design of the drive amplifier circuit, snubber/output filter network, lag compensation network and lead compensation network blocks (of Figure 2-1) is to 1) analyze the compensation operational amplifier circuitry without these blocks; 2) identify the issues/problems with stability, settling, and accuracy; and 3) introduce these blocks as an adequate solution/improvement to these issues/problems. Of course, one may design these blocks using a top down/system approach. However, the bottom up approach taken in section 5.5 gives some insight into the purpose and design constraints of each block.

Finally, section 5.6 presents the SPICE analysis of the stability, settling and accuracy of the compensation operational amplifier circuitry and isolation transformer used in the Isolated Analog Selector. An analysis of stability and accuracy considering component part-to-part and temperature extreme variations is also provided.

Stability, settling, and accuracy are interrelated. Usually, there is a tradeoff between the margin of stability and settling time. Settling is an important part of accuracy. As

will be shown in the following sections, once the control circuit has settled, the accuracy is determined by the amount of available open loop gain of the control system.

5.1 Control Loop Stability

A basic control loop for a linear voltage input/output system can be modeled in the frequency domain with a forward transfer function, G(*s*), and a feedback transfer function, H(*s*) as shown in Figure 5-1 [15]. G(*s*) is typically referred to as the system and H(*s*) is referred to as the controller.

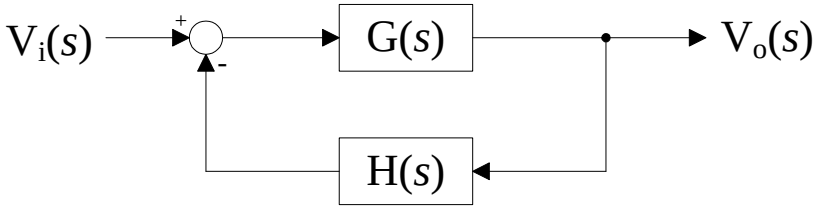

Figure 5-1: Basic control loop.

The transfer function, T(*s*), is the ratio of output voltage signal to input voltage signal and can be calculated in terms of the forward and feedback transfer functions, G(*s*) and H(*s*), respectively:

$$\frac{V_o(s)}{V_i(s)} = T(s) = \frac{G(s)}{1 + G(s)H(s)}. \qquad (5\text{-}1)$$

The numerator and denominator of the transfer function can typically be factored. Each factor in the numerator identifies the zeros (i.e. values for *s* resulting in zero for the numerator). Similarly, each factor in the denominator identifies the poles (i.e. values for *s* resulting in zero for the denominator). Stability is determined by analyzing the denominator of 1 + G(*s*)H(*s*), which is known as the characteristic polynomial.

The stability criteria for a control system is that the characteristic polynomial, denominator of T(*s*), contains no right half plane roots (in the s plane). Sometimes

factoring the characteristic polynomial is impractical and the Routh-Hurwitz test can be applied to determine the number of right half plane and imaginary axis roots [16].

Another method for determining stability is to analyze the open loop frequency response: $G(j\omega)H(j\omega)$ of the control loop. A control loop is unstable (i.e. characteristic polynomial right half plane root(s)) if the magnitude of the open loop response is greater than or equal to unity at an open loop phase of ±180°. As long as there are no characteristic polynomial right half plane real root(s), the control loop is stable if [17]:

$$\left|G(j\omega)H(j\omega)\right| < 0\,\text{dB}\text{, for } \omega \text{ such that the angle of } G(j\omega)H(j\omega) = \pm 180^\circ . \qquad (5\text{-}2)$$

Analyzing the open loop gain of an electronic circuit is easily done using SPICE. As exposed in the next sections, open loop gain/phase plots generated using SPICE can quickly identify the stability or instability of an electronic circuit. A common design guideline is to have an adequate gain margin (> 12 dB) and phase margin (> 30°). Having good gain and phase margins yield good transient performance, and contribute to the robustness of the circuitry over time or extreme conditions.

The gain margin is a measurement (in dB) of how far the gain is below unity gain (0 dB) at the point(s) the phase crosses through ±180°. The phase margin is typically a measurement (in °) of how far away the phase is from ±180° at the point(s) the gain crosses through unity gain (0 dB). Phase margin is further defined as the minimum distance the phase is from ±180° for all gain greater than 0 dB. The subsequent sections will provide a few examples of phase and gain margins.

A design goal of the compensation operational amplifier circuitry is to achieve a gain margin > 12 dB and a phase margin > 30°.

5.2 Stability and Settling Analysis of a 2nd Order Passive Low Pass Filter Using SPICE

An illustrative and insightful example of using SPICE to 1) generate a gain/phase plot and 2) to observe the settling/accuracy of an output signal to a unit step input signal, is obtained by analyzing the 2nd order passive low-pass filter shown in Figure 5-2.

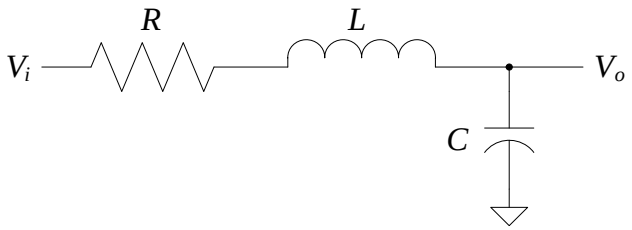

Figure 5-2: 2nd order passive low-pass filter.

In addition to obtaining the transfer function and step response for the 2nd order passive low-pass filter, the system dynamics are also viewed as a unity feedback control system later in this section. The transfer function for the RLC (resistor, inductor, capacitor) passive low-pass filter circuit of Figure 5-2 is:

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{1 + RCs + LCs^2} = \frac{\omega_o^2}{s^2 + 2\alpha s + \omega_o^2}, \qquad (5\text{-}3)$$

where $\omega_o = 1/\sqrt{LC}$ and $\alpha = R/2L$.

Depending on the values of α and ω_o (i.e. R, L and C), the circuit is under damped ($\alpha < \omega_o$), critically damped ($\alpha = \omega_o$), or over damped ($\alpha > \omega_o$). The Bode plots of the transfer function are shown in Figure 5-3 and the step responses are shown in Figure 5-4 for the under damped, critically damped, and over damped cases.

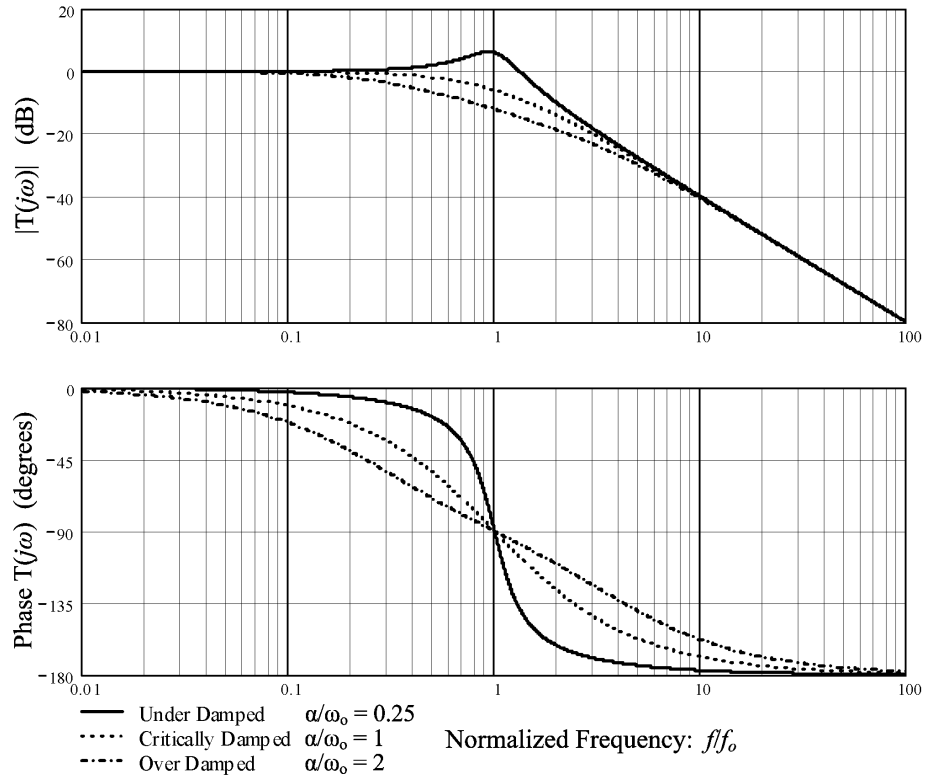

Figure 5-3: Transfer function Bode plots for 2nd order low-pass system (under damped, critically damped, and over damped).

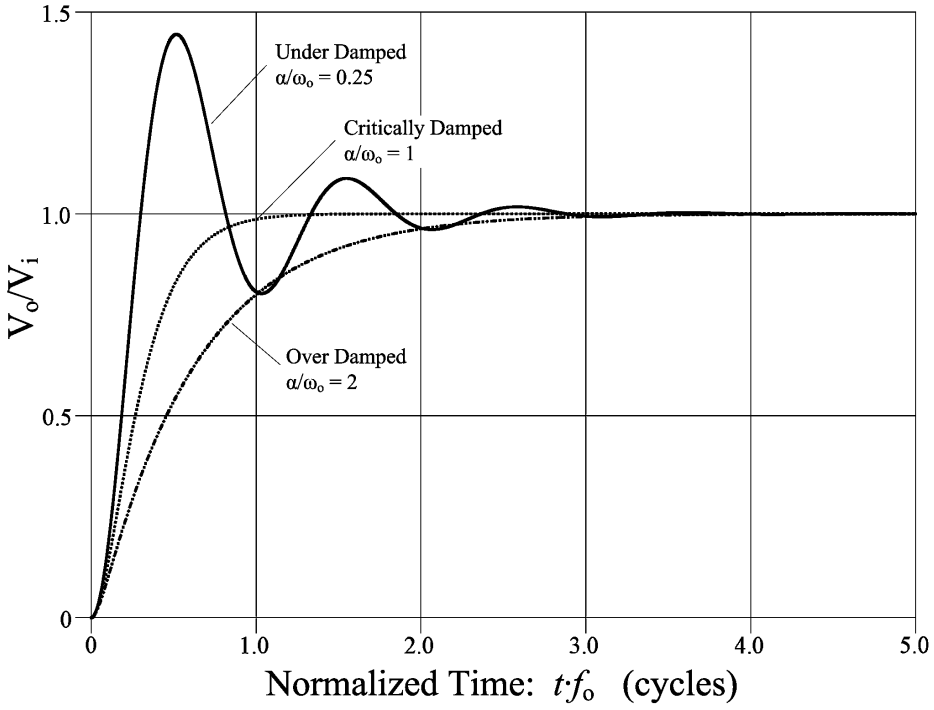

Figure 5-4: Step response for 2nd order low-pass system (under damped, critically damped, and over damped).

Some useful insight into the 2nd order passive low-pass filter is achieved by rearranging the transfer function into a form of a control loop, similar to (5-1):

$$T(s) = \frac{\omega_o^2}{s^2 + 2\alpha s + \omega_o^2} = \frac{\dfrac{\omega_o^2}{s(s+2\alpha)}}{1 + \dfrac{\omega_o^2}{s(s+2\alpha)}}. \qquad (5\text{-}4)$$

By inspection of (5-1) and (5-4) the feedback transfer function is H(s) = 1 and the 2nd order low-pass system is transformed to the control loop shown in Figure 5-5.

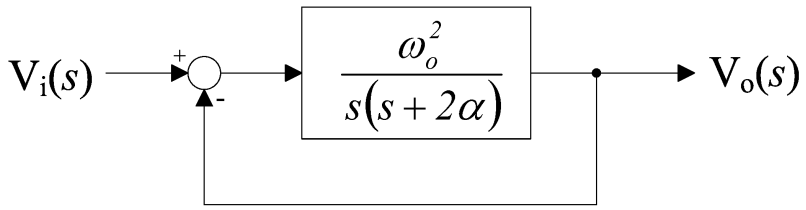

Figure 5-5: Control loop for 2nd order low-pass system.

SPICE is used to generate the open loop gain/phase plot for the control system of Figure 5-5. The open loop gain/phase plot for the under damped, critically damped and over damped cases are shown in Figure 5-6. All of the open loop gain/phase plots generated by SPICE (presented in this chapter) have a similar layout. The gain axis (in dB = 20log(|G($j\omega$)H($j\omega$)|) is on the left and the phase axis (in degrees) is on the right. The unity gain point, 0 dB (on the left axis), is always aligned with the phase = -180 degrees point (on the right axis). The frequency axis is a log scale.

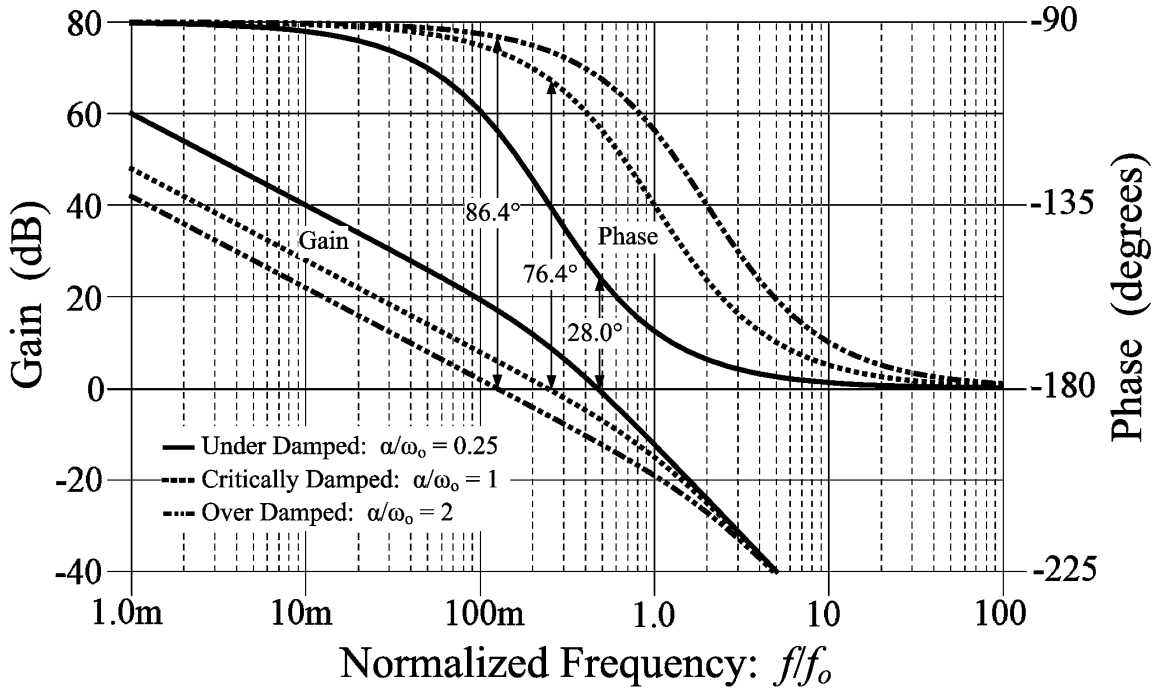

Figure 5-6: Open loop gain/phase plot for 2nd order low-pass system.

The phase plots (upper three curves of Figure 5-6) start at –90 degrees for low frequencies and transition to –180 degrees for high frequencies. The gain plots (lower three curves of Figure 5-6) all continue to progress higher at lower frequencies. Since the unity gain (0 dB) point on the left axis is aligned with the –180 degree point on the right axis, the phase margin is easily determined by 1) identifying the frequency that the gain curve crosses through unity (0 dB) and measuring the degrees between that point and the phase cure. The under damped, critically damped, and over damped cases have a phase margin of 28.0°, 76.4° and 86.4° respectively.

With the 2nd order low-pass system, there is a relationship between the phase margin of the open loop gain/phase plot (Figure 5-6) and the overshoot of the step response (Figure 5-4). This relationship can be determined analytically and is shown in Figure 5-7. Figure 5-7 is a great reference to obtain a first order prediction of a control system's

phase margin given the percent overshoot of a voltage signal (at any node in the closed loop path) due to an input step change.

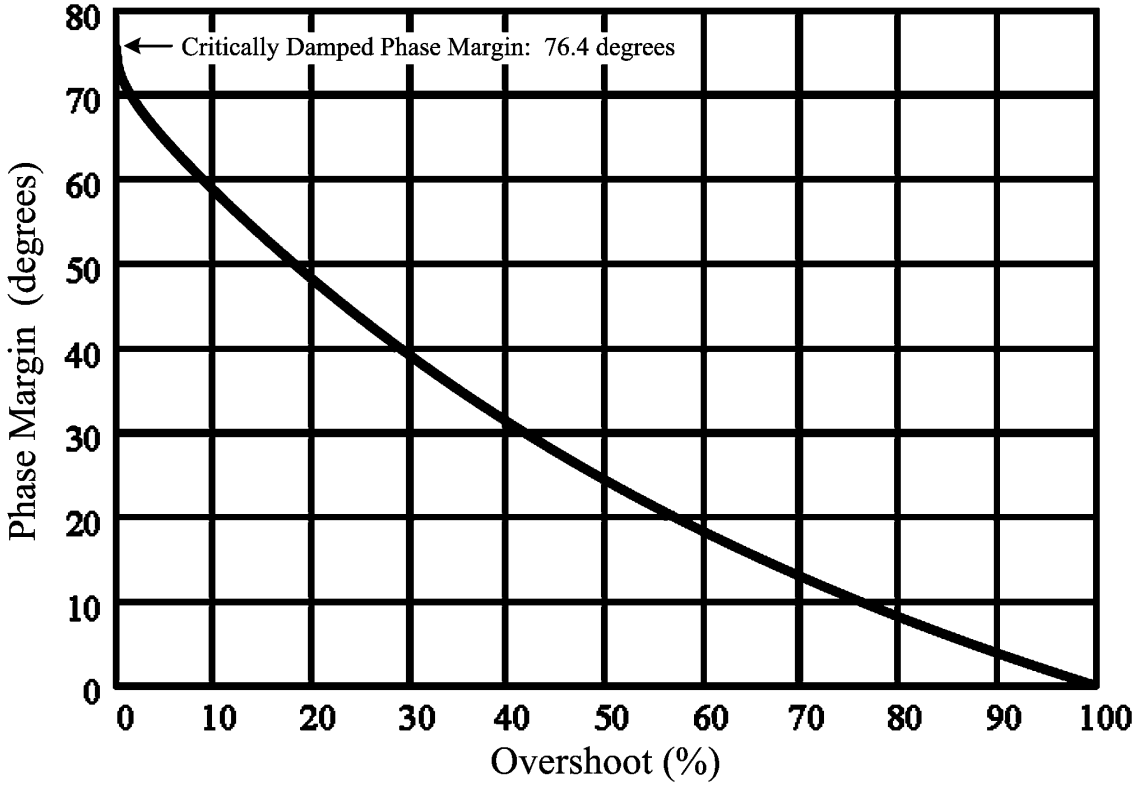

Figure 5-7: Percent Overshoot versus phase margin for 2nd order system.

Another plot generated using SPICE, is the output error (in dB = $20\log|(V_o - V_i)/V_i|$) versus time shown in Figure 5-8. This plot reveals how quickly the output signal settles and to what level of accuracy. For the 2nd order low-pass system, the output voltage never really settles, but continually gets closer to the input voltage level (error approaches zero as time approaches infinity). This correlates to the gain/phase plot: as the frequency approaches zero, the available gain of the "control loop" approaches infinity (as shown in Figure 5-6).

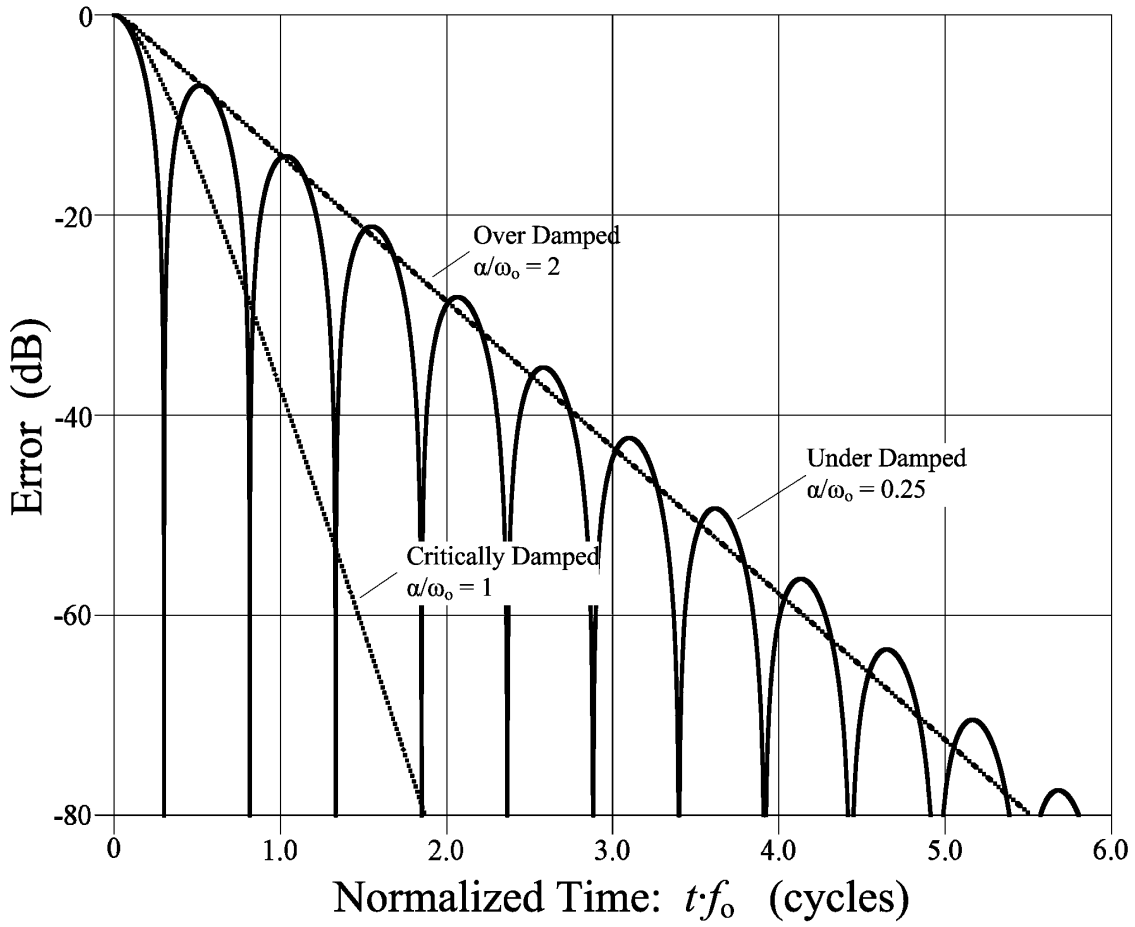

Figure 5-8: Settling time/error for 2nd order low-pass system.

Plots similar to Figure 5-4 (step response plot), Figure 5-6 (open loop gain/phase plots), and Figure 5-8 (settling time/error plot) generated using SPICE are presented throughout the remainder of this chapter. Particularly, the open loop gain/phase plots are used to determine the gain and phase margins and the settling time/error plot to determine the accuracy. One can obtain some insight into gain/phase plots by analyzing and observing the gain/phase plots of the 2nd order low-pass system given previously in this section.

5.3 Compensation Operational Amplifier SPICE Modeling, Stability and Accuracy

Operational amplifiers are used throughout the electronic industry and are the basic building blocks for many control systems. The transfer function of an operational amplifier circuit can be quite complicated. A simplified block diagram of the transfer function elements for an operational amplifier is shown in Figure 5-9.

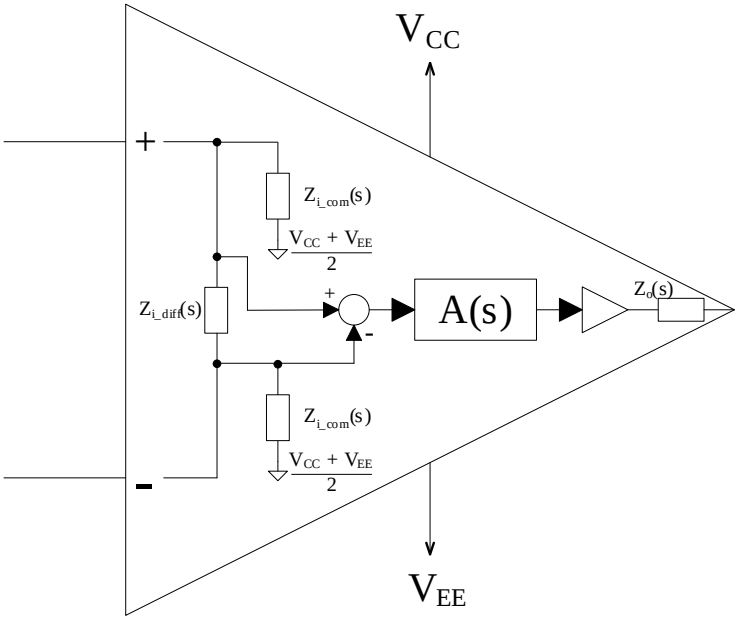

Figure 5-9: Operational amplifier transfer function elements.

Typically the common mode and differential mode input impedances, $Z_{i\_com}(s)$ and $Z_{i\_diff}(s)$ respectively, are large and the output impedance, $Z_o(s)$ is small. These impedances are ignored for the ideal operational amplifier. The gain of the operational amplifier, $|A(j\omega)|$, is assumed large for lower frequencies.

A typical configuration for an operational amplifier is the voltage follower shown in Figure 5-10. Ignoring the input and output impedances for the moment, the control system of Figure 5-10 is nothing more than the control loop of Figure 5-1 with G(s) = A(s) and H(s) = 1.

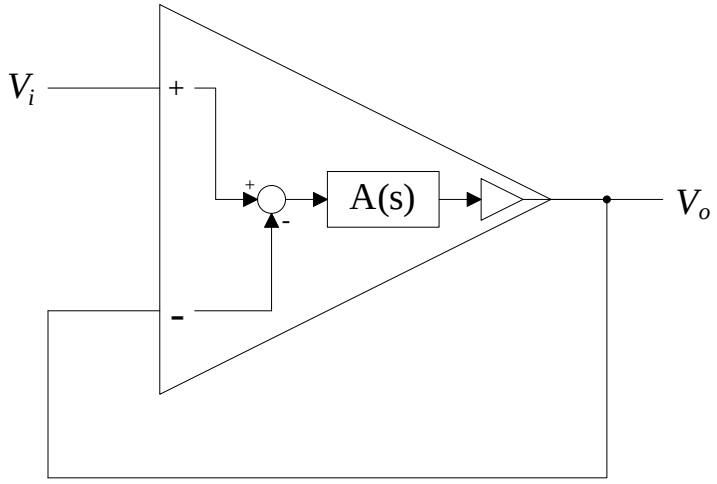

Figure 5-10: Operational amplifier voltage follower.

Therefore, the open loop transfer function of the voltage follower operational amplifier circuit is merely the operational amplifier's open loop transfer function, A(s). Most operational amplifier datasheets provide an open loop gain/phase plot. The open loop/gain phase plot for the OPA357 operational amplifier used in the Isolated Analog Selector circuit is shown in Figure 5-11 (output loading specified at 1 kΩ) [18].

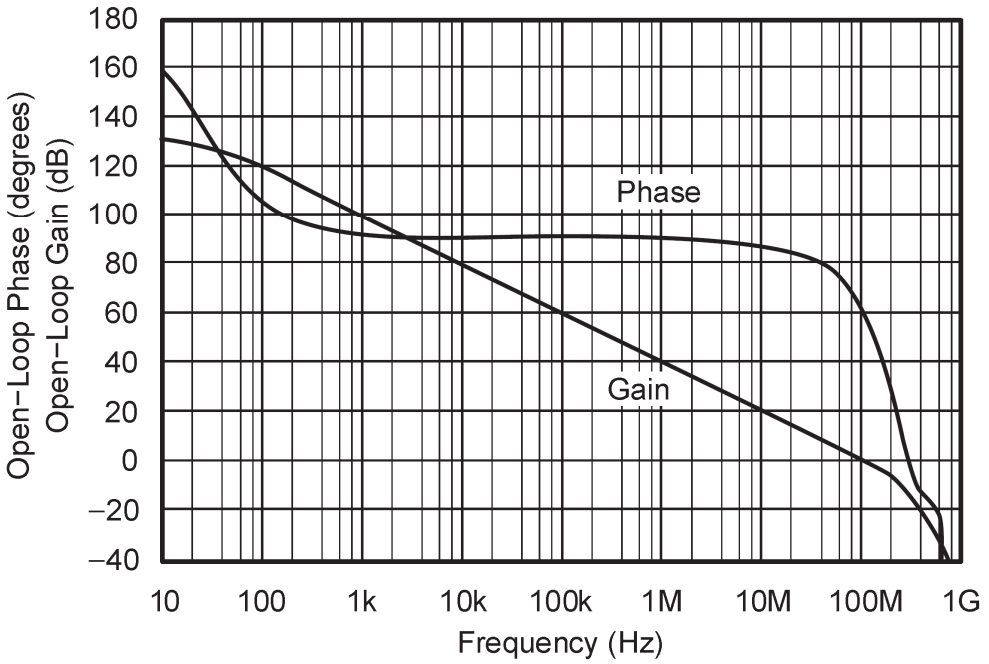

Figure 5-11: OPA357 datasheet open loop gain/phase plot (Courtesy Texas Instruments).

As with most operational amplifiers, the OPA357 is stable when configured as a voltage follower, with a phase margin of approximately 60°. A typical operational amplifier has an open loop low frequency pole (around 30 Hz for the OPA357) determined by the gain-bandwidth product of the operational amplifier and the low frequency gain. Most operational amplifiers have many open loop poles existing at or above the unity gain frequency.

In order to use SPICE to analyze a control circuit containing an operational amplifier, a SPICE model for the operational amplifier needs to be obtained or created. SPICE models for most operational amplifiers can be downloaded from the manufacture's website, as is the case with the OPA357 (see Appendix A.2 for OPA357 SPICE Model).

However, as with any device, the SPICE model should be validated before relying on any SPICE results obtained. A good starting place to validate the SPICE model is to generate an open loop gain/phase plot for the OPA357 voltage follower circuit. The SPICE schematic for generating the open loop gain/phase plot is shown in Figure 5-12. V1 is a small ac voltage signal (1 mV) that is swept in frequency by the SPICE simulator. V1 is connected between the negative (-) input of the OPA357 and the output of the unity gain buffer. The purpose of the buffer is so the voltage source V1 does not interfere with the output impedance of the operational amplifier. Vin can be varied between Vee and Vcc to analyze the gain/phase plot at different dc bias operation points of the OPA357.

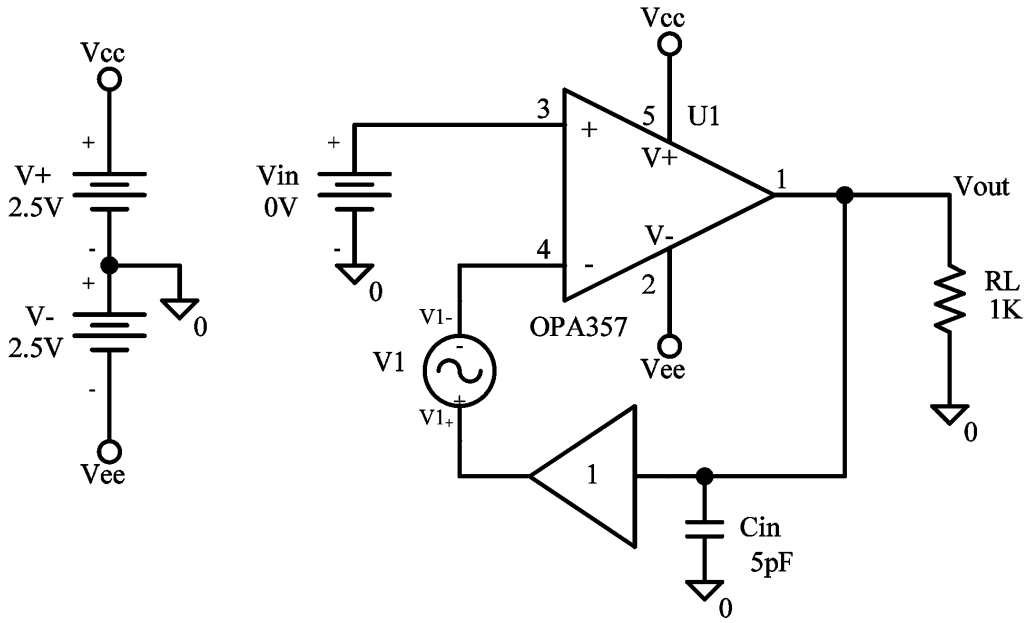

Figure 5-12: SPICE schematic for generating OPA357 open loop gain and phase plot.

With the addition of the unity buffer to the SPICE circuit, the input impedance of the OPA357 needs to be modeled at the input of the unity buffer. This is accomplished by adding the C_{in} = 5 pF (input capacitance specified by the OPA357's datasheet) to the input of the unity buffer. The open loop transfer function is then calculated by dividing the voltage at the output of the unity buffer, $V1_+$ (with respect to ground), by the voltage at the negative (-) terminal of the operational amplifier, $V1_-$ (with respect to ground). Since $V1_+$ equals the negative of $V1_-$ times the open loop transfer function, $G(j\omega)$, the open loop transfer function can be calculated in SPICE as:

$$G(j\omega) = -\frac{V1_+}{V1_-}. \qquad (5\text{-}5)$$

The open loop transfer function, $G(j\omega)$, accounts for the open loop transfer function of the OPA357 plus the additional transfer function of the output impedance of the OPA357 interacting with the 1 kΩ load resistance in parallel with the 5 pF input capacitance. The open loop gain/phase plot generated by SPICE is shown in Figure 5-13.

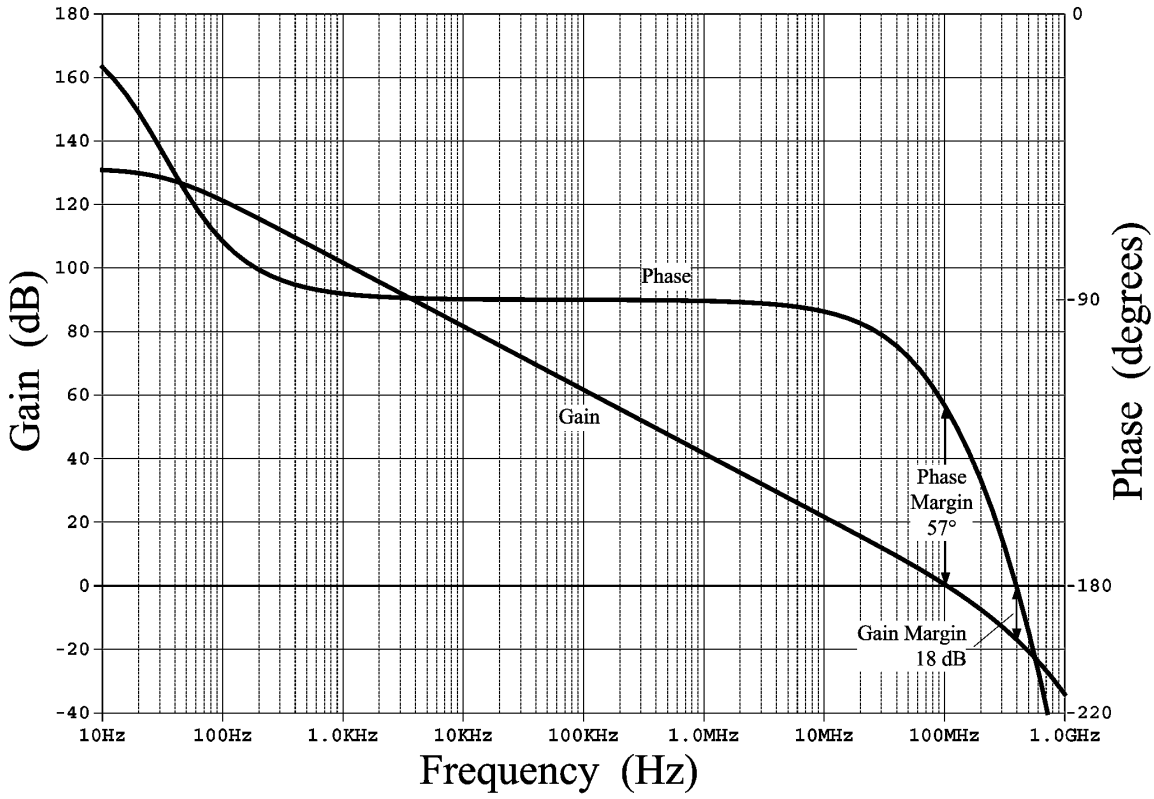

Figure 5-13: OPA357 open loop gain/phase plot using SPICE.

The open loop gain/phase plot of Figure 5-13 generated by SPICE closely matches the open loop gain/phase plot of the OPA357's datasheet shown in Figure 5-11. If the gain/phase plots did not match, then a more accuracy OPA357 SPICE model would need to be created. The gain and phase margins from the SPICE simulation is 18 dB and 57° respectively. The step response plot for the OPA357 voltage follower generated by SPICE is shown in Figure 5-14.

The output voltage is fairly settled within 30 ns. The overshoot for the step response is around 12% as shown in Figure 5-14. This is very close to the value obtained from Figure 5-7 considering a phase margin of 57°. A SPICE generated plot of the output error of the OPA357 voltage follower is shown in Figure 5-15.

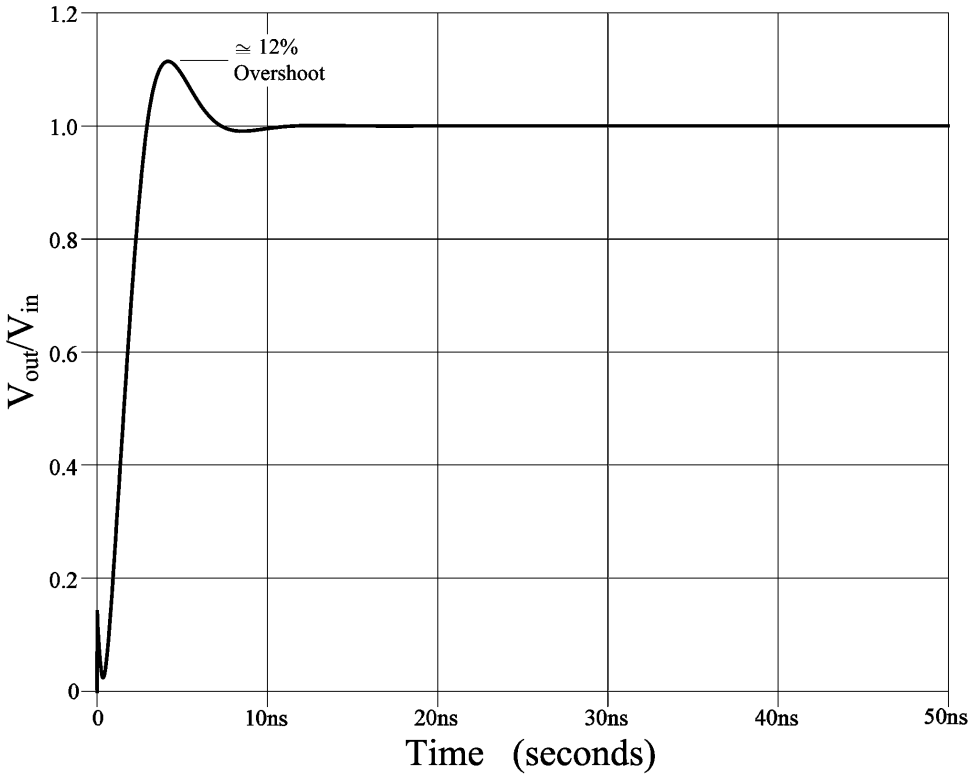

Figure 5-14: Step response for OPA357 voltage follower using SPICE.

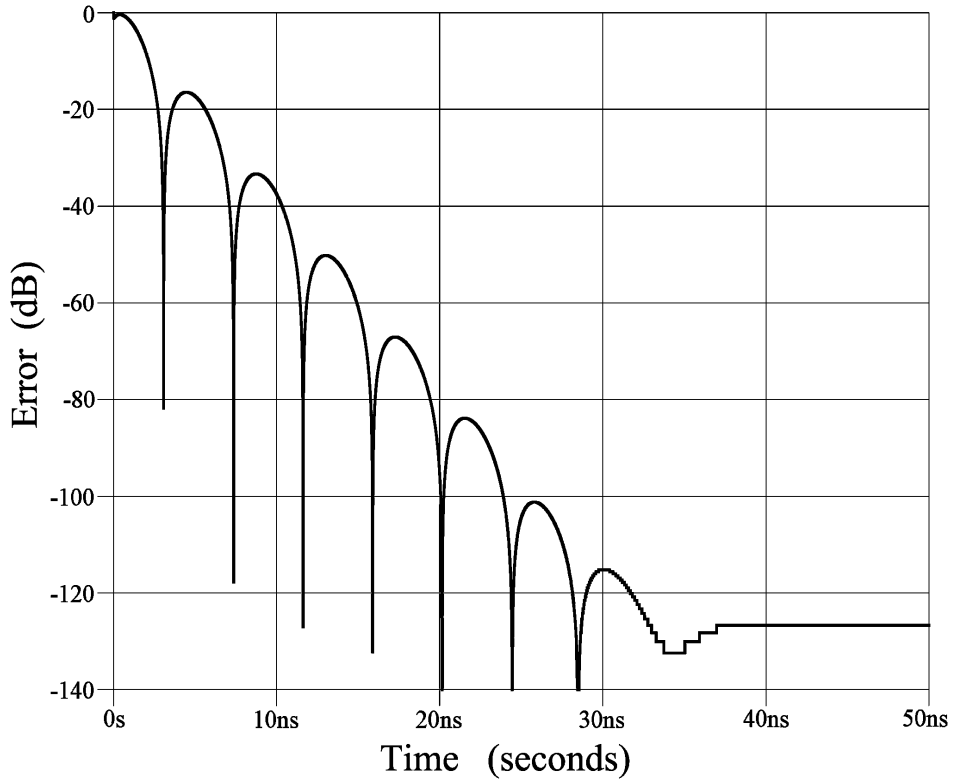

Figure 5-15: Settling time error for OPA357 voltage follower using SPICE.

Due to the "choppy" nature of the SPICE plot around 33 ns, the SPICE results below –125 dB are questionable (this is near the accuracy limit of the SPICE program). The actual error after the settling has occurred is equal to:

$$\text{Error} = 1 - \frac{V_o}{V_i} = \lim_{j\omega \to 0}\left(1 - \frac{G(j\omega)}{1 + G(j\omega)}\right) = \lim_{j\omega \to 0}\left(\frac{1}{G(j\omega) + 1}\right). \qquad (5\text{-}6)$$

For large open loop gain (at low frequency), the error is approximately $1/G(j\omega \to 0)$. Therefore the error (in dB) after settling has occurred is equal to the negative of the low frequency open loop gain (in dB). Table 5-1 gives the relationship between the available open loop gain (in dB) and the error (after settling has occurred). To achieve accuracy better than 0.02% for the compensation operational amplifier circuitry, the available open loop gain must be at least 74 dB.

Gain (dB)	Error (%)
20	9.1 %
40	0.99%
60	0.1%
80	0.01%
100	0.001%
120	0.0001%

Table 5-1: Open loop gain versus error (%).

Another aspect of the OPA357 SPICE model to validate is the output impedance. The OPA357's datasheet provides a plot of the output impedance as a function of frequency as shown in Figure 5-16.

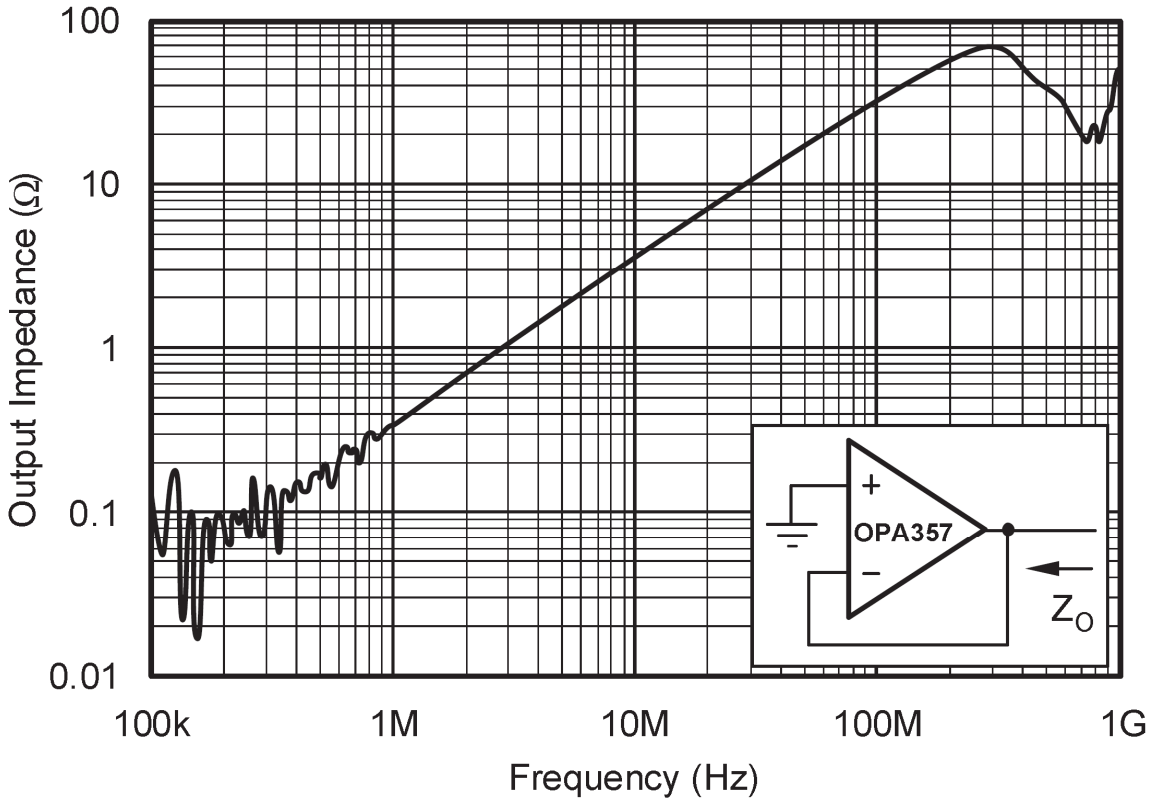

Figure 5-16: OPA357 datasheet output impedance versus frequency (Courtesy Texas Instruments).

It is important that the output impedance of the OPA357 SPICE model is consistent with the datasheet since the output impedance interacts with any circuitry connected to the operational amplifier output. The output impedance can also be determined from the SPICE model for the OPA357. The SPICE schematic for determining the output impedance of the OPA357 is shown in Figure 5-17. A small ac current (1 nA) is applied to the output of the voltage follower configuration and swept in frequency by the SPICE simulator.

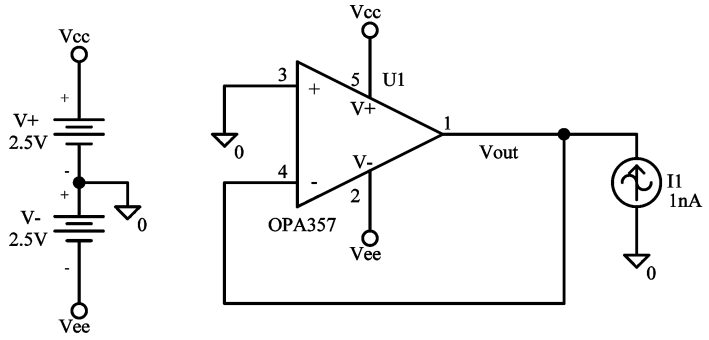

Figure 5-17: SPICE model schematic for generating OPA357 closed loop output impedance plot.

The output impedance can be calculated by dividing the output voltage simulated by SPICE by the 1 nA current source. A plot of the output impedance versus frequency is obtained using SPICE and shown in Figure 5-18. The SPICE simulated plot of Figure 5-18 is very similar to the OPA357 datasheet plot of Figure 5-16. Again, if these plots did not match, then a more accuracy OPA357 SPICE model would need to be created.

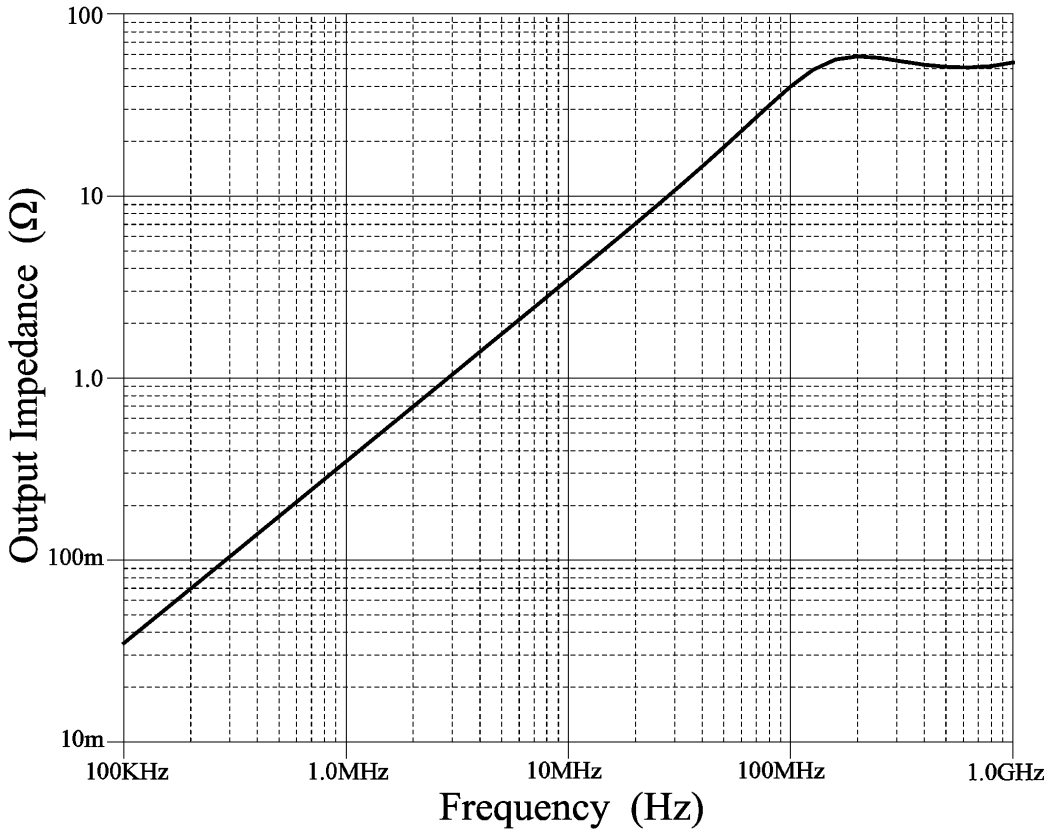

Figure 5-18: OPA357 closed loop output impedance plot using SPICE.

With the validation of the OPA357 SPICE model's output impedance, the effect of loading the voltage follower output with a resistive load can be determined. The SPICE schematic of Figure 5-19 is used to vary the output load resistor, R_Load.

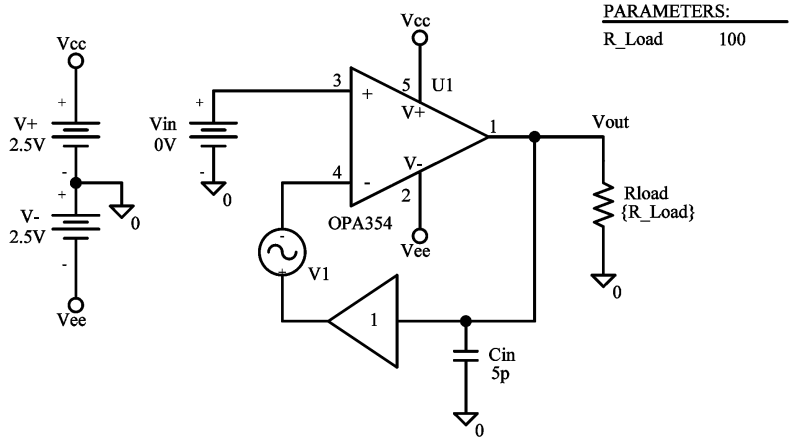

Figure 5-19: SPICE model schematic for generating gain/phase plot of OPA357 voltage follower with resistive output loading.

The output load resistor creates a divider network with the output impedance of the OPA357, causing an attenuation of the output voltage. The output load resistor somewhat affects the low frequency pole location of the OPA357. The effects of the output load resistor for values of 100 Ω, 10 Ω and 1 Ω, on the open loop gain/phase plot are shown in Figure 5-20.

The low frequency open loop gain is reduced to approximately 110 dB, 90 dB and 70 dB due to the output loading resistances of 100 Ω, 10 Ω, and 1 Ω respectively. The reduced gain impacts the accuracy of the voltage follower after settling has occurred as shown in Figure 5-21. The error (after settling) is approximately –110 dB, –90 dB and –70 dB for the loading resistances of 100 Ω, 10 Ω and 1 Ω respectively. The error (in dB) is the negative of the available open loop gain (in dB).

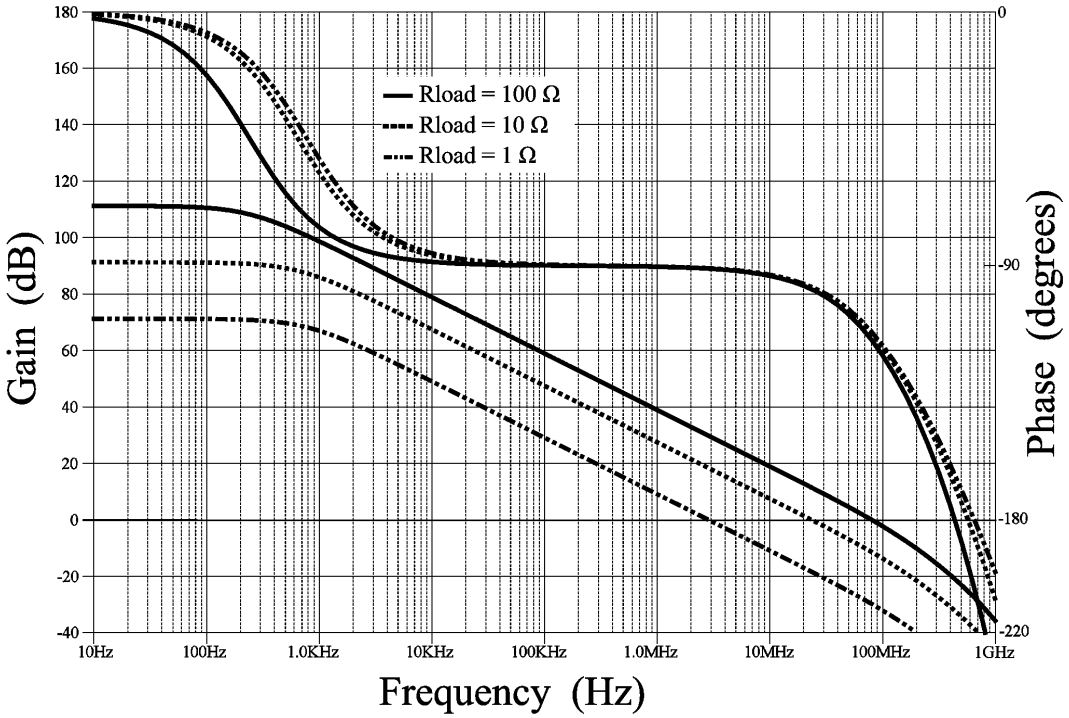

Figure 5-20: OPA357 voltage follower with resistive output loading open loop gain/phase plot using SPICE.

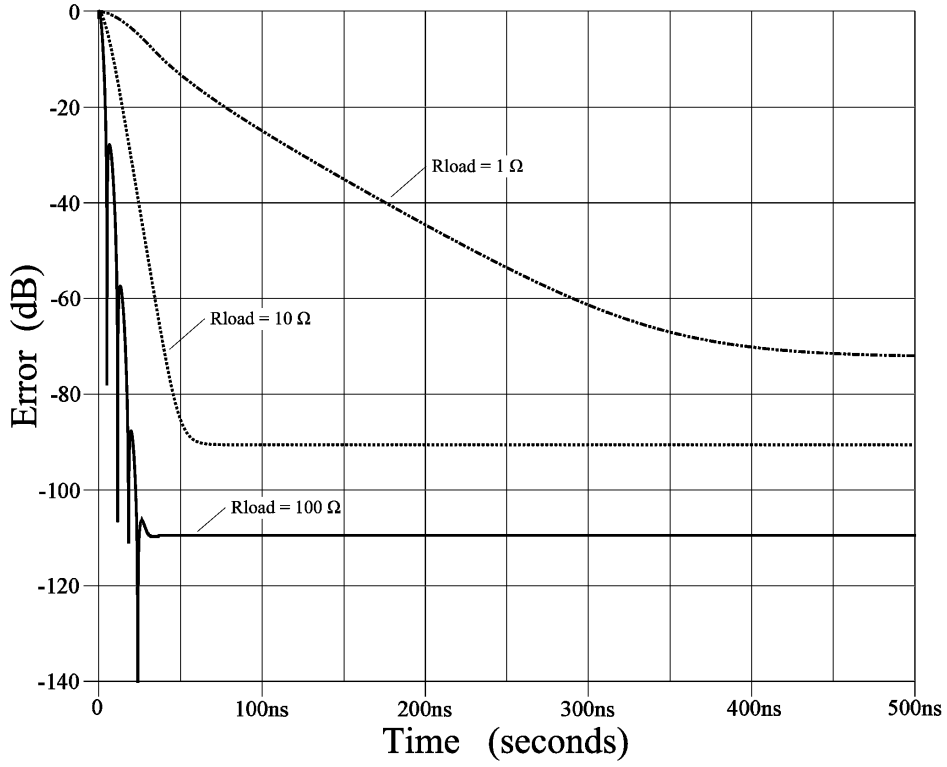

Figure 5-21: OPA357 voltage follower with resistive output loading settling time error using SPICE.

5.4 Lead/Lag Compensation with an Operational Amplifier

A common issue with operational amplifier circuits is created by a delay in the feedback path (or introduction of another pole) due to the parasitic input capacitance of the operational amplifier. A resistance, R_f, in the feedback path of the voltage follower illustrates this issue (SPICE schematic shown in Figure 5-22).

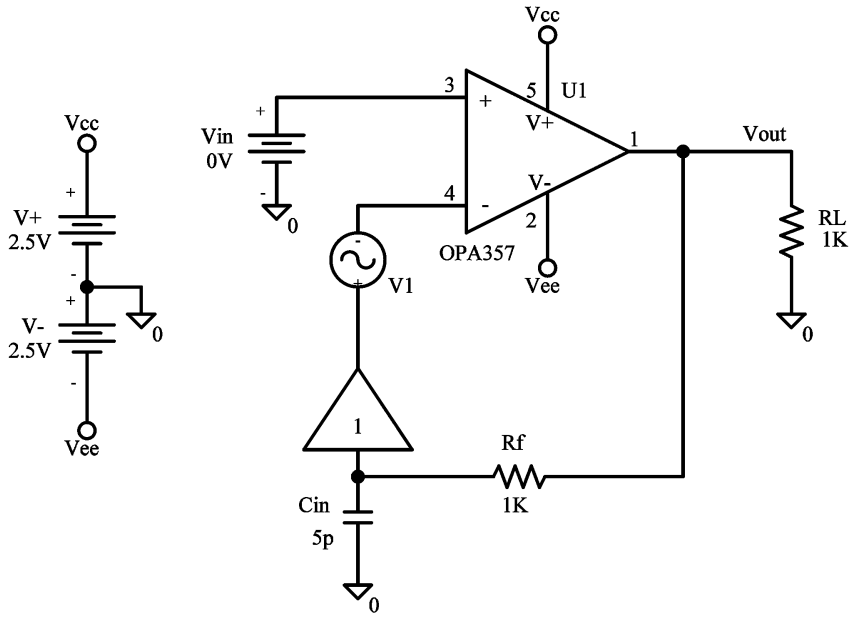

Figure 5-22: SPICE model schematic for generating gain/phase plot of OPA357 voltage follower with feedback resistance.

The resistance, R_f, and parasitic input capacitance, C_{in}, form a pole that has a corner frequency around the unity gain frequency of the OPA357. This additional pole reduces the open loop gain and phase margin as illustrated in Figure 5-23.

With the phase margin reduced to 12°, the voltage follower circuit is close to marginal stablility. The output voltage response to a step input has significant overshoot as shown in Figure 5-24.

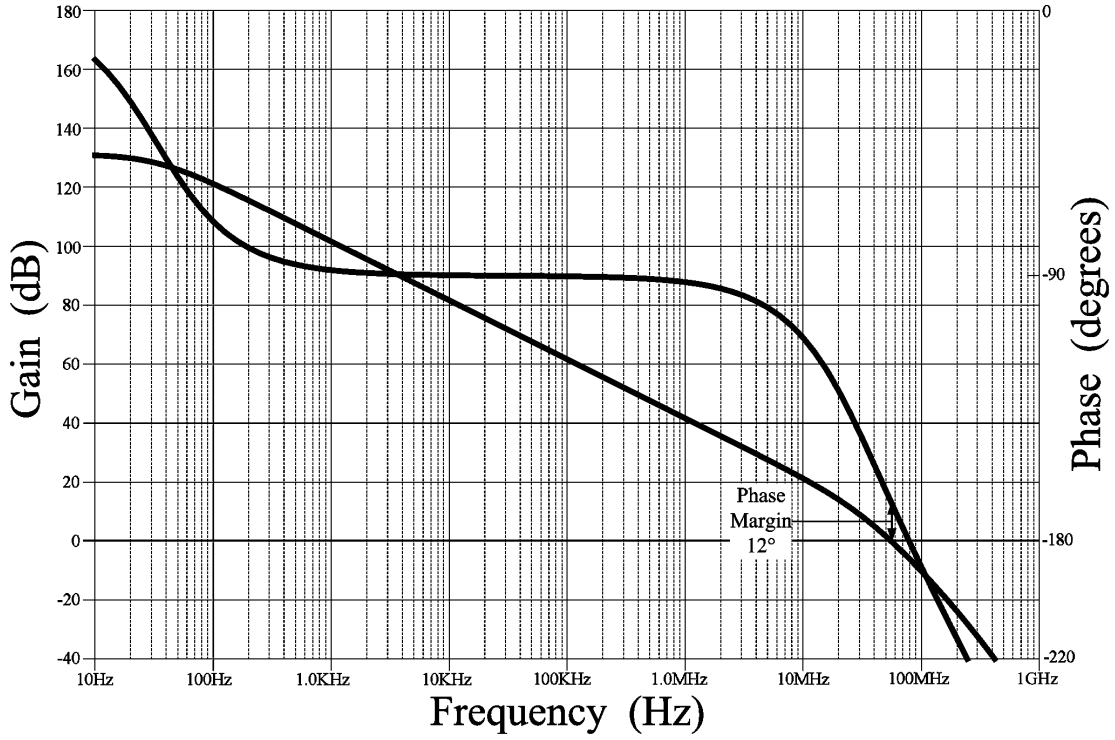

Figure 5-23: OPA357 voltage follower with feedback resistance open loop gain/phase plot using SPICE.

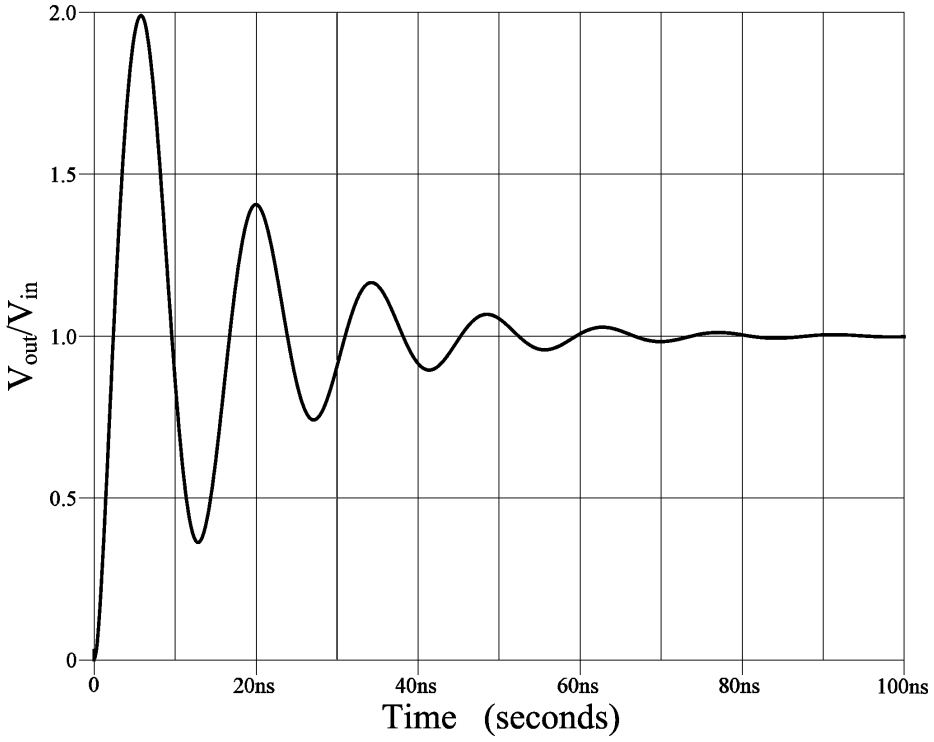

Figure 5-24: Step response for OPA357 voltage follower with feedback resistance using SPICE.

A classic approach to improving the phase margin (i.e. stability) of a voltage follower circuit (having noticeable feedback resistance) is to add a lead/lag compensation network. The lead/lag compensation network is a resistor, R_c, and capacitor, C_c, in series place across the input pins of the operational amplifier as shown in Figure 5-25.

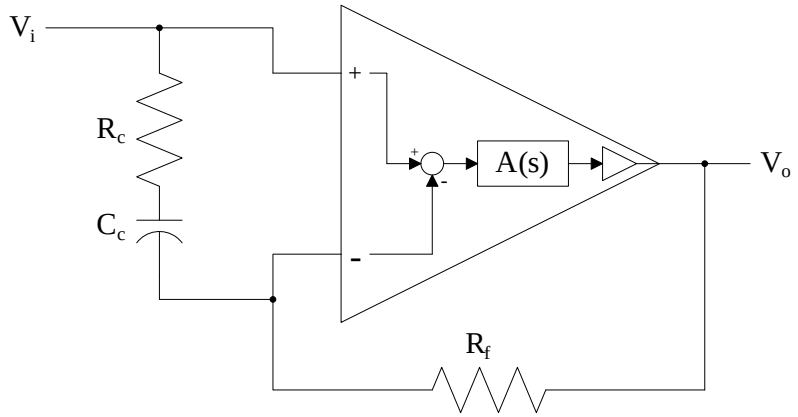

Figure 5-25: Classic operational amplifier lead/lag compensation.

The transfer function, for Figure 5-25, is obtained analytically (ignoring the operational amplifier input capacitance, C_{in}, and output impedance):

$$\frac{V_o}{V_i} = \frac{A(s)\dfrac{R_c}{R_c + R_f}\dfrac{\left(s + \dfrac{1}{R_c C_c}\right)}{\left(s + \dfrac{1}{(R_c + R_f)C_c}\right)}}{1 + A(s)\dfrac{R_c}{R_c + R_f}\dfrac{\left(s + \dfrac{1}{R_c C_c}\right)}{\left(s + \dfrac{1}{(R_c + R_f)C_c}\right)}}. \qquad (5\text{-}7)$$

The additional compensation resistor, R_c, and capacitor, C_c, add a zero [corner frequency at $1/2\pi R_c C_c$] and a pole [corner frequency at $1/2\pi(R_c + R_f)C_c$] to the open loop transfer function [numerator of (5-7)]. The corner frequency of the pole is always lower

than the corner frequency of the zero with both corner frequencies typically chosen to be below the unity gain frequency.

The actual transfer function also includes the interaction of the operational amplifier's input capacitance, C_{in}, and output impedance with the rest of the circuitry. The open loop gain is easily plotted using the SPICE model schematic of Figure 5-26.

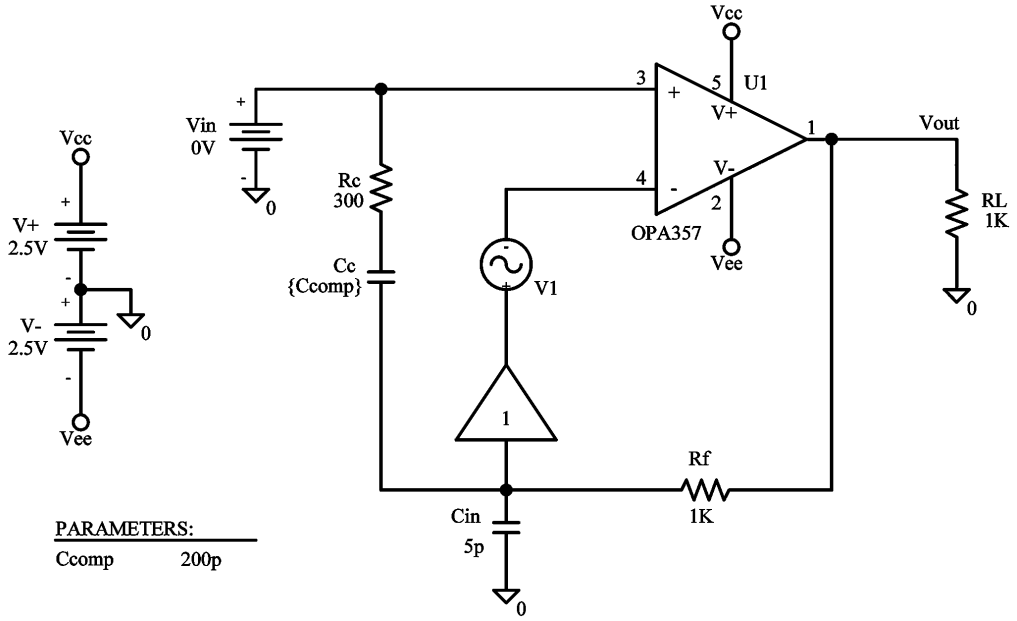

Figure 5-26: SPICE model schematic for OPA357 voltage follower with lead/lag compensation.

Figure 5-27 shows the open loop gain/phase plot for the voltage follower with lead/lag compensation and with no compensation. The additional lead/lag compensation resistor and capacitor improves the phase margin from 12° to 50°.

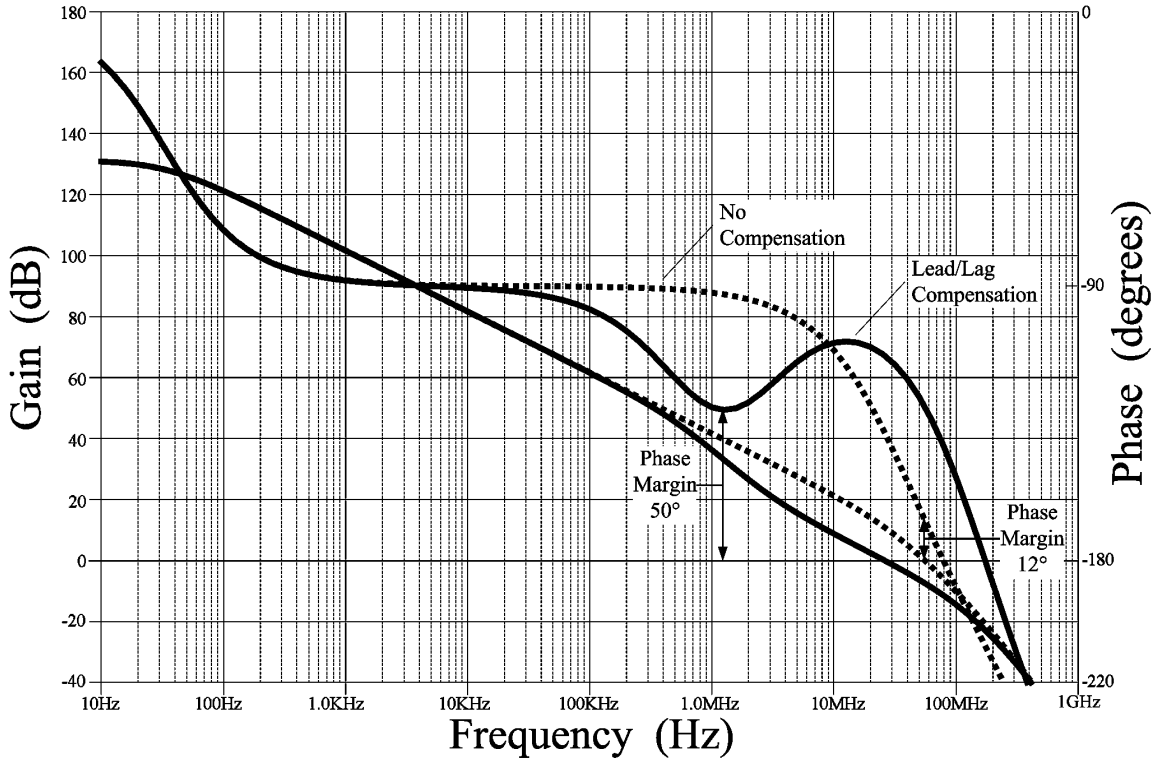

Figure 5-27: OPA357 voltage follower with lead/lag compensation open loop gain/phase plot using SPICE.

The corner frequency of the added pole is 612 kHz and the corner frequency of the added zero is 2.65 MHz. As shown in Figure 5-27, the lead/lag compensation open loop gain is attenuated (compared to no compensation) above the corner frequency for the pole. Additionally, the frequency at which the lead/lag compensation open loop phase passes through –180° is moved to a higher frequency (again compared to no compensation). The lead/lag compensation substantially increases the phase margin (at the unity gain frequency) from 12° to around 70°.

It is extremely important that the compensation capacitor, C_c, maintains its capacitive impedance for frequencies through 100 MHz (since the application of the lead/lag compensation is addressing gain and phase margin concerns around 80 MHz). The frequency response of typical SMT (surface mount technology) capacitors is shown in

Figure 5-28 [19]. The only capacitors suitable for C_c are the COG dielectric with the 0805 or 0603 package sizes.

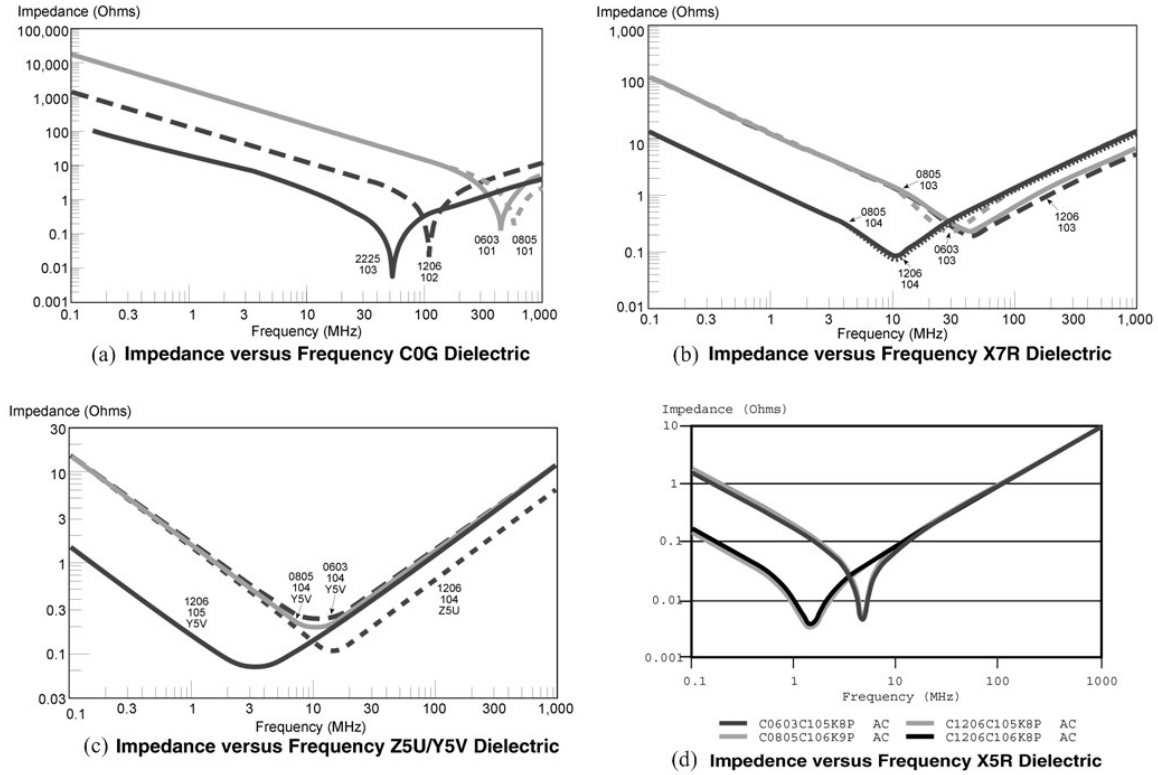

Figure 5-28: SMT (Surface Mount Technology) capacitor frequency response (Courtesy Kemet Electronics Corporation).

The step response for the OPA357 voltage follower with lead/lag compensation is shown in Figure 5-29. The amount of overshoot is significantly less for the lead/lag compensation voltage follower circuit compared to the circuit with no compensation.

The lead/lag compensation network approximately doubles the settling time as shown in Figure 5-30. This is typical of the trade-off between overshoot and settling (decreased overshoot is achieved at the expense of increased settling time).

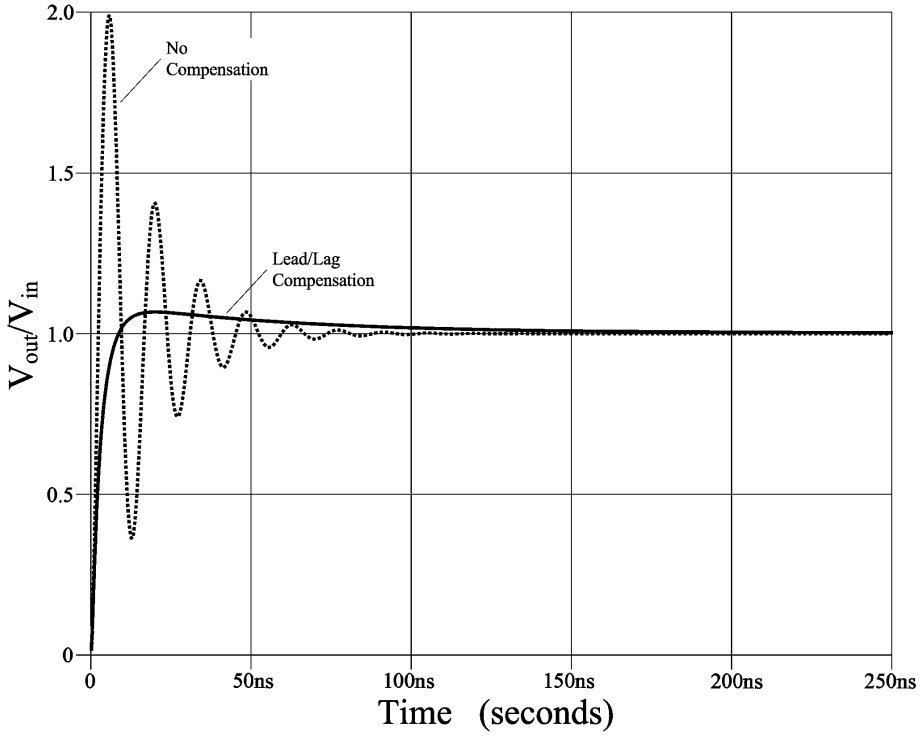

Figure 5-29: Step response for OPA357 voltage follower with lead/lag compensation using SPICE.

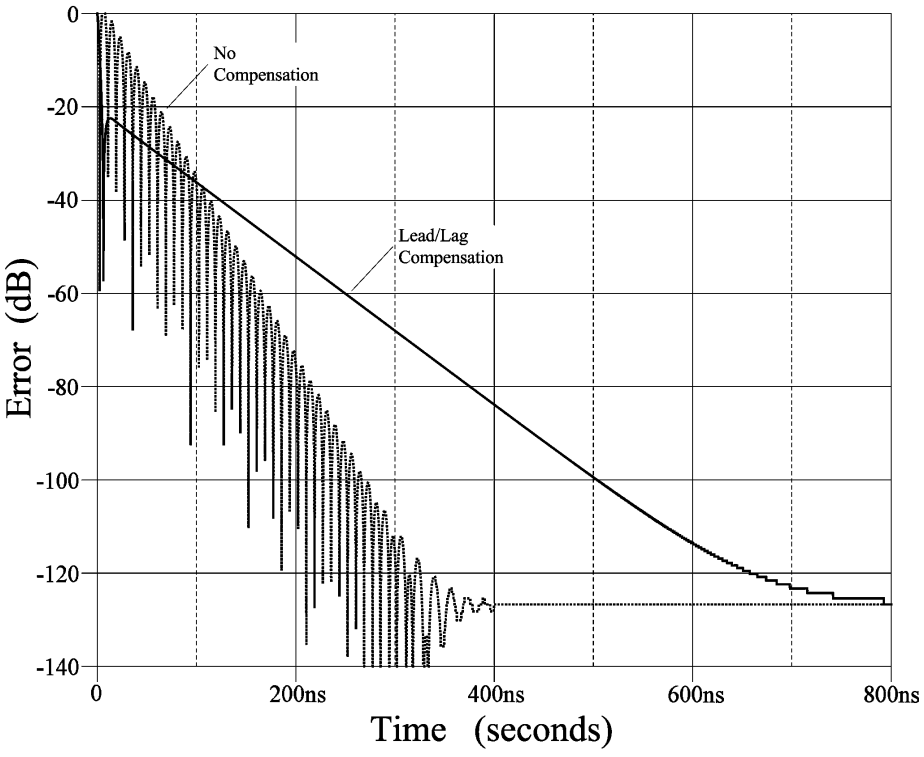

Figure 5-30: OPA357 voltage follower with lead/lag compensation settling time error using SPICE.

Lead/lag compensation is an effective way of improving the gain and phase margin of an operational amplifier circuit. As shown in section 5.5.4, this compensation is applied to the compensation operational amplifier circuit to improve the overall gain and phase margin.

5.5 SPICE Modeling and Improving the Compensation Operational Amplifier Circuitry

The previous sections provided some foundations and key components to analyzing the stability, settling, and accuracy of a operational amplifier control circuit using SPICE. These techniques are now applied to the compensation operational amplifier circuitry driving the isolation transformer.

The design challenges and design progression of the compensation operational amplifier circuitry are presented in the following sub-sections. The method chosen to convey the need and design of the drive amplifier circuit, snubber/output filter network, lag compensation network and lead compensation network blocks (of Figure 2-1) is to 1) analyze the compensation operational amplifier circuitry without these blocks; 2) identify the issues/problems with stability, settling, and accuracy; and 3) introduce these blocks as an adequate solution/improvement to these issues/problems.

5.5.1 *SPICE results of Compensation Operational Amplifier With Isolation Transformer*

The isolation transformer SPICE model of Figure 4-10 is combined with the SPICE model of the OPA357 operational amplifier in the conceptual circuit configuration of Figure 1-6. The SPICE schematic for the OPA357 and isolation transformer used for generating the open loop gain/phase plot is shown in Figure 5-31.

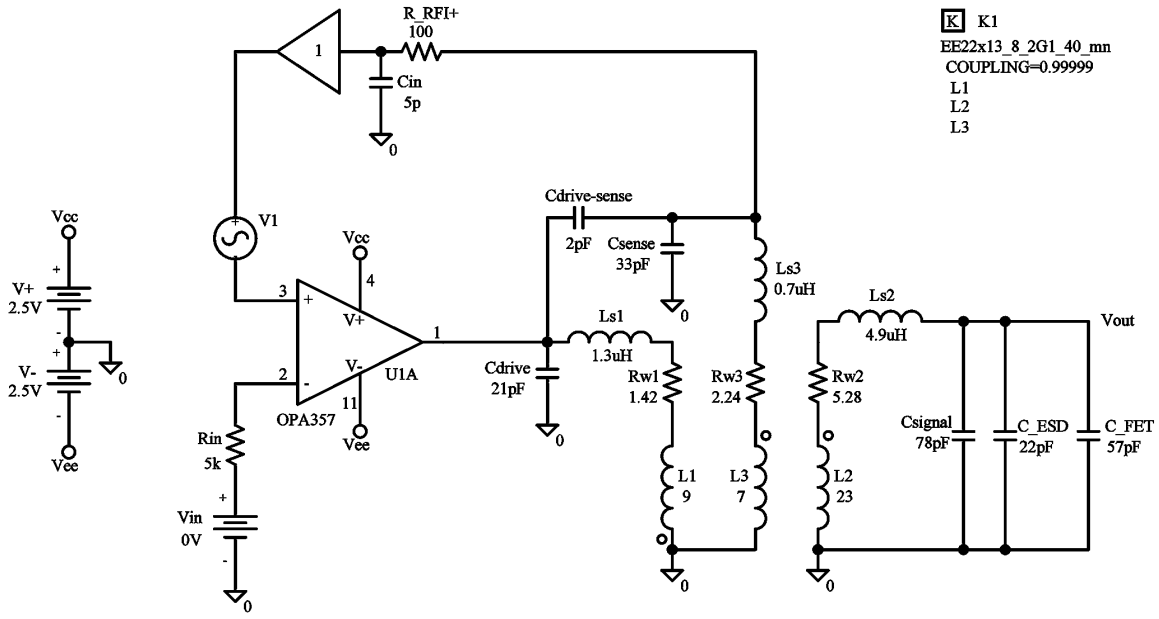

Figure 5-31: SPICE model schematic for OPA357 compensation operational amplifier with isolation transformer.

The open loop gain/phase plot for the circuitry of Figure 5-31 is shown in Figure 5-32. From a stability standpoint, there are four issues identified from the open loop gain/phase plot: 1) at low frequencies, the gain drops below unity (0 dB) when the phase is very near 180° (i.e. no phase margin); 2) at about 3 MHz, the phase passes through –180° with around 20 dB of available gain (i.e. no gain margin); 3) at about 5 MHz, the gain drops below 0 dB and the phase is transitioning through –180° (i.e. no gain or phase margin); and 4) at around 25 MHz, the phase passes through –180° with around 20 dB of available gain (i.e. no gain margin).

Issue 1) is not a problem for this system. Since the compensation operational amplifier is only enabled for at most 15 μs, the marginal instability at low frequency does not have enough time to be realized. The remaining three issues are serious problems that are addressed in the subsequent sections.

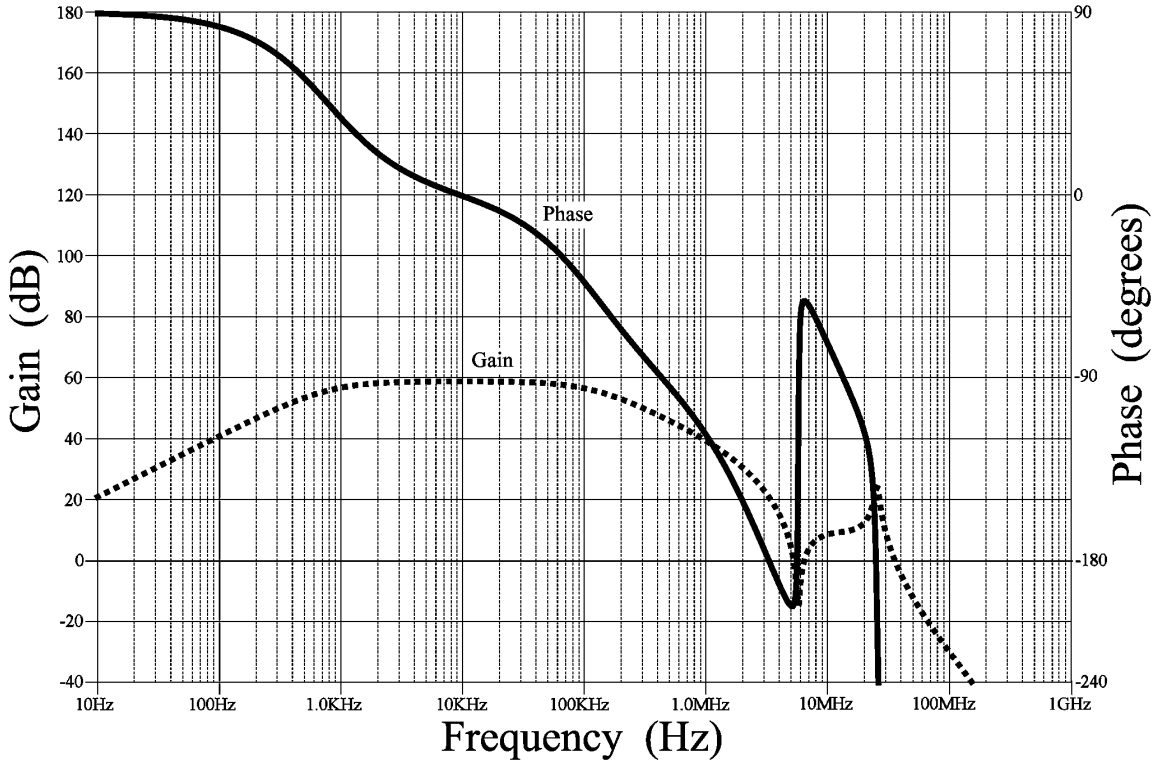

Figure 5-32: OPA357 compensation operational amplifier with isolation transformer open loop gain/phase plot using SPICE.

From an accuracy standpoint, there is a problem with the available open loop gain. As shown in Figure 5-32, the gain peaks at slightly less than 60 dB. Therefore, even if there were no stability issues, the accuracy of the circuit is worse than 0.1% (see Table 5-1). This accuracy issue is addressed in the next section.

5.5.2 *Driving the Magnetizing Inductance of the Isolation Transformer*

The OPA357 operational amplifier of Figure 5-31 drives the magnetizing inductance of the E-E core through the printed circuit board winding resistance. In essence, this R-L circuit is a high-pass filter in the closed loop of the compensation operational amplifier circuit. It is this R-L interaction that limits the available open loop gain shown in Figure 5-32.

Analysis of the transfer function of this high-pass filter gives insight into how the R-L combination limits the available open loop gain. The simple R-L high pass filter can be analyzed in SPICE using the circuit of Figure 5-33. The inductance value, L = 125 μH represents the lower limit of the magnetizing inductance of the isolation transformer referred to the drive winding.

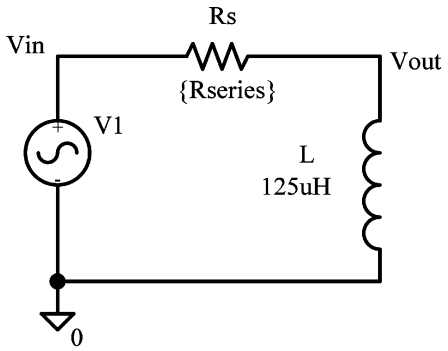

Figure 5-33: SPICE model schematic for resistor/inductor high-pass filter.

The resistor R_s is set to 1 Ω, 10 Ω, and 100 Ω and represents the possible combination of the drive winding resistance and output impedance of the operational amplifier. The Bode plots for this high-pass filter are shown in Figure 5-34. The high-pass filter has a corner frequency of $R_s/2\pi L$.

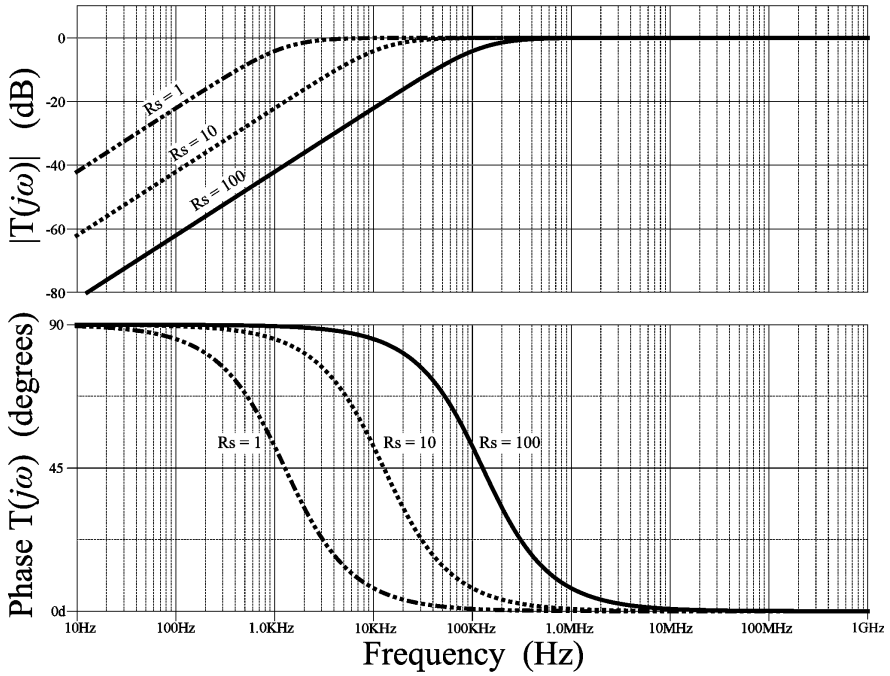

Figure 5-34: Transfer function Bode plots for resistor/inductor high-pass filter.

The high-pass, R-L filter is placed in the closed loop path of a voltage follower circuit using the OPA357 operational amplifier to observe the effect on the open loop gain. The SPICE model for the combination of the OPA357 voltage follower and R-L filter (simulates magnetizing inductance of the isolation transformer) is shown in Figure 5-35.

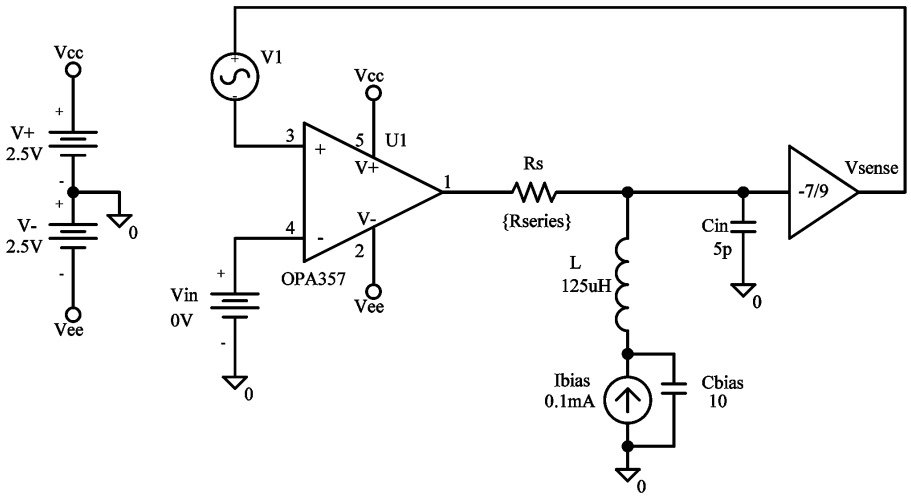

Figure 5-35: SPICE model schematic for OPA357 driving the magnetizing inductance of the isolation transformer.

The purpose of the bias current, Ibias, and bias capacitor, Cbias, is to define the OPA357 bias output voltage/current used for the SPICE simulation during the frequency sweep. SPICE determines all the dc voltages and currents of the circuit before it performs the frequency sweep. Without the bias current or bias capacitor, Vsense = 0 V since the dc voltage across the ideal inductor, L, is 0 V. The OPA357 SPICE model has a slight input offset voltage causing the OPA357 output voltage to be large (input offset voltage multiplied by dc open loop gain), and possibly at the power supply rail. The bias current, Ibias, establishes the OPA357 output current and the bias capacitor allows a small dc voltage to be established such that Vsense is approximately equal to the negative of the OPA357 SPICE model's input offset voltage.

The resulting open loop gain/phase plot is basically the combination of the open loop gain/phase plot for the OPA357 (Figure 5-13) with the high-pass transfer function of Figure 5-34 as shown in Figure 5-36. The open loop output impedance of the OPA357 is approximately 100 Ω at around 100 kHz. Hence, there is not much difference between the additional series resistance, R_s, of 1 Ω and 10 Ω.

The reduction in the available open loop gain reduces the accuracy after settling as portrayed in Figure 5-37. Again, the error (in dB) is the negative of the available open loop gain (in dB).

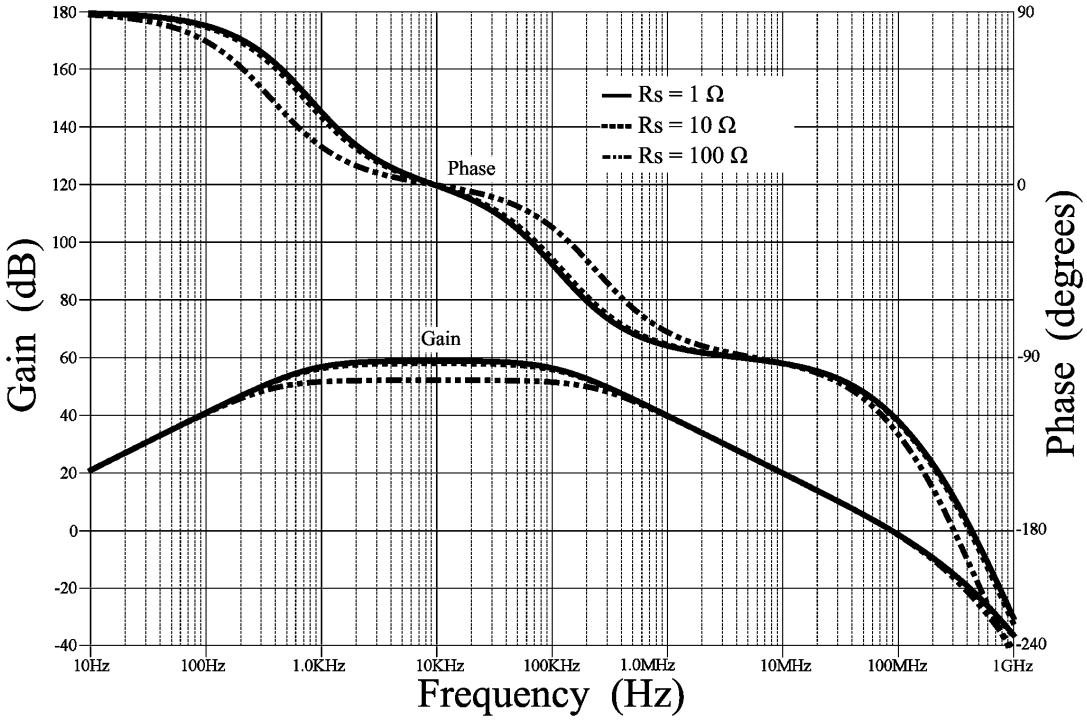

Figure 5-36: OPA357 driving the magnetizing inductance of the isolation transformer, open loop gain/phase plot using SPICE.

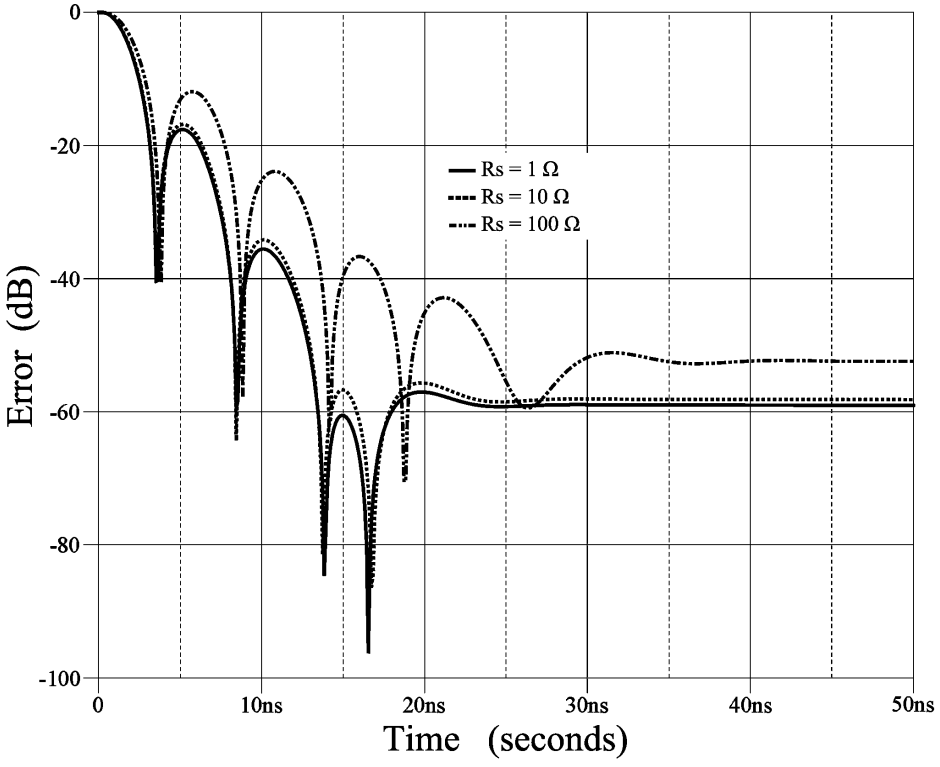

Figure 5-37: OPA357 driving the magnetizing inductance of the isolation transformer, settling time error using SPICE.

The available open loop gain can be improved by finding an operational amplifier with either increased gain-bandwidth product or reduced open loop output impedance. If an operational amplifier has an open loop gain of 80 dB at the corner frequency of the R-L high-pass filter (operational amplifier output impedance, series winding resistance and isolation transformer magnetizing inductance), then it can achieve 0.01 % accuracy.

The reduced open loop gain problem is solved cost effectively by adding a drive amplifier circuit to the output of the OPA357. This is easily accomplished with an NPN and PNP transistor ($.02), class B push-pull amplifier stage with a bias resistor. The bias resistor is pulled high or low depending on the polarity of the LPF output voltage at the time the enable signal is activated (in turn, biasing the appropriate NPN or PNP transistor in its active region). A SPICE model schematic for the circuit of Figure 5-31 with the additional class B amplifier stage is shown in Figure 5-38.

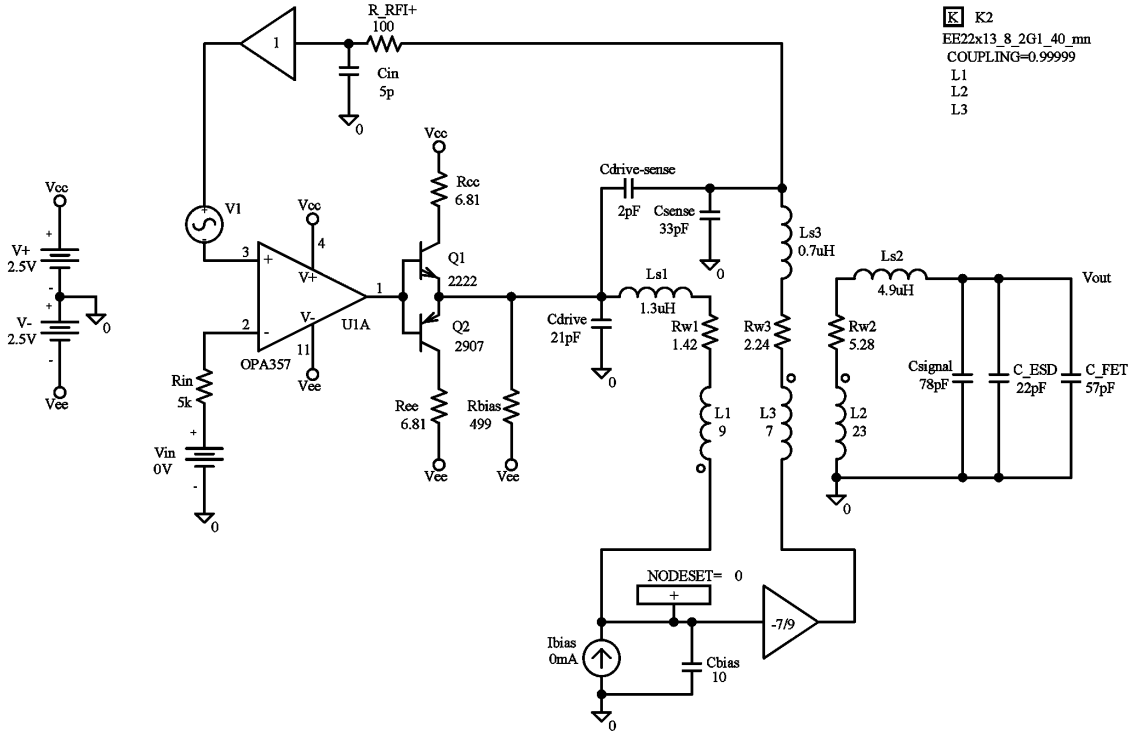

Figure 5-38: SPICE model schematic for OPA357 with class B push-pull drive amplifier stage.

The open loop gain/phase plot for the OPA357 with the class B push-pull drive amplifier circuit is shown in Figure 5-39. Since the output impedance of the drive amplifier circuit is small, the corner frequency of the R-L high-pass filter (winding resistance in combination with the magnetizing inductance) is at a lower frequency, where the available open loop gain is higher.

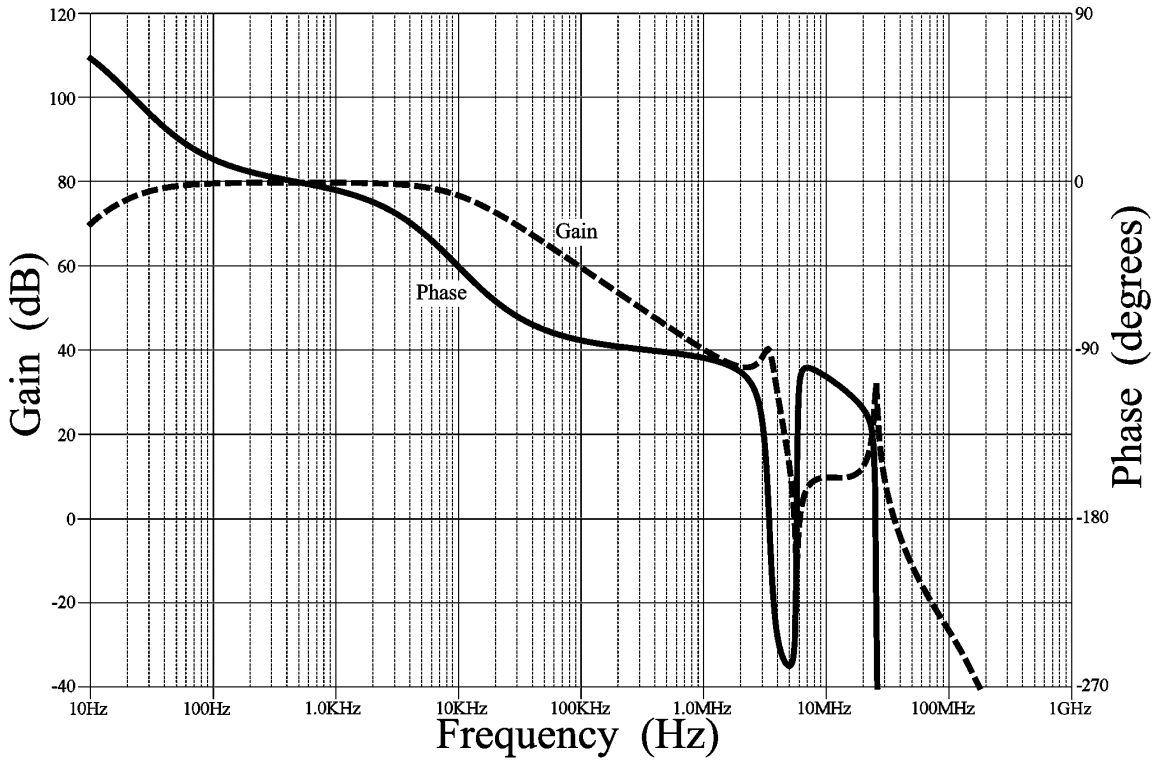

Figure 5-39: OPA357 with class B push-pull drive amplifier stage, open loop gain/phase plot using SPICE.

The added drive amplifier circuit changes the open loop gain/phase characteristic between 1 MHz and 10 MHz. However, there is still instability around 3 MHz and 5 MHz. This instability is addressed in the next section.

5.5.3 *De-Q'ing the Isolation Transformer's Parasitics*

The instabilities, around 3 MHz and 5 MHz of Figure 5-39, are the result of the parasitics (winding capacitance, winding resistance, and leakage inductance) of the

isolation transformer circuit. The parasitic circuitry is identified by removing the magnetizing inductance, and transferring the remaining circuit elements to the drive winding as shown in Figure 5-40.

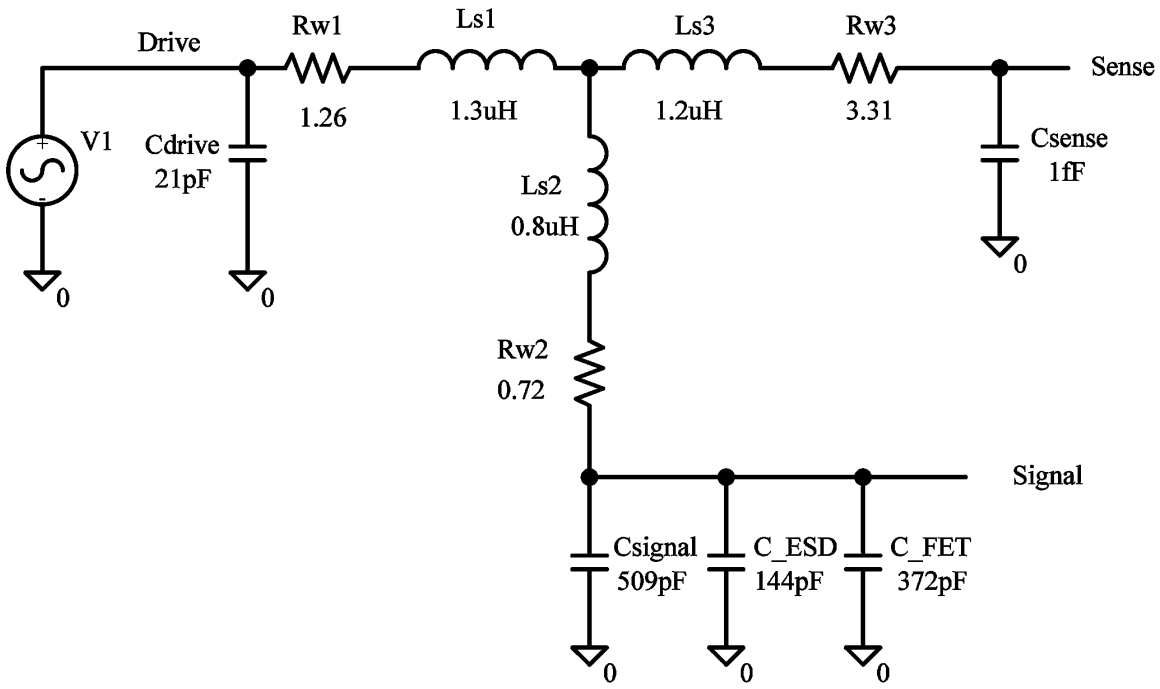

Figure 5-40: SPICE model schematic for the typical parasitics of isolation transformer circuit.

For the purposes of this analysis, the capacitance on the sense winding is set to an extremely low value. The drive node and sense nodes are in the closed loop path of the compensation operational amplifier circuit. Therefore, it makes sense to analyze the transfer function between the sense and drive nodes. The Bode plots for the drive to sense parasitic transfer function is given in Figure 5-41.

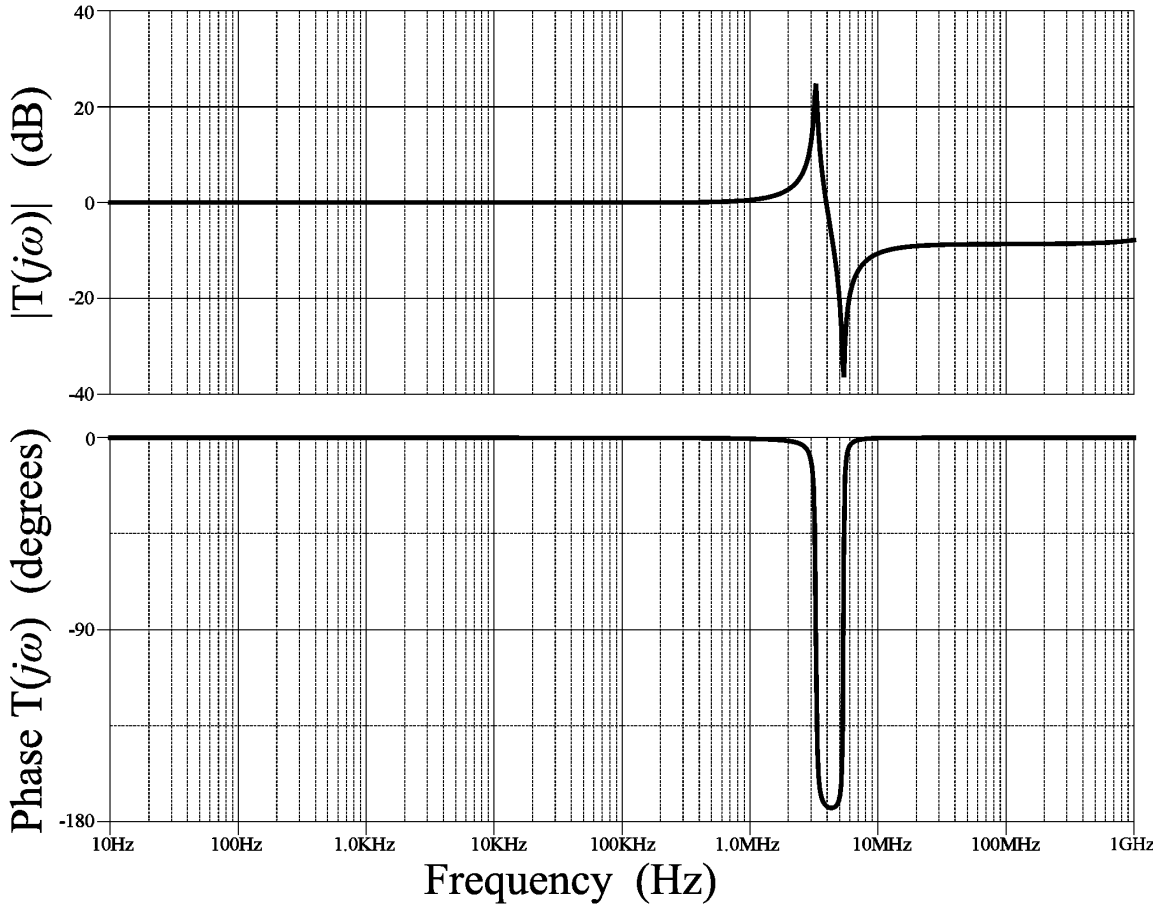

Figure 5-41: Drive to sense winding transfer function Bode plots for the typical parasitics of isolation transformer circuit.

This transfer function looks similar to the open loop gain/phase characteristic between 1 MHz and 10 MHz of Figure 5-39. Since the phase changes by almost –180 degrees around 3 MHz, there are two poles near this frequency. Since the phase changes by almost 180 degrees around 5 MHz, there are two zeroes near this frequency. These two poles and two zeroes are a result of the parasitic inductances and capacitances of Figure 5-40.

The two poles can be analyzed by looking at the transfer function between the drive and signal nodes (removing the elements connected to the sense node) as shown in Figure 5-42(a). These two poles have a high Q (quality factor) since the phase is abruptly

changing by –180 degrees. A way to de-Q a circuit, without drastically affecting its lower frequency performance, is to add an R-C snubber circuit as shown in Figure 5-42(b) [20].

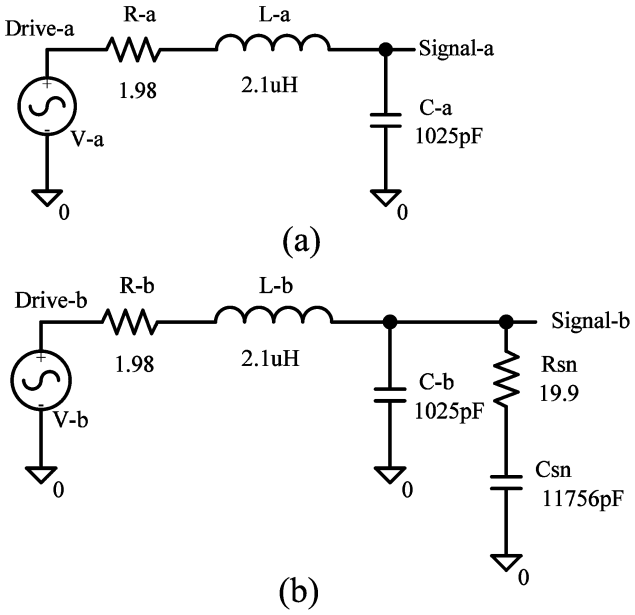

Figure 5-42: SPICE model schematic for: (a) transfer function between drive and signal nodes, and (b) transfer function between drive and signal nodes with additional R-C snubber.

The snubber capacitor, Csn, is chosen to be 3 to 10 times the existing node capacitance, C-a or C-b. The snubber resistor, Rsn, is chosen to appropriately reduce the Q of the circuit. The snubber resistor value, Rsn = 19.9 Ω, and snubber capacitor value, Csn = 11756 pF, reduce the Q from around 24.7 to approximately 0.4. The Bode plots for the transfer function between the drive and signal nodes (with and without the R-C snubber) are shown in Figure 5-43.

A SPICE model schematic for the typical parasitics of the isolation transformer circuit with additional R-C snubber is shown in Figure 5-44. The R-C snubber also impacts the settling time of the circuit and therefore may not be optimally selected for stability.

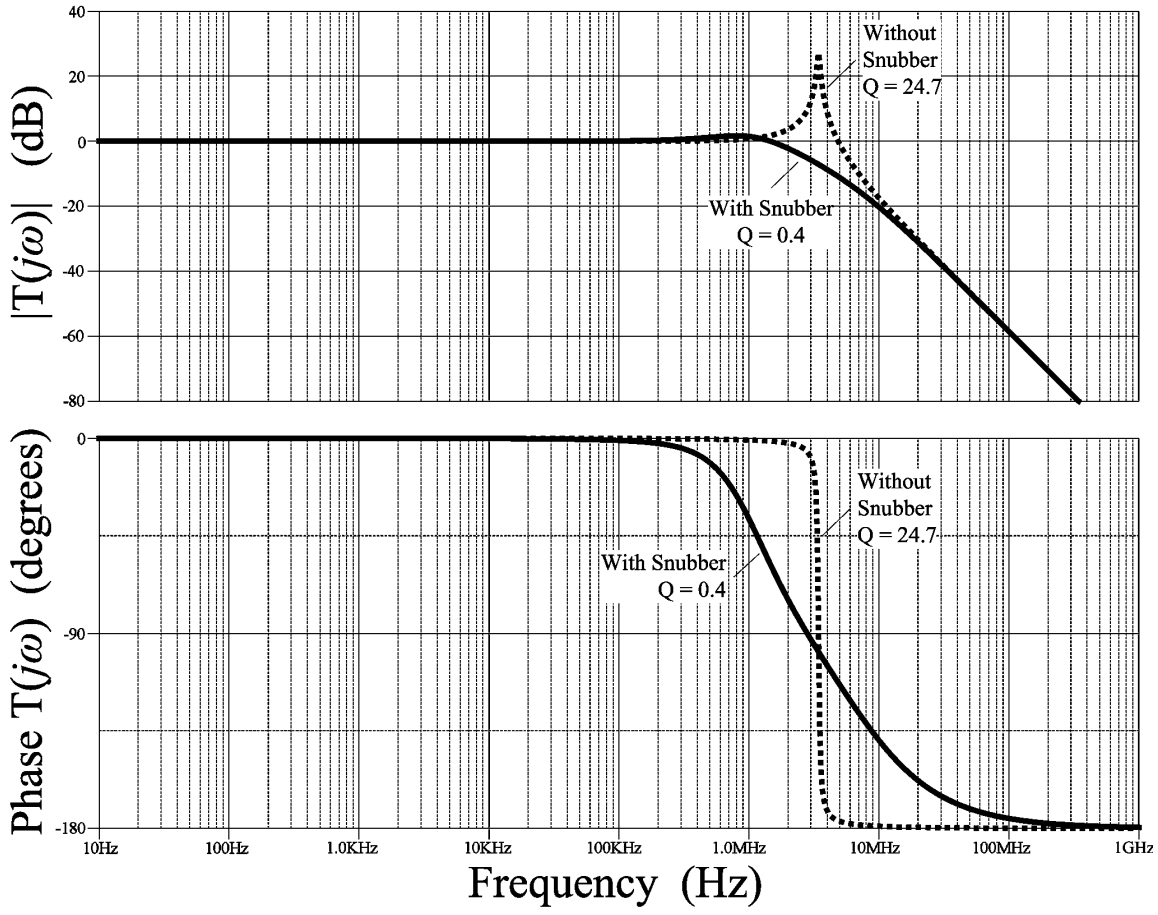

Figure 5-43: Transfer function Bode plots for additional R-C snubber.

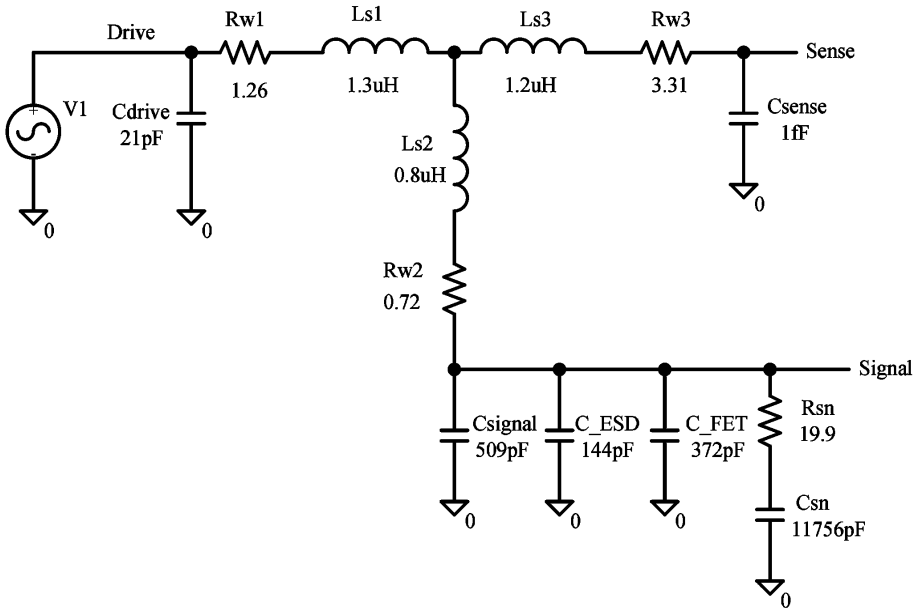

Figure 5-44: SPICE model schematic for the typical parasitics of isolation transformer circuit with additional R-C snubber.

The Bode plots for the drive to sense parasitic transfer function with and without the additional R-C snubber is given in Figure 5-45. For the purposes of this analysis, the capacitance on the sense winding is set to an extremely low value.

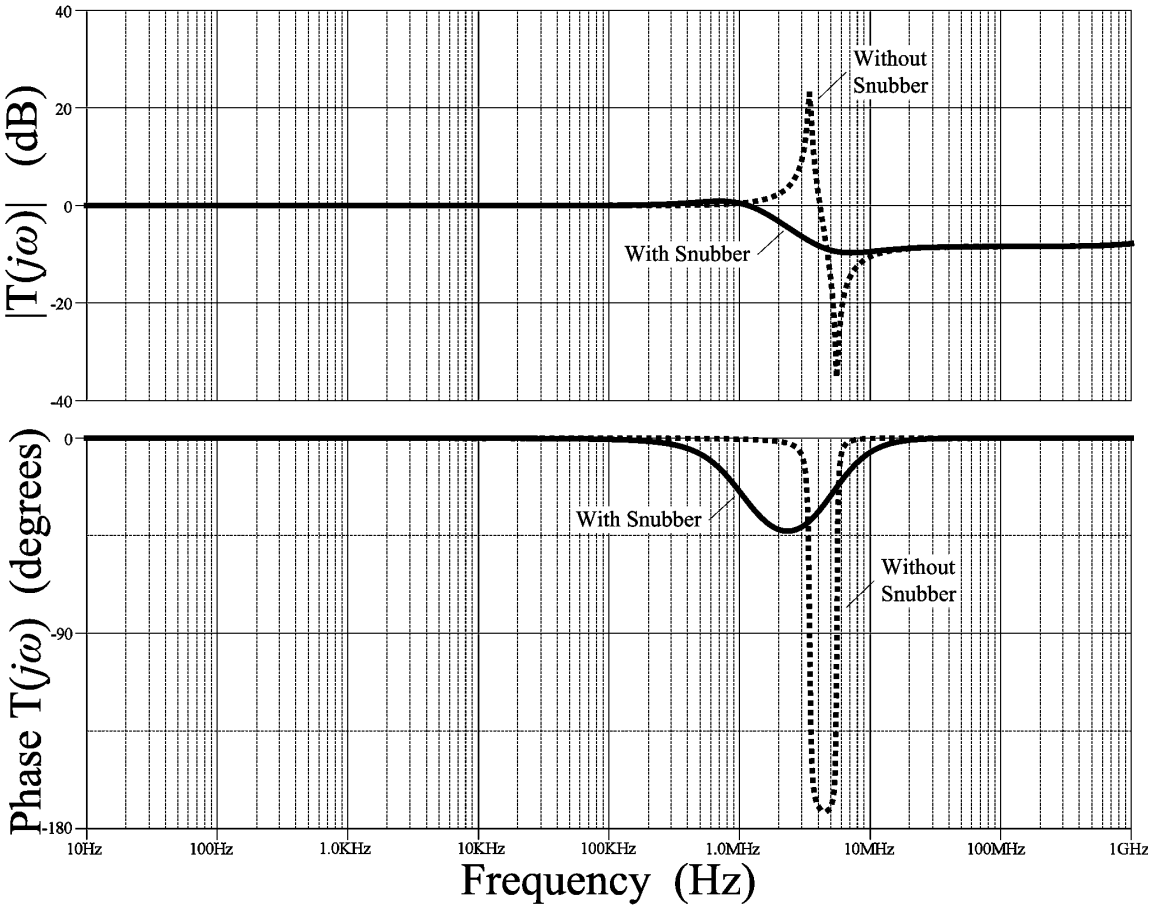

Figure 5-45: Transfer function Bode plots for typical parasitic of isolation transformer circuit with additional snubber.

The R-C snubber is now applied to the compensation operational amplifier circuitry of Figure 5-38. The SPICE model schematic with the added R-C snubber is shown in Figure 5-46. The R-C snubber is also used as an output filter by selecting the snubber capacitor voltage as the output signal, Vout.

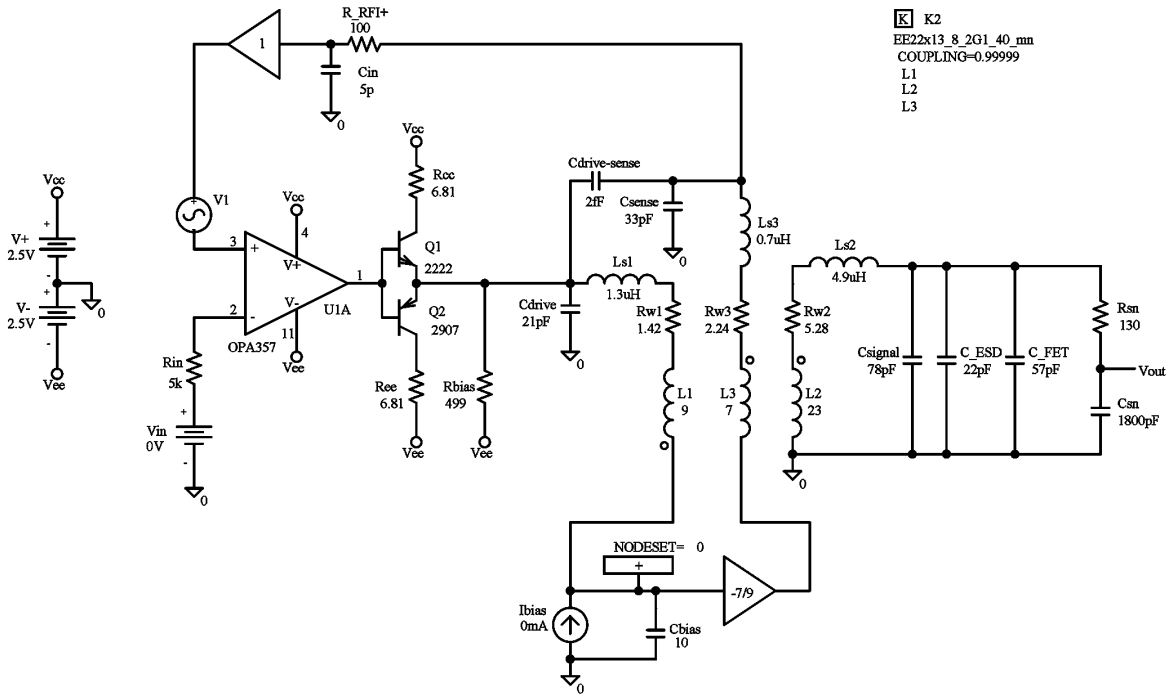

Figure 5-46: SPICE model schematic for OPA357 circuit with R-C snubber/output filter.

The open loop gain/phase plot for the OPA357 circuit with the R-C snubber/output filter is shown in Figure 5-47. The only remaining issue is the instability around 25 MHz, and is addressed in the next section.

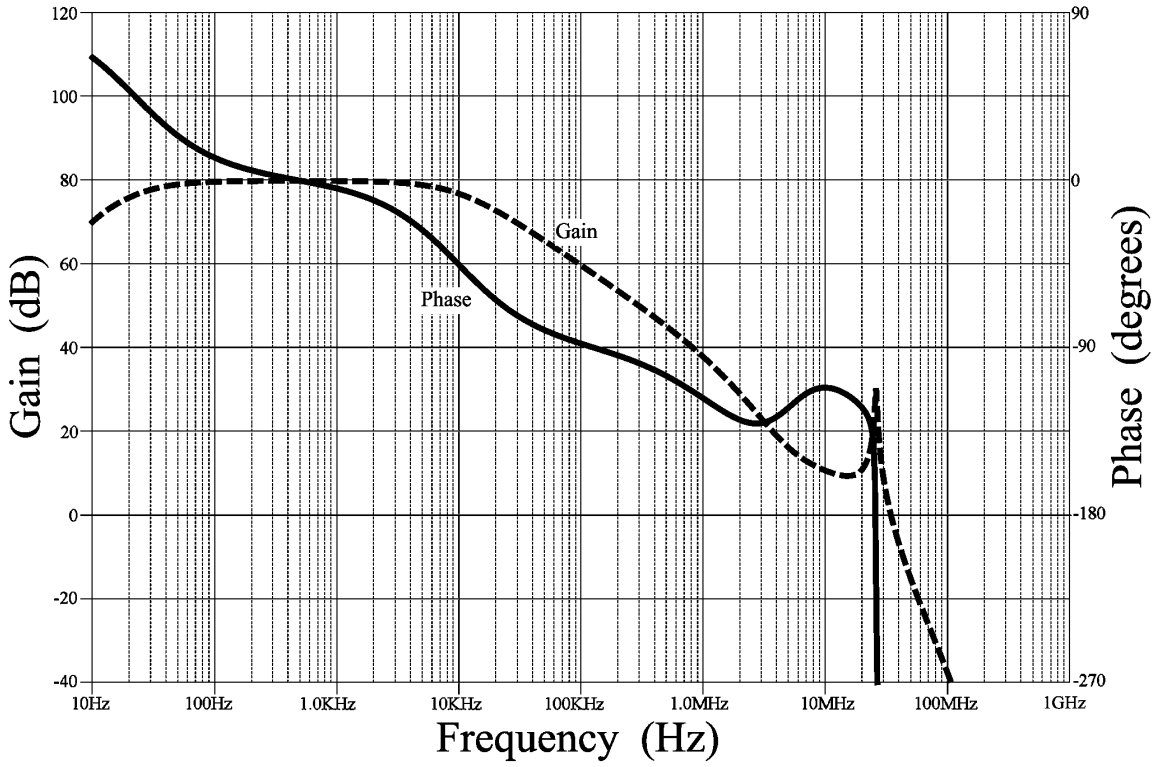

Figure 5-47: OPA357 circuit with snubber/output filter, open loop gain/phase plot using SPICE.

5.5.4 *Lead/ Lag Compensation*

The last issue remaining is the instability around 25 MHz shown in Figure 5-47. This instability can be resolved by applying the lead/lag compensation technique. The optimal placement of the lag compensation (in the feedback path from the sense winding) is at a frequency of around 7.2 MHz. The lead compensation is achieved by adding a 4 pF feedback capacitor at the output of the BJT drive amplifier to the negative input node of the compensation operational amplifier as shown in Figure 5-48.

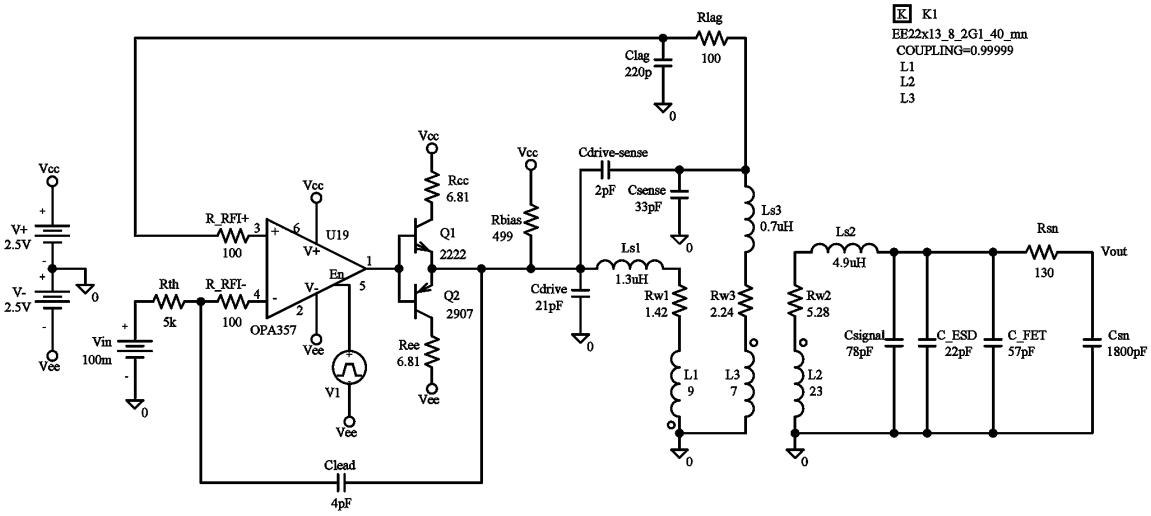

Figure 5-48: SPICE model schematic for OPA357 circuit with lead/lag compensation.

SPICE is used to maximize the phase margin by selecting the optimal values for the lead and lag resistors and capacitors. The open loop gain/phase plot for the SPICE model schematic of Figure 5-48 is given in Figure 5-49.

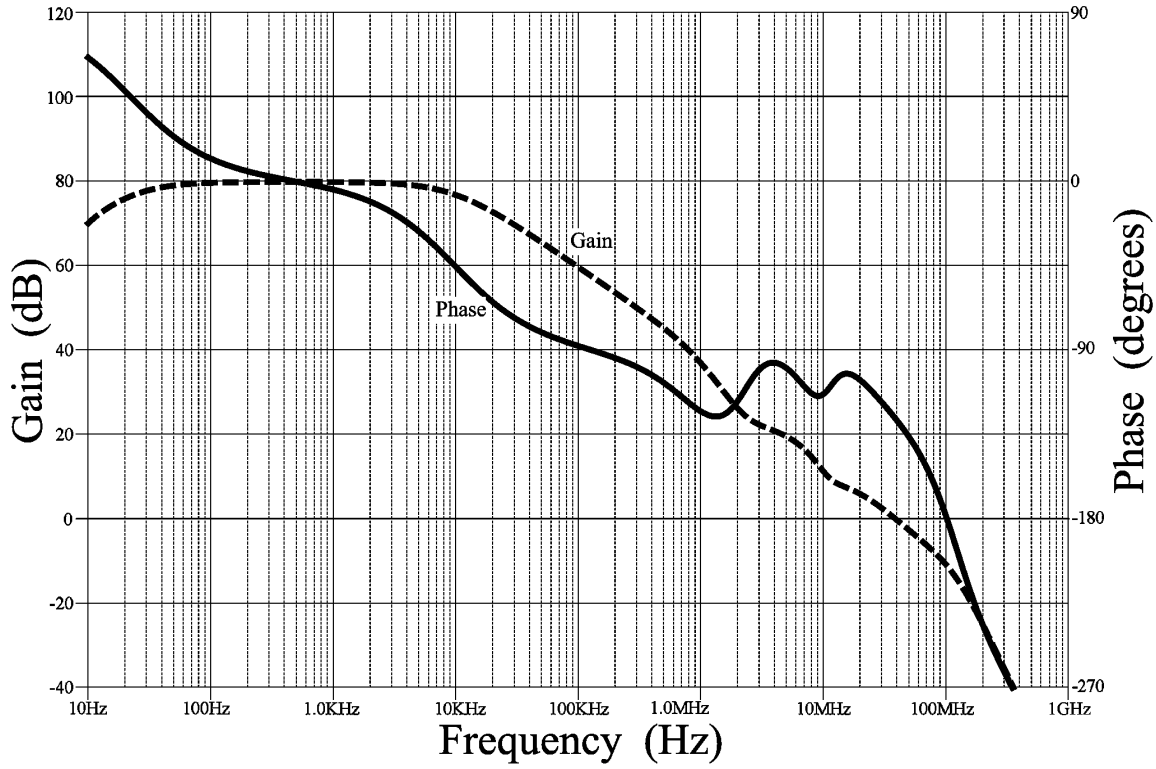

Figure 5-49: OPA357 circuit with lead/lag compensation, open loop gain/phase plot using SPICE.

The phase margin achieved with the lead/lag compensation is around 58°. It is important to verify that the accuracy is being met with the addition of these networks. The error (in dB) as a function of time is plotted using SPICE and shown in Figure 5-50.

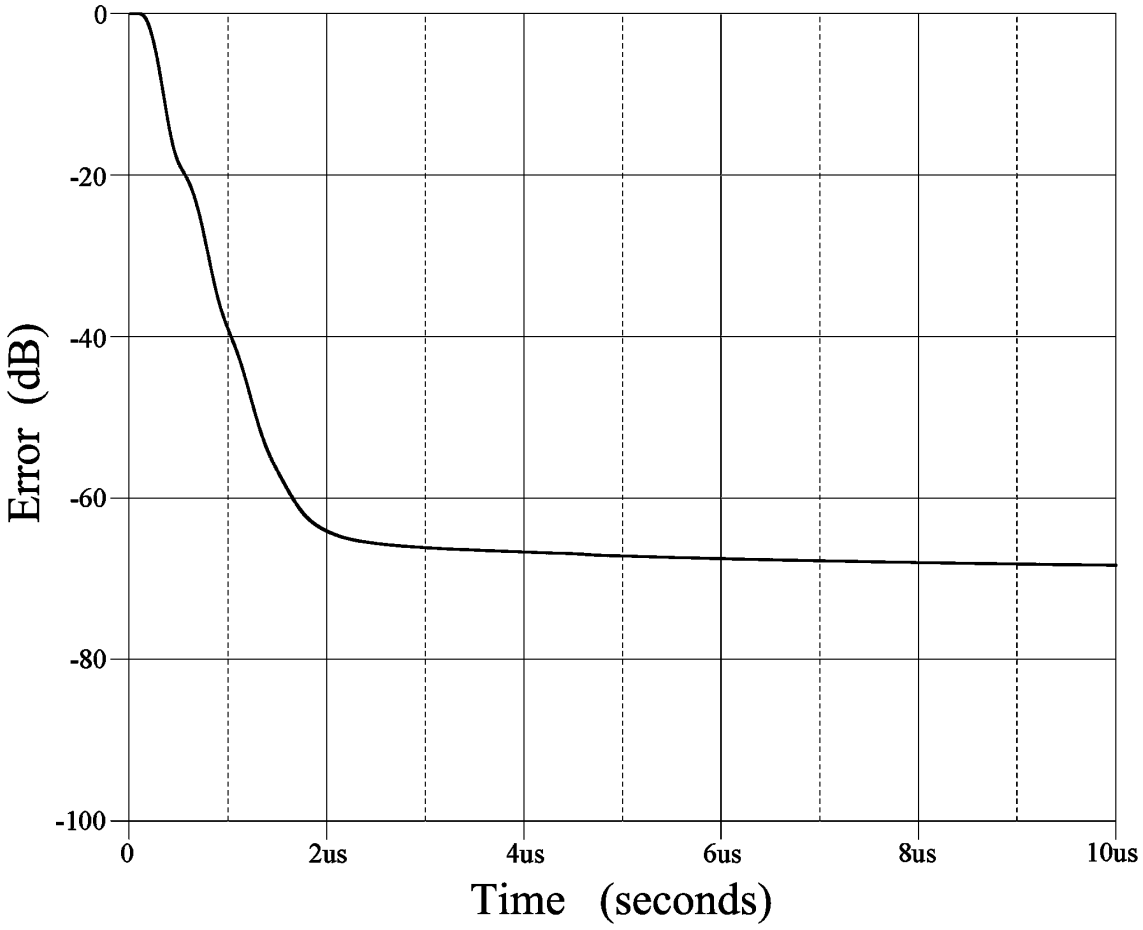

Figure 5-50: OPA357 circuit with lead/lag compensation, settling time error using SPICE.

The error settles at around –68 dB, even though the open loop gain available is closed to 80 dB (see Figure 5-49). The discrepancy between the error and the available open loop gain is a result of the ramping nature of the voltage signal at the output of the BJT drive amplifier. Equation (1-3) shows that the current in the magnetizing inductance is ramping up with time. This is a valid approximation since the OPA357 will continue to adjust to maintain a dc voltage on the sense winding (assuming that the magnetizing

inductance is constant with time). As the current ramps up, the voltage at the output of the BJT drive amplifier must also ramp up to compensate for the ramping voltage drop of the drive winding resistance. A ramping voltage on the output of the BJT drive amplifier results in a dc current flow through the 4 pF lead compensation feedback capacitor, causing a slight dc voltage across the 5 kΩ Thevenin resistance.

This error can be reduced by the addition of a 10 kΩ resistor to ground and a second series feedback capacitor as shown in the SPICE model schematic of Figure 5-51. Any dc current flowing through the first lead capacitor (due to the ramping voltage of the drive amplifier) will cause a dc voltage drop in the 10 kΩ resistor and prevent the dc current to continue to flow through the second capacitor. The third capacitor, shown in Figure 5-51, provides a capacitor divider network to aid in optimally setting the lead compensation frequency.

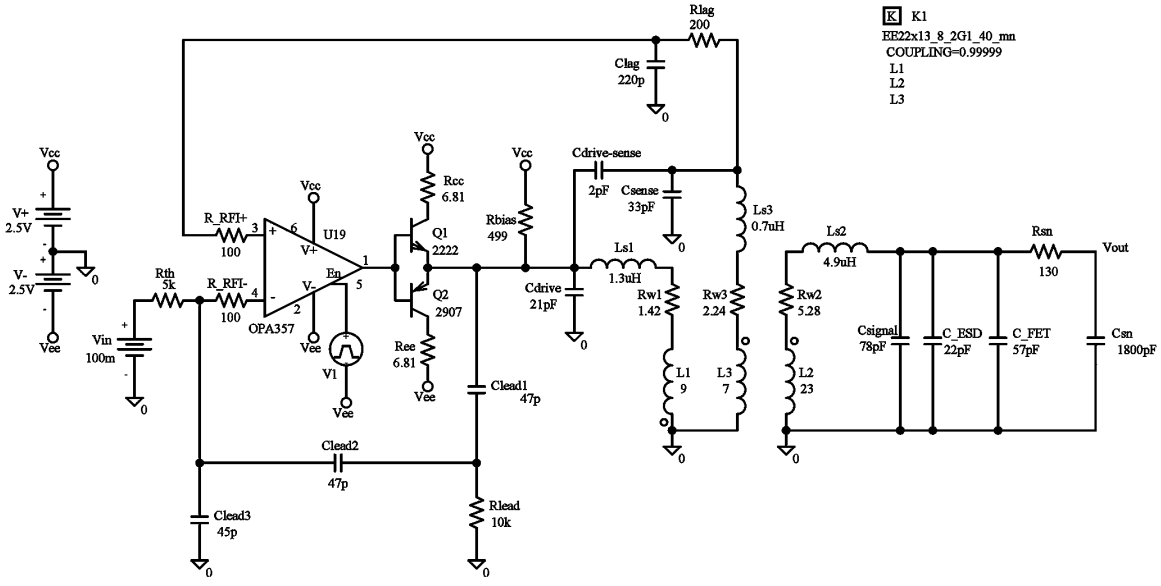

Figure 5-51: SPICE model schematic for OPA357 circuit with improved lead/lag compensation.

The value of the original, 4 pF lead capacitor (of Figure 5-48), is on the order of the parasitic capacitance of the OPA357. It is advantageous to have the lead capacitance at least 10 times this value so that variance in the parasitic capacitance will not drastically affect the lead compensation network. Therefore, the 47 pF value of the two series lead capacitors provide a more robust compensation network to variances in the parasitic circuit capacitance. SPICE is used to maximize the phase margin by selecting the optimal values for the lead and lag resistors and capacitors. The open loop gain/phase plot for the SPICE model schematic of Figure 5-51 is given in Figure 5-52.

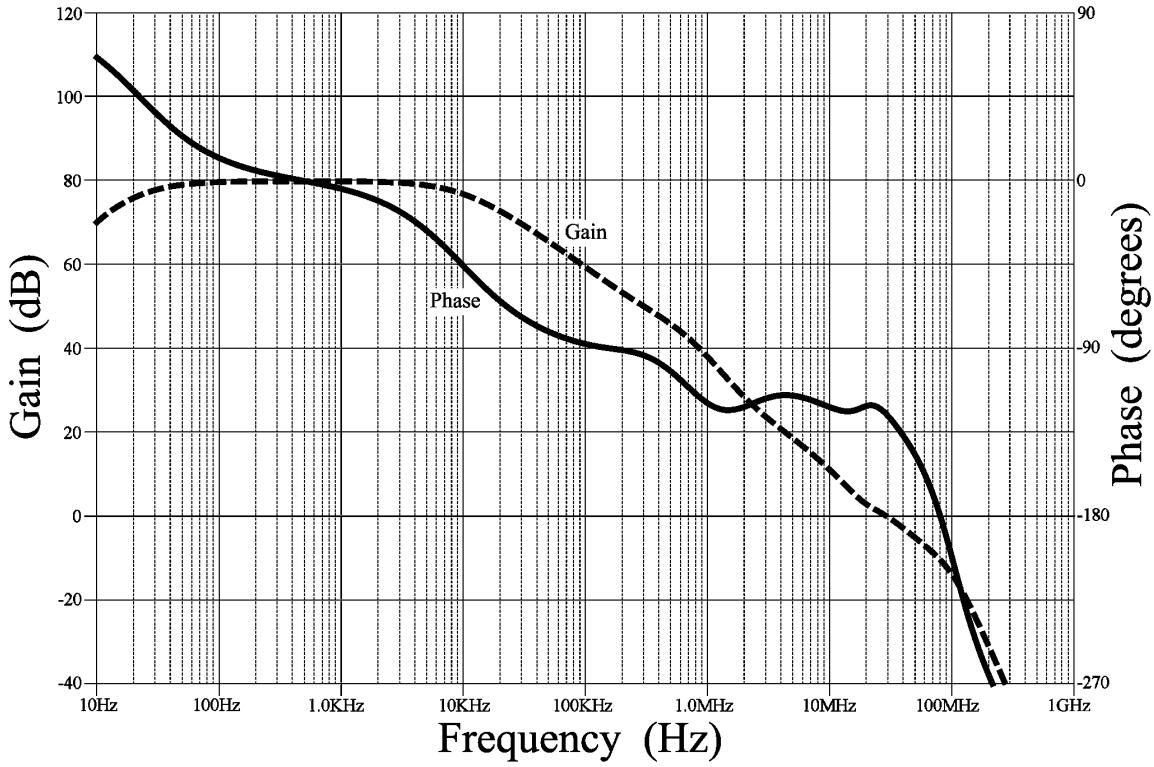

Figure 5-52: OPA357 circuit with improved lead/lag compensation, open loop gain/phase plot using SPICE.

The phase margin achieved with the improved lead/lag compensation network is around 56°. The error (in dB) as a function of time is plotted using SPICE and shown in Figure 5-53. With the addition of the improved lead/lag compensation network (along

with the drive amplifier circuit and snubber network), the compensation operational amplifier circuit is stable and meets the ±0.02 % accuracy goal (error less than –74 dB).

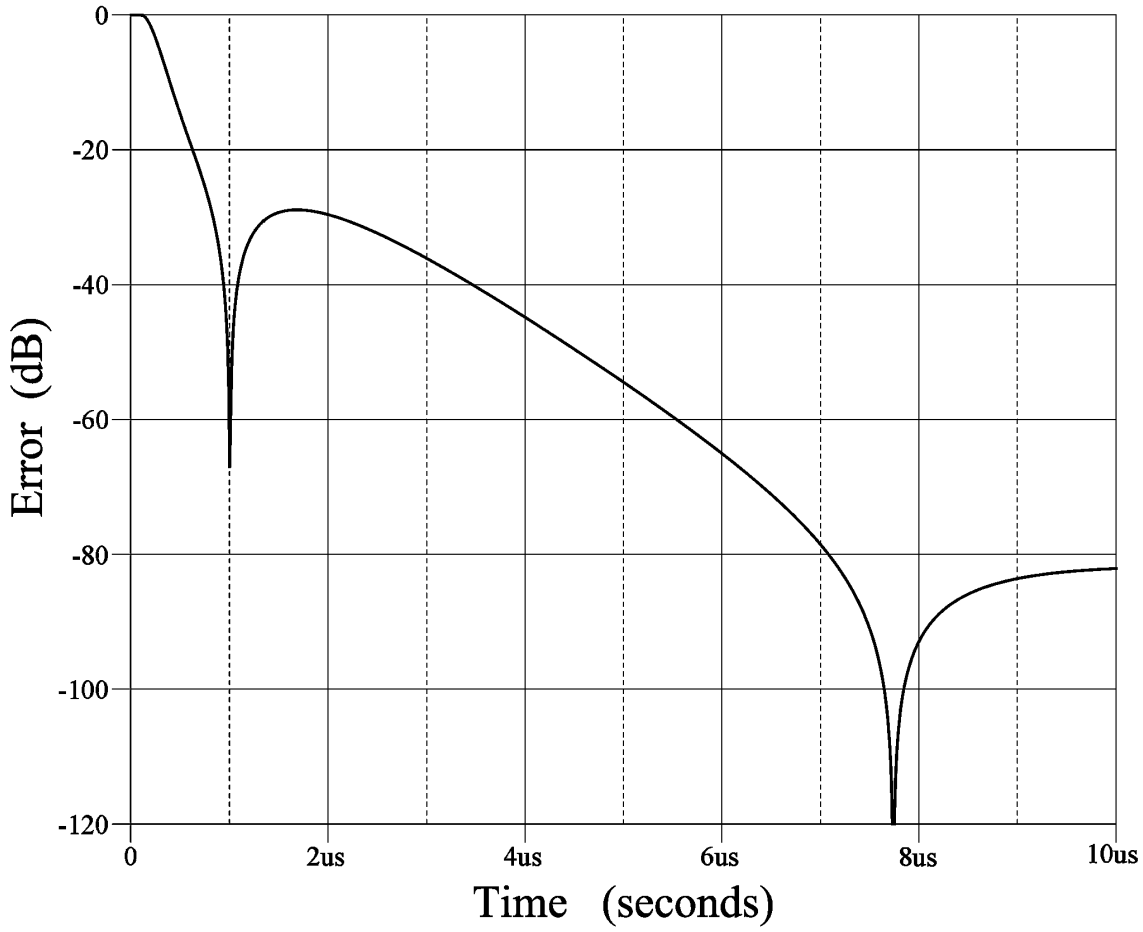

Figure 5-53: OPA357 circuit with improved lead/lag compensation, settling time error using SPICE.

5.6 Compensation Operational Amplifier Circuitry Stability and Accuracy

The isolation transformer of the Isolated Analog Selector is also used for the push/pull switched mode forward converter as shown in Figure 2-1. The additional power supply windings, diode/power supply storage capacitors, and power supply switching FETs are added to the SPICE model schematic as shown in Figure 5-54. The additional power supply windings do effect the stability of the compensation operational amplifier circuitry and require a snubber resistor/capacitor to maintain stability (499 Ω

resistor and 470 pF capacitor shown across the positive and negative power supply windings of Figure 5-54).

A three-stage R-C passive low-pass filter is added to the output of the signal winding to filter unwanted high frequency energy. High frequency energy may couple across the isolation transformer (from primary side to secondary side) during ESD or fast transient common mode events on the primary terminals of the digital protective relay.

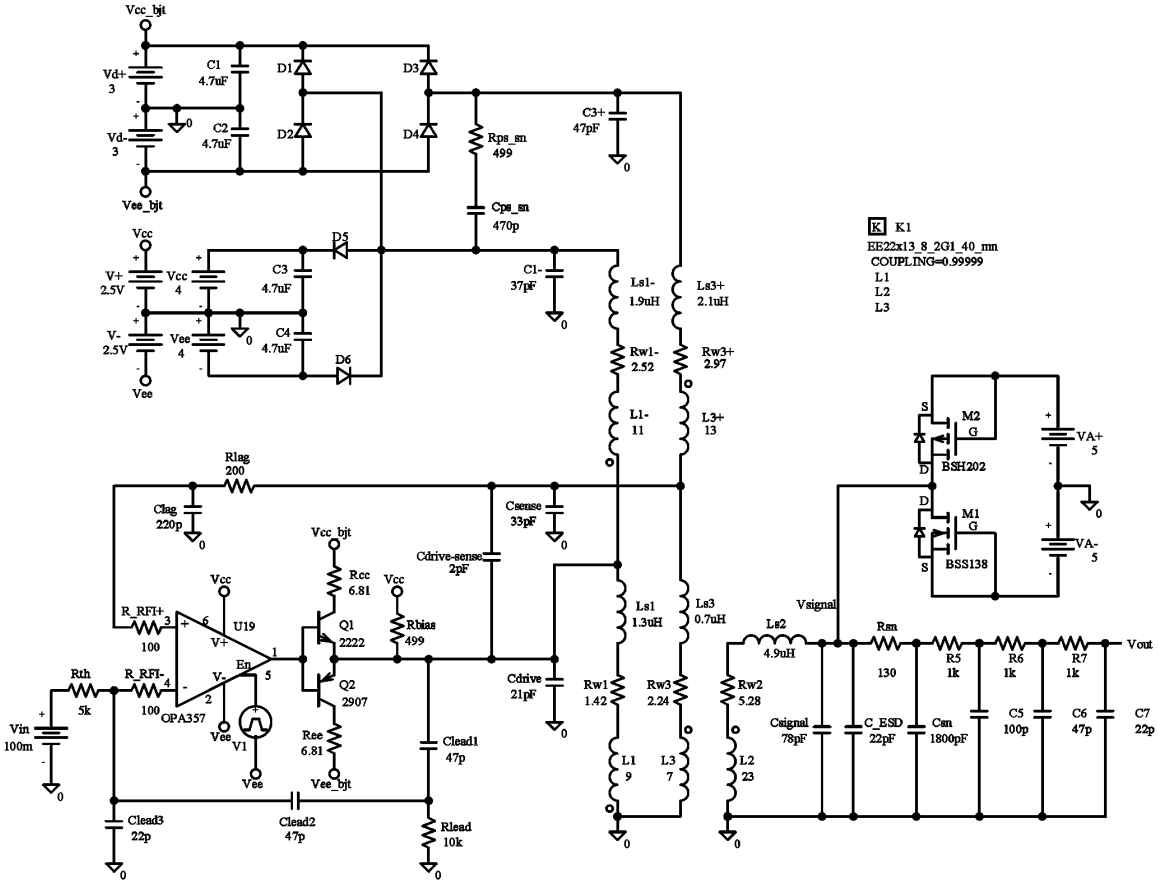

Figure 5-54: SPICE model schematic for compensation operational amplifier circuitry.

SPICE is used to maximize the phase margin by selecting the optimal values for the power supply winding snubber and lead/lag resistors and capacitors. The open loop gain/phase plot for the SPICE model schematic of Figure 5-54 is given in Figure 5-55.

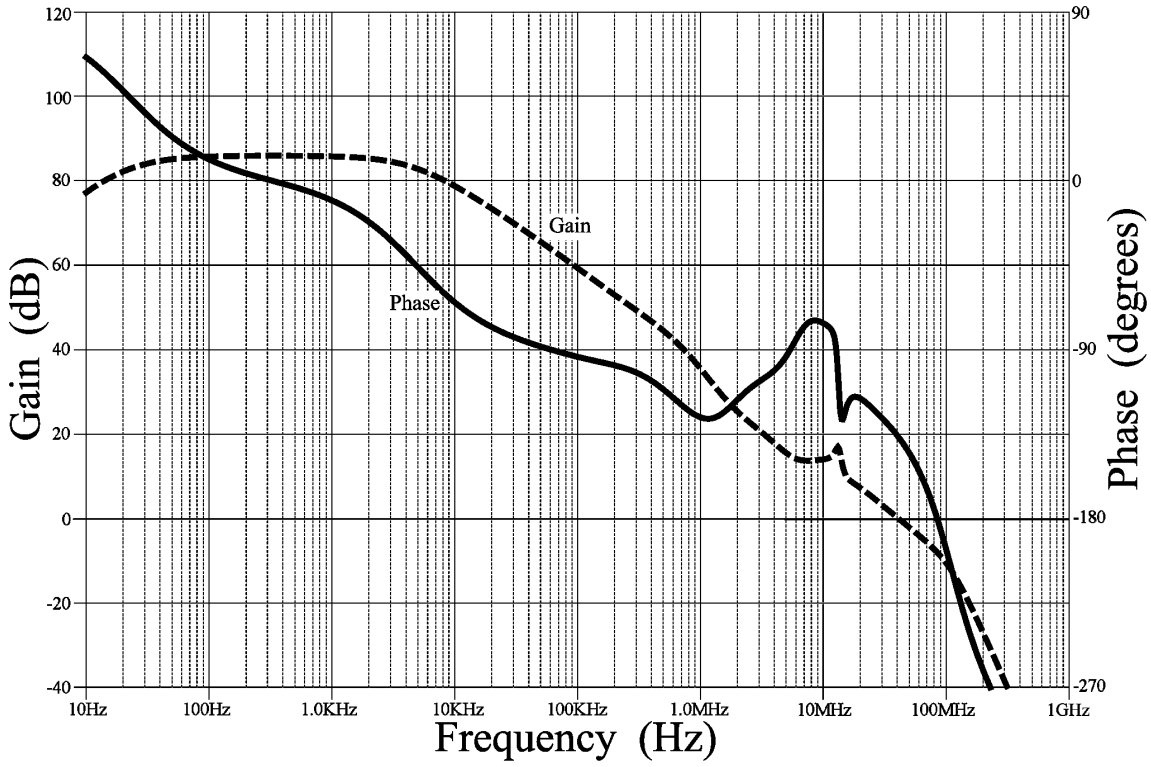

Figure 5-55: Compensation operational amplifier circuitry, open loop gain/phase plot using SPICE.

The phase margin achieved with the improved lead/lag compensation network is around 43.4°. The input step response for signal winding voltage and the output voltage, V_{out}, is shown in Figure 5-56. The V_{out} signal is the output of the Isolated Analog Selector connected to the analog multiplexer as shown in Figure 1-3.

The error (in dB) as a function of time is plotted using SPICE and shown in Figure 5-57. The final compensation operational amplifier circuit is stable (at least 43° of phase margin) and meets the ±0.02 % accuracy goal (error less than –74 dB).

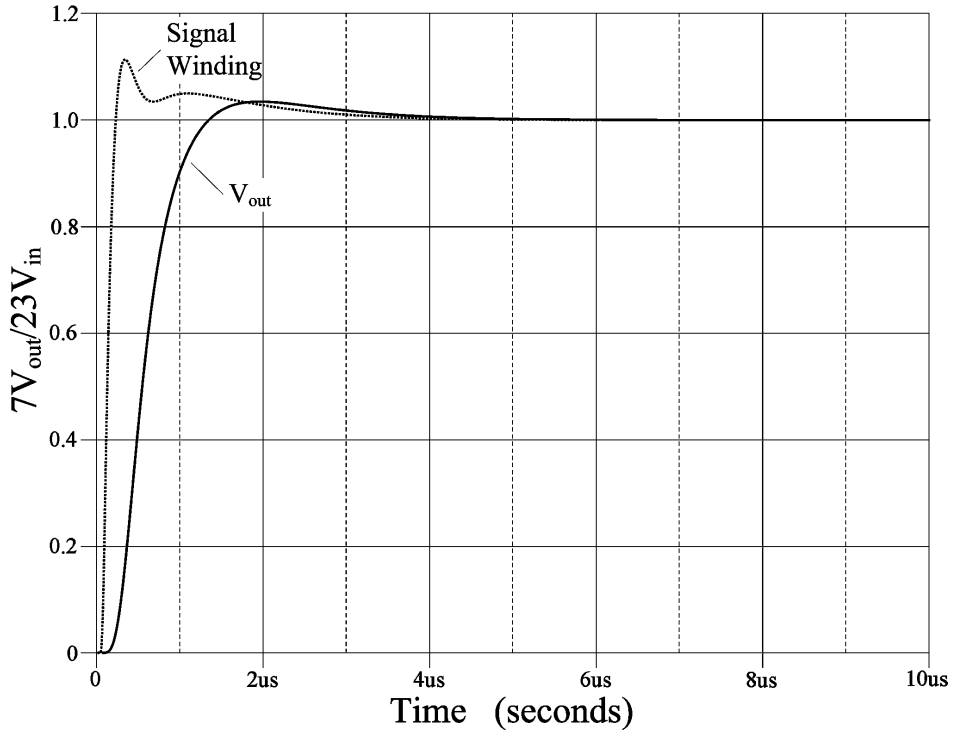

Figure 5-56: Step response for compensation operational amplifier circuitry using SPICE.

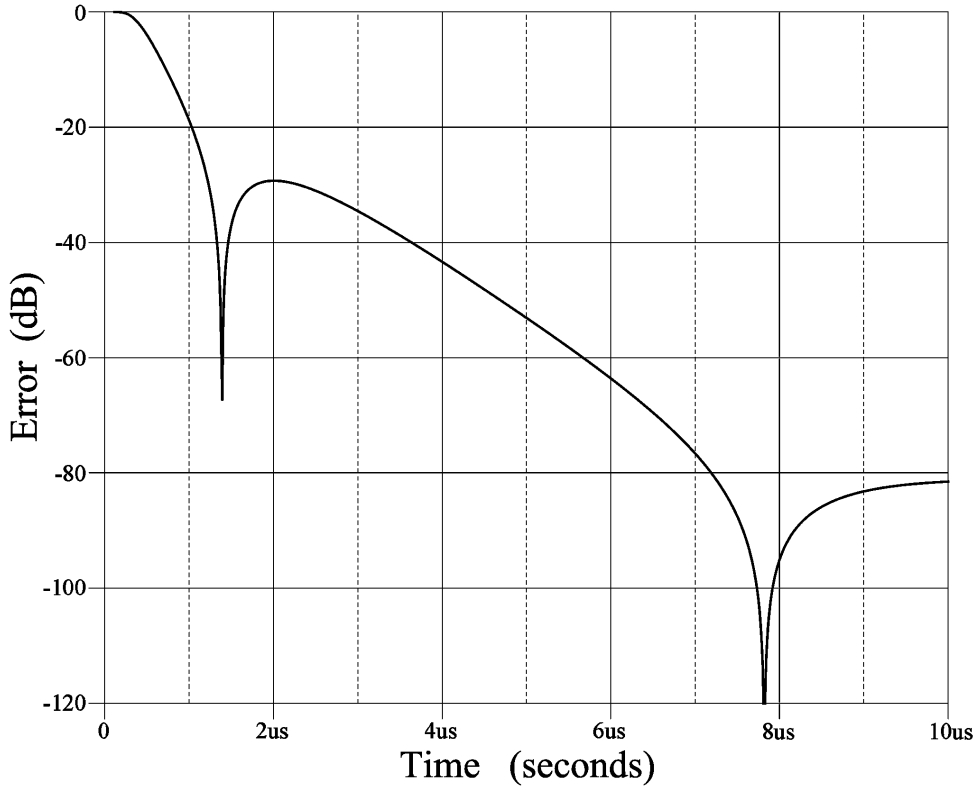

Figure 5-57: Compensation operational amplifier circuitry, settling time error using SPICE.

The capacitors used for the lead, lag, and snubber networks are NPO dielectric capacitors with a tolerance of ±5% ±30 ppm/°C. The resistors used for the lead, lag, and snubber networks are SMT resistors with a tolerance of ±1% ±100 ppm/°C. An analysis was done on the part-to-part and temperature variance of these components as well as the parasitic capacitance of the printed circuit board windings, compensation operational amplifier, switching FETs, winding resistances variations (from Table 4-2), and the various E-E core models (from Table 4-1). The range of the phase margin varied from 42.6 to 44.9 degrees. The range of the available open loop gain varied from 79.8 to 89.6 dB. The range of the error at 8 µs varied from –88.8 to –102.1 dB. And, the settling time to achieve an error under –74 dB varied from 6.50 to 7.12 µs.

Chapter 6 Isolation Transformer Magnetic Coupling Accuracy

In addition to the error introduced by the compensation operational amplifier circuitry, another major aspect of the accuracy of the new transformer isolated analog acquisition system is the magnetic coupling error between the drive, sense, and signal windings. In order to achieve an overall acquisition system accuracy of ±0.1 %, the magnetic coupling of the isolation transformer is constrained to have an error of ±0.02 %.

The purpose of this chapter is to analyze the magnetic coupling error between the three isolation transformer windings and identify an optimum placement of the windings to achieve high accuracy. A FEA (Finite Element Analysis) tool is used to model and measure the magnetic coupling error.

Understanding the magnetic coupling in a three winding transformer is an order of magnitude more difficult than for the two winding transformer. Three mutual inductance (magnetic coupling) terms exist for the three winding pair combinations. Obviously, the magnetic flux confined to the inside of a core couples to all three windings. This represents the bulk of the magnetizing inductance. However, how does one begin to comprehend the coupling of the magnetic flux located outside of a core?

In order to properly analyze the magnetic coupling between the drive, sense, and signal windings of the isolation transformer, an understanding of the general three winding transformer is needed. The approach taken in this chapter, is to build an understanding of the three winding transformer by defining a circuit model based on the physical magnetic flux of the three winding transformer.

The purpose of Section 6.1 is to create the three winding circuit model based on the physical magnetic flux. The first two sub-sections define the concepts of self-inductance

and mutual inductance. These two sub-sections are presented in order to provide a foundation for relating inductance to magnetic flux and for understanding and analyzing the FEA magnetic flux plots found in the remainder this chapter. The next sub-section 6.1.3, relates the well established two winding circuit model to the physical magnetic flux. And finally sub-section 6.1.4, defines the three winding transformer circuit model and relates the model elements to physical magnetic flux. This model is used to define the magnetic coupling error for a three winding transformer applied to the Isolated Analog Selector circuit, in terms of both the circuit elements and physical magnetic flux.

The FEA tool used is only two-dimensional and the E-E core used for the isolation transformer is, of course, three-dimensional. Section 6.2 describes the double 2-D method used to add the results of two orthogonal FEA simulations to arrive at a total accurate solution for the three dimensional E-E core.

And finally, section 6.3 analyzes the accuracy of the isolation transformer used for the Isolated Analog Selector and identifies the optimal placement of the drive and sense windings to achieve high accuracy.

6.1 Transformer Modeling

For the analog circuit design engineer, it is extremely helpful to model a circuit component with familiar ideal elements (e.g. resistors, capacitors, inductors, voltage sources, current sources, ...). This usually provides insight into how the component operates which may lead to intuition of how the component may be used. In addition, the model can be used in circuit simulators, such as SPICE to help analyze how the component interacts with the rest of the circuitry.

The circuit models developed in this section contain circuit elements that are directly related to the physical magnetic flux. This is important for identifying and improving the magnetic coupling accuracy of the Isolated Analog Selector isolation transformer. In general, these models can give insight to a design engineer for understanding and properly integrating a two or three winding transformer in an analog circuit. As an outcome of basing the circuit elements on physical magnetic flux, the circuit model can also be used in SPICE for simulation of a circuit with a three winding transformer (i.e., no negative elements).

For components or systems containing inductive coupling, the familiar modeling elements (in addition to the resistor, capacitor, inductor, ...) can also include the coupled inductor as well as the ideal transformer combined with the magnetizing inductor (all elements assumed to be ideal). These two modeling elements are introduced in greater detail in sub-section 6.1.3.

For any of the inductive coupling model elements (inductor, coupled inductor, or ideal transformer with magnetizing inductor), it is insightful to identify the physical magnetic flux associated with the inductive element. The next sub-section identifies and defines the relationship between magnetic flux and inductance.

For simplicity, the inductor and transformer circuit modeling in this chapter excludes capacitance. A first order capacitance model for the transformer was introduced in Chapter 4 and used for SPICE simulations throughout Chapter 5. The result of the SPICE simulations shows that the compensation operational amplifier circuitry is settled within 8 μs. Therefore, the error introduced by the isolation transformer consists solely

of magnetic coupling error (at the point in time of A-D sampling). Hence, the models in this chapter can exclude capacitance.

6.1.1 *Self-Inductance*

Electromagnetic induction is summarized in Faraday's Law of Induction (the basis for one of Maxwell's equations):

$$V(t) = -\frac{d}{dt}\Phi(t). \tag{6-1}$$

For any closed loop, Faraday's Law of Induction, (6-1) states that the voltage induced in a loop (i.e. voltage across two terminals of a loop if the loop were broken) is proportional to the rate of change in the magnetic flux, Φ, passing through the loop.

The simplest inductive element, the ideal inductor, is a two-terminal element of lumped self-inductance. In circuit analysis, the relationship between the constant, linear inductance, *L* (in henries, H), and the voltage across and current through an ideal inductor is:

$$V(t) = L\frac{d}{dt}I(t). \tag{6-2}$$

Lumped circuit elements, like the inductor in (6-2), are assumed to have spatial dimensions that are electrically small (i.e., the largest dimension of the physical component or system is less than 1/10 of the wavelength [21]).

By combining (6-1) and (6-2), the relationship between the inductance, *L*, magnetic flux, Φ, and current, *I*, for the ideal inductor is:

$$L = \frac{\Phi(t)}{I(t)}. \tag{6-3}$$

The magnetic flux, $\Phi(t)$, whose derivative induces the voltage in the ideal inductor, is proportional to and a direct consequence of the inductor current, $I(t)$. This relationship between $I(t)$ and $\Phi(t)$ is in accordance with Ampere's law since the dimensions are electrically small (i.e., the quasi static approximation of Maxwell's equations). The inductance, L, is the ratio of this voltage inducing magnetic flux to the inductor current.

Hence, self-inductance is by definition the proportionality constant (of voltage inducing magnetic flux to inductor current) of a two-terminal circuit element as determined from the current solely flowing through the two terminals, with all other circuit currents and/or sources of magnetic fields inhibited.

For an illustrative example of magnetic flux corresponding to self-inductance, consider a single coil of wire (in the x-y plane) in free space, being driven by a current, I, as shown in Figure 6-1. The two terminals of the coil are not shown and the current in the lead wires connecting to the two coil terminals are ignored for this example.

The solution for the magnetic flux, Φ, is portrayed in Figure 6-1 as lines of flux in the x-z plane only. However, the total magnetic flux is symmetric about the z-axis. Flux lines follow the angle of the magnetic flux density vector $\vec{\mathbf{B}}$ and the magnitude of $\vec{\mathbf{B}}$ can be determined by the shading and concentration of the flux lines. All of the magnetic flux produced by the single coil passes through and induces a voltage in the coil.

The self-inductance, L, of the coil in Figure 6-1 is the ratio of the magnetic flux, Φ, and the current, I, in the coil. The value of L can be determined by solving for the magnetic flux and is a function of the radius of the coil as well as the wire diameter [22].

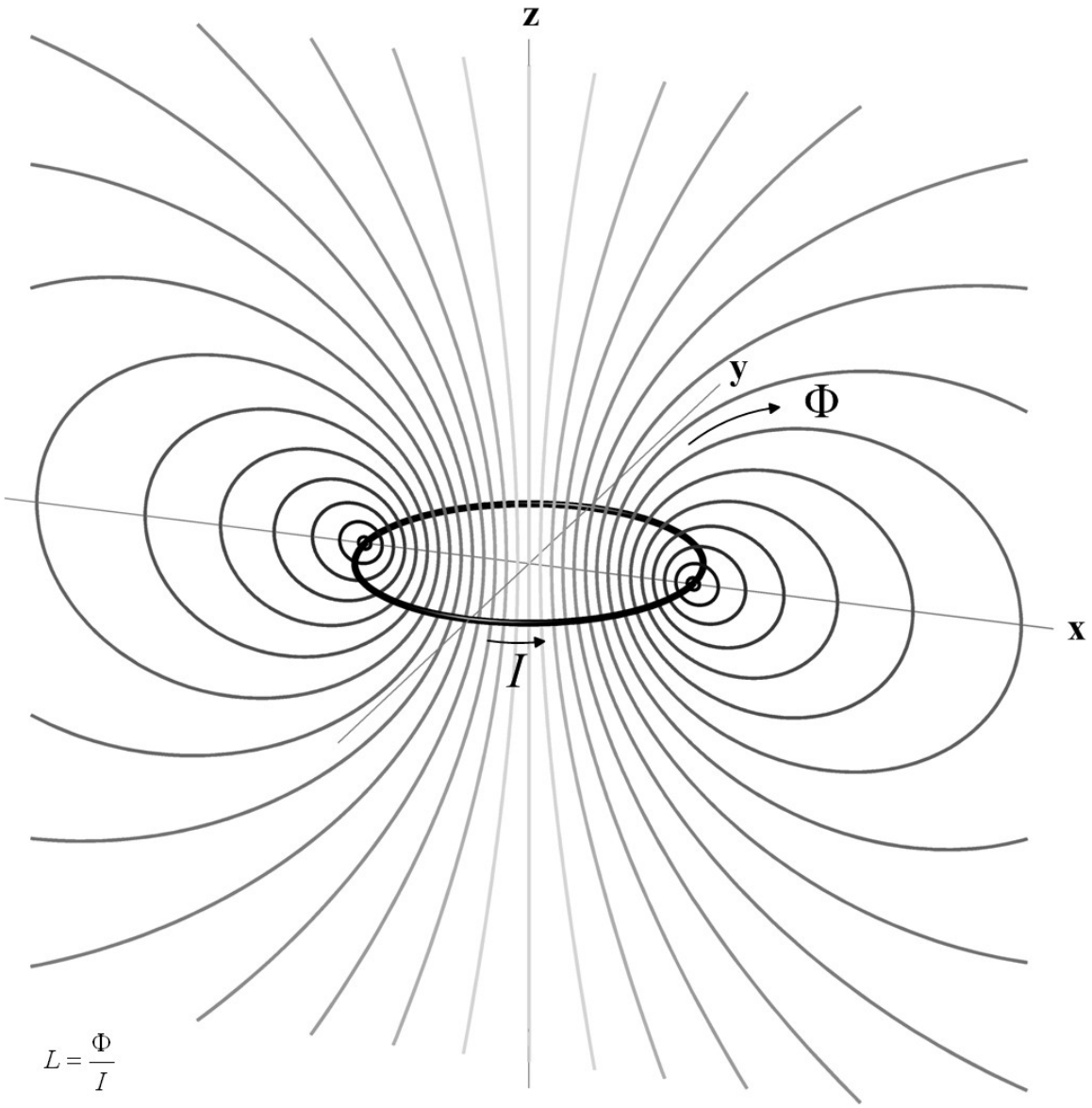

Figure 6-1: Magnetic flux, Φ, produced by a single coil of wire being driven by current, *I*.

Ignoring capacitance, an actual inductor component can be modeled with an ideal resistor, *R* (equal to the winding/lead resistance) in series with an ideal inductor, *L* (equal to the lumped self-inductance). The voltage, *V*, across the actual inductor due to the sinusoidal current, *I*, through the inductor is: $V = (R + j\omega L)I$.

6.1.2 *Mutual Inductance*

Mutual inductance may occur between any two, two-terminal circuit elements/components. Mutual inductance is related to the voltage induced (by electromagnetic induction) in one two-terminal circuit element due to the current flowing solely in another two-terminal circuit element.

From a magnetic flux standpoint, the mutual inductance between element #2 from element #1, M_{21}, is the ratio of magnetic flux that couples to element #2, Φ_{21}, (i.e. induces a voltage in element #2) due to current flowing only in element #1, I_1: $M_{21} = \Phi_{21}/I_1$.

For an illustrative example of magnetic flux corresponding to mutual inductance, consider two separate coils of wire in free space as shown in Figure 6-2. When Coil 1 is driven with I_1, only the magnetic flux Φ_{21} couples to Coil 2 (this magnetic flux is bounded by the lopsided inner-tube shaped volume portrayed in Figure 6-2(a)): $M_{21} = \Phi_{21}/I_1$. Similarly, when Coil 2 is driven with I_2, only the magnetic flux Φ_{12} couples to Coil 1 (this magnetic flux is bounded by the volume portrayed in Figure 6-2(b)): $M_{12} = \Phi_{12}/I_2$. Even though the magnetic fluxes Φ_{12} and Φ_{21} are in different physical locations and the two coils are different sizes, by reciprocity, $M_{12} = M_{21}$. Reciprocity applies to any system that consists of linear, isotropic materials.

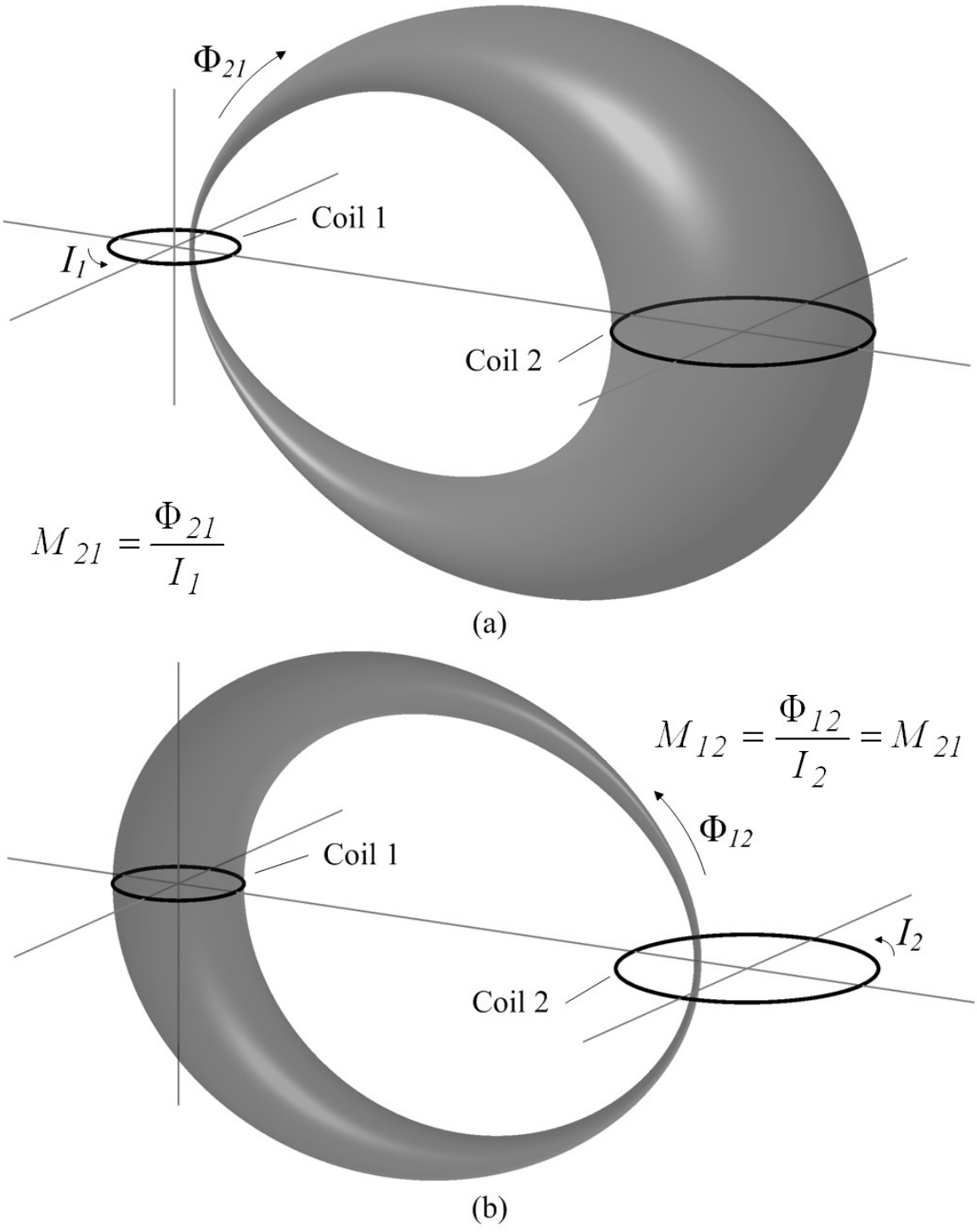

Figure 6-2: Mutual inductance and corresponding magnetic flux: (a) Magnetic flux, Φ_{21}, coupling to Coil 2 due to I_1 flowing only in Coil 1, (b) Magnetic flux, Φ_{12}, coupling to Coil 1 due to I_2 flowing only in Coil 2.

6.1.3 *Two Winding Transformer Modeling*

The two winding transformer is a two port (four terminal) component containing both self-inductance and mutual inductance. From a circuit analysis standpoint, the two winding transformer is captured in Figure 6-3.

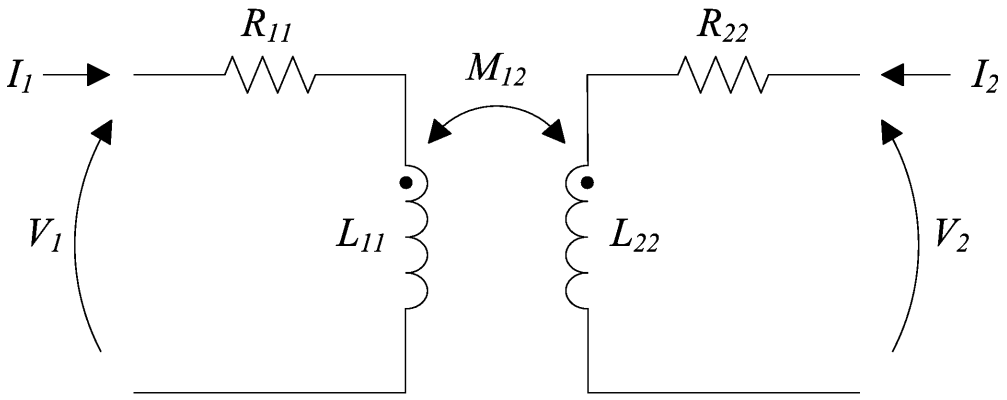

Figure 6-3: Two winding transformer circuit model.

The linear equation defining the relationship of the voltage and currents can be written in matrix form as: $\mathbf{V} = (\mathbf{R} + j\omega\mathbf{L})\mathbf{I}$ (where **R** and **L** are the resistance and inductance matrices respectively):

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \left(\begin{bmatrix} R_{11} & 0 \\ 0 & R_{22} \end{bmatrix} + j\omega \begin{bmatrix} L_{11} & M_{12} \\ M_{21} & L_{22} \end{bmatrix} \right) \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \Rightarrow \mathbf{V} = (\mathbf{R} + j\omega\mathbf{L})\mathbf{I} . \quad (6\text{-}4)$$

The self-inductance of the primary circuit, L_{11}, is associated with the two primary terminals (V_1 of Figure 6-3). Likewise, the self-inductance of the secondary circuit, L_{22}, is associated with the two primary terminals (V_2 of Figure 6-3).

The mutual inductance, M_{12}, defines the amount of magnetic coupling (i.e. magnetic flux that induces a voltage) between the primary circuit (relating to V_1 and I_1 of Figure 6-3) and the secondary circuit (relating to V_2 and I_2 of Figure 6-3). Again, by reciprocity, $M_{21} = M_{12}$.

It is not easy to acquire a physical intuition about the circuit model of Figure 6-3. Mathematically, the model works. But, it is difficult to fully understand the model when connected to surrounding circuitry. A simpler approach is to redefine the two winding transformer model using either the ideal coupled inductor or the ideal transformer along with ideal inductors.

The simplification is achieved by separating the model into inductance that does not couple the primary and secondary circuits (leakage inductance) from inductance that entirely couples both primary and secondary windings (mutual inductance). The leakage inductance is modeled with the ideal inductor and the mutual inductance is modeled with the coupled inductor as shown in Figure 6-4(a) (leakage/series inductance: L_{s1} and L_{s2}, coupled inductance: L_{c1} and L_{c2}).

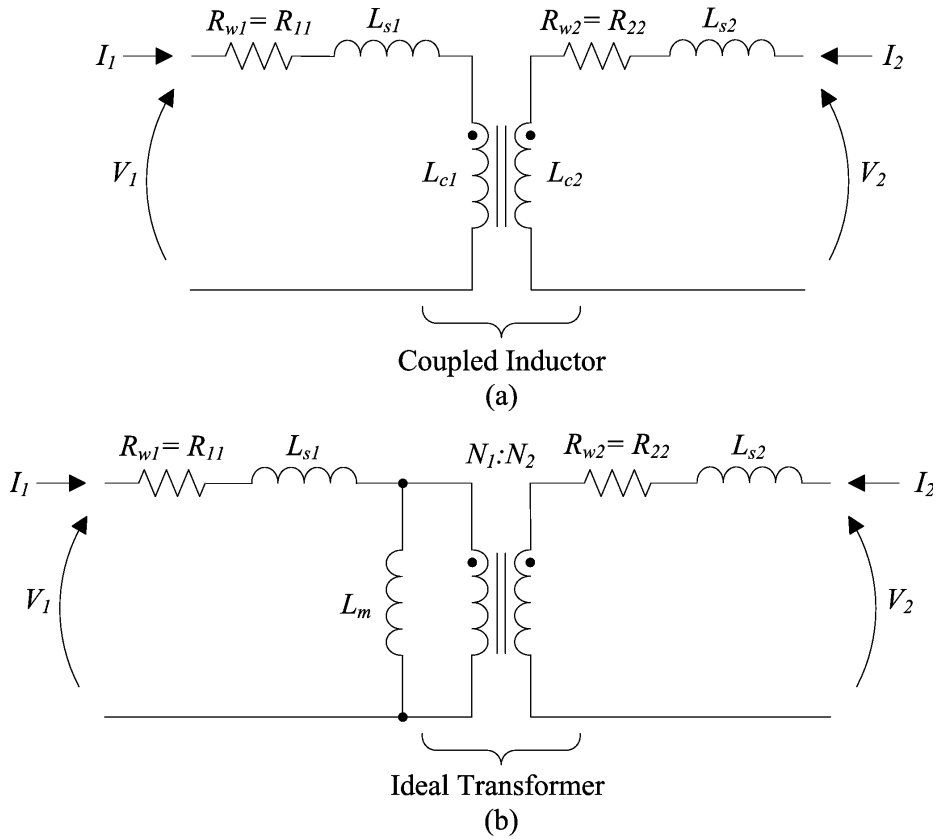

Figure 6-4: Two winding transformer equivalent circuit model.

The value of L_{s1}, L_{s2}, L_{c1} and L_{c2} could be arbitrarily chosen as long as $L_{11} = L_{s1} + L_{c1}$, $L_{22} = L_{s2} + L_{c2}$ and $M_{12} = \sqrt{L_{c1}L_{c2}}$ (L_{c1} and L_{c2} positive). However, some values of L_{c1} and L_{c2} will result in negative leakage inductances values for L_{s1} and L_{s2}. Although any combination of L_{s1}, L_{s2}, L_{c1} and L_{c2} meeting the above requirements will mathematically result in the same linear matrix equation: $\mathbf{V} = (\mathbf{R} + j\omega\mathbf{L})\mathbf{I}$, the only set of values that makes physical sense is the set based on the actual number of turns for the primary (N_1) and secondary (N_2) transformer windings:

$$\begin{aligned} L_{c1} &= \frac{N_1}{N_2} M_{12} \\ L_{c2} &= \frac{N_2}{N_1} M_{12} = \frac{N_2^2}{N_1^2} L_{c1} \,. \\ L_{s1} &= L_{11} - L_{c1} \\ L_{s2} &= L_{22} - L_{c2} \end{aligned} \qquad \text{(6-5)}$$

Choosing $L_{c1} = (N_1/N_2)M_{12}$ and $L_{c2} = (N_2/N_1)M_{12}$ will always result in positive values for L_{s1} and L_{s2} for a real transformer. The ideal coupled inductor, shown in Figure 6-4(a), is based on these values for L_{c1} and L_{c2}. Although the ideal coupled inductor is easily implemented in SPICE, it can still be somewhat confusing to analyze a circuit containing a coupled inductor. For this reason, the preferred model used for the remainder of this chapter is the one shown in Figure 6-4(b) combining the ideal transformer and magnetizing inductor, $L_m = (N_1/N_2)M_{12}$.

For the model of Figure 6-4(b), N_1 and N_2 could also be arbitrarily chosen and still mathematically result in the same linear matrix equation: $\mathbf{V} = (\mathbf{R} + j\omega\mathbf{L})\mathbf{I}$. However, the only values for N_1 and N_2 that make physical sense are when N_1 equals the number of primary turns and N_2 equals the number of secondary turns:

$$L_m = \frac{N_1}{N_2} M_{12}$$
$$L_{s1} = L_{11} - L_m \quad . \tag{6-6}$$
$$L_{s2} = L_{22} - \frac{N_2^2}{N_1^2} L_m$$

The ideal transformer and magnetizing inductor, L_m, of Figure 6-4(b) provides some physical intuition into the model. The leakage inductance represents magnetic flux that does not couple to the other winding. The magnetizing inductance represents magnetic flux that always couples to both windings. Even though the model of Figure 6-4(b) was derived for linear systems, it is also useful for nonlinear systems as well. The nonlinear characteristics of a core material are essentially associated with the magnetic flux that couples to both windings (i.e., the magnetizing inductance, L_m). Typical, the leakage inductance is associated with magnetic flux located internal to the winding, in the winding insulation, or in air around the winding (with a small amount possibly located in the core itself). As a good first order approximation, the leakage inductance is modeled with a linear inductor with permeability of free space, μ_o. The nonlinear core is easily simulated in SPICE by coupling the winding turns to a nonlinear core model.

The final advantage of the model of Figure 6-4(b) is that the physical flux associated with each inductance term is easily identified. As an illustrative example, consider two single turn coils in free space: Coil 1 (primary) and Coil 2 (secondary). Assume the coils have the same *z* axis of symmetry with both coils located in the *x*-*y* plane as shown in Figure 6-5 (again lead wires ignored).

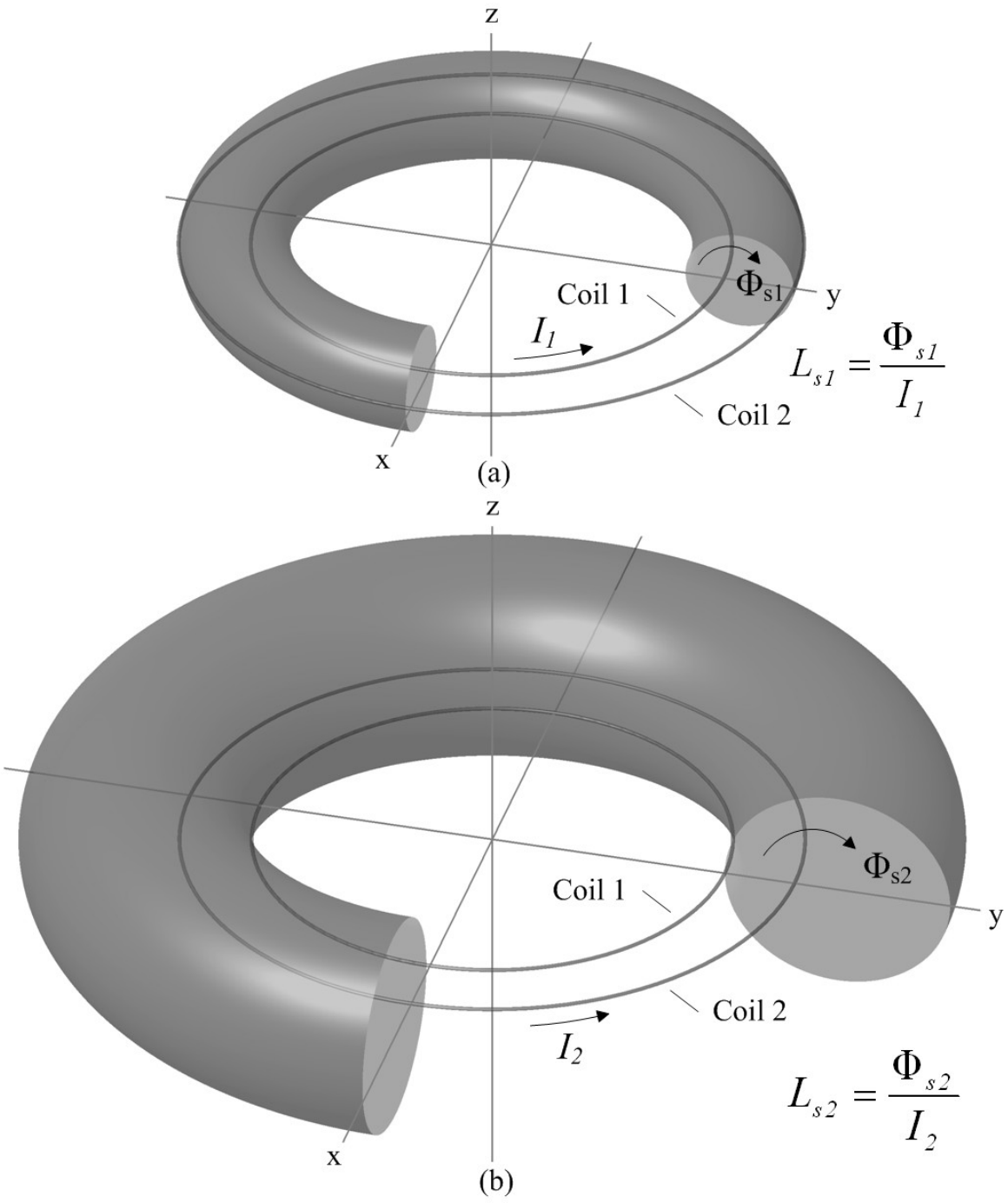

Figure 6-5: Leakage inductance and corresponding magnetic flux in free space: (a) Leakage flux, Φ_{s1}, coupling to Coil 1 (but not to Coil 2) due to I_1 flowing only in Coil 1, (b) Magnetic flux, Φ_{s2}, coupling to Coil 2 (but not to Coil 1) due to I_2 flowing only in Coil 2.

The leakage inductance, L_{s1} of Coil 1 is associated with the magnetic flux Φ_{s1} about Coil 1 (due to current flowing in Coil 1, I_1) that does not couple to Coil 2. The leakage

flux, Φ_{s1}, is bounded by a near toroidal shaped volume as shown in Figure 6-5(a) (1/4 of the volume is cut out for illustrative purposes).

For a magnetic flux to couple to (i.e., induce a voltage in) a coil, a net magnetic flux must pass through a surface bounded by the coil. For example, for Coil 1, the surface could be a disk in the *x*-*y* plane with the same radius as Coil 1. It is clear from Figure 6-5(a) that the leakage flux, Φ_{s1}, couples to Coil 1, since all of the flux passes upwardly through the disk shaped surface bounded by Coil 1. However, for Coil 2, the leakage flux, Φ_{s1}, of Figure 6-5(a) does not have a net magnetic flux through the disk shaped surface bounded by Coil 2 (any flux passing upwardly on the inside of Coil 1 has to also pass downwardly on the outside of Coil 1).

The mutual flux, Φ_{21}, that couples both Coil 1 and 2 (due to current flowing in Coil 1) is located in the rest of the physical space outside of the near toroidal shaped volume portrayed in Figure 6-5(a), with the flux lines having shapes similar to that shown in Figure 6-1.

The leakage inductance, L_{s2}, of Coil 2 is associated with the leakage flux, Φ_{s2}, about Coil 2 (due to current flowing in Coil 2, I_2), that does not couple to Coil 1. It is easier to recognize that the leakage flux, Φ_{s2}, of Figure 6-5(b) couples to Coil 2, but not to Coil 1. The mutual flux, Φ_{12}, that couples both Coil 1 and Coil 2 (due to current flowing in Coil 2) is located in the rest of the physical space outside the near toroidal shaped volume portrayed in Figure 6-5(b).

For systems with symmetry about an axis, an FEA (Finite Element Analysis) 2-D (two-dimension) solver is used to quickly obtain the inductance matrix and plot the flux lines associated with driving a given coil/winding [23]. Consider the two single turn coils

of Figure 6-5 with sizes and cross sectional areas similar to the PCB traces found in the Isolated Analog Selector transformer of Figure 3-2. Using an FEA 2-D solver (axial symmetric), the resistance and inductance matrices are:

$$\mathbf{R} = \begin{bmatrix} R_{11} & 0 \\ 0 & R_{22} \end{bmatrix} = \begin{bmatrix} 0.108\,\Omega & 0 \\ 0 & 0.141\,\Omega \end{bmatrix}$$
$$\mathbf{L} = \begin{bmatrix} L_{11} & M_{12} \\ M_{21} & L_{22} \end{bmatrix} = \begin{bmatrix} 32.4\,\text{nH} & 10.4\,\text{nH} \\ 10.4\,\text{nH} & 44.2\,\text{nH} \end{bmatrix}, \quad \text{(6-7)}$$

and thus the transformer model element values are found and given in Figure 6-6.

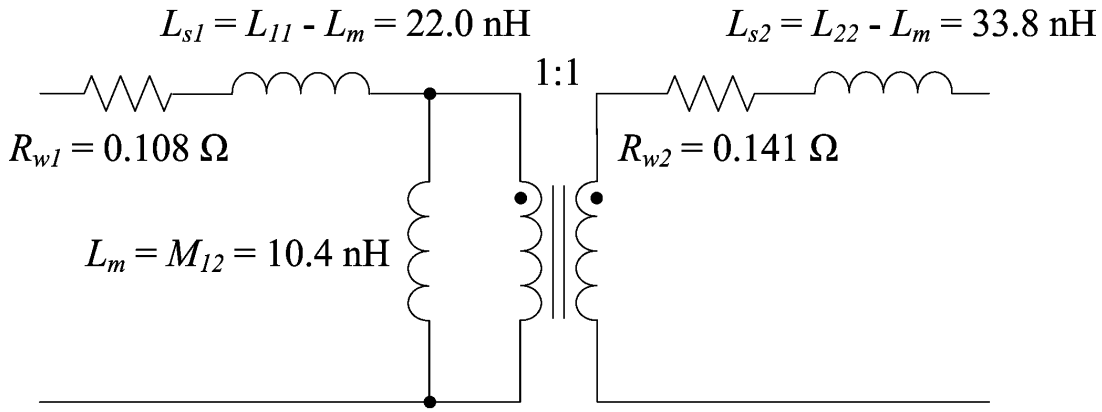

Figure 6-6: Transformer equivalent circuit model for two single turn coils.

The FEA 2-D solver is also used to plot the various magnetic fluxes associated with the corresponding inductances as shown in Figure 6-7.

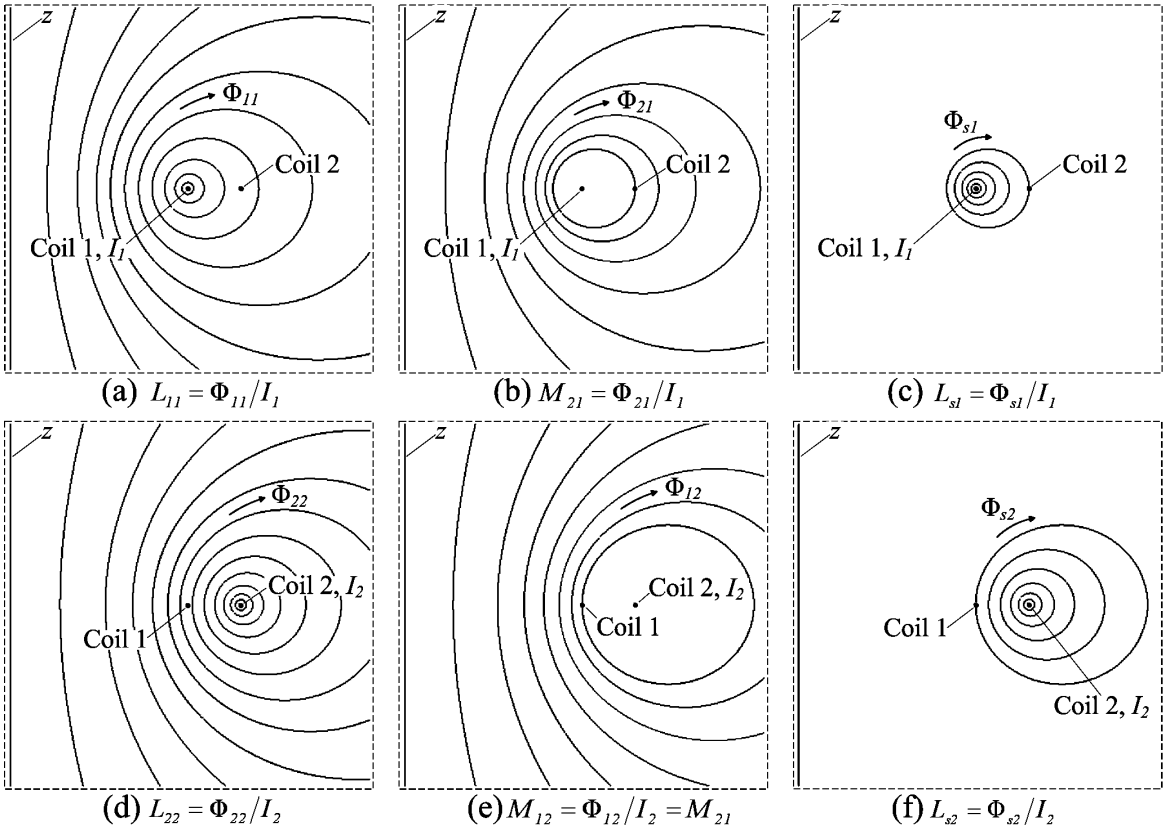

Figure 6-7: Magnetic flux and corresponding inductances associated with two single turn coils.

In the 2-D plots of Figure 6-7, the *z* axis of symmetry is located on the left hand side. To obtain the full 3-D (three-dimension) solution, the 2-D plot is rotated about the *z*-axis (similar to Figure 6-1). Therefore, in 2-D, Coil 1 and 2 are represented by their circular cross sections. Figure 6-7(a) shows the magnetic flux associated with the self-inductance, L_{11}, of Coil 1. Figure 6-7(b) shows the magnetic flux associated with the mutual inductance, M_{21}, between Coil 2 from Coil 1. Figure 6-7(c) shows the magnetic flux (leakage flux) associated with the leakage inductor, L_{s1}, of Coil 1 (2-D portrayal of similar flux shown in Figure 6-5(a)).

In 2-D, for a magnetic flux to couple to (i.e., induce a voltage in) a coil, a net magnetic flux must pass through a line from the coil to the axis of symmetry (i.e., *z*-axis

in this example). From Figure 6-7(b), all of the magnetic flux, Φ_{21}, couples both coils since a horizontal line from either coil to the *z*-axis will be upwardly crossed by all of the flux Φ_{21}. However, the leakage flux, Φ_{s1}, in Figure 6-7(c) only couples to Coil 1. A horizontal line from Coil 2 to the *z*-axis is crossed upwardly and downwardly by the same flux lines of Φ_{s1}, having a net zero contribution.

Figure 6-7(d), (e) and (f) show the magnetic flux associated with the self-inductance, L_{22}, mutual inductance, M_{12} and leakage inductor, L_{s2}, respectively, associated with Coil 2. The leakage flux of Figure 6-7(f) is a 2-D portrayal of the similar flux shown in Figure 6-5(b).

If a core material is added to the two coil transformer of Figure 6-5, Figure 6-6 and Figure 6-7, the self-inductance terms L_{11} and L_{22} and mutual/magnetizing inductance, $L_m = M_{12}$, would increase proportional to the magnetic cross section and inversely proportional to the magnetic length of the core as shown in (4-5). However, the leakage inductance terms, $L_{s1} = L_{11} - L_m$ and $L_{s2} = L_{22} - L_m$ would only change slightly in value. The leakage flux would still be constrained about the corresponding coil, with the cross-section boundary being slightly influenced by the shape and location of the actual core.

Leakage inductance approximation formulas for two winding, multi-turn transformers with windings about the center leg of an E-E or E-I core are based on measurements from actual transformers [24]. The leakage inductance values are proportional to the square of the winding turns and are also a function of the space occupied by the winding as well as the proximity of the two windings to each other.

For analyzing the accuracy of the coupling between the drive, sense and signal windings of the Isolated Analog Selector transformer of Figure 3-2, a three winding

transformer model is first presented in the next section. It turns out that the leakage inductance values have virtually nothing to do with the coupling accuracy between the three windings. Therefore, the leakage inductance approximation formulas give little insight into optimizing the windings for coupling accuracy. Finite Element Analysis is used to obtain the inductance values for the three winding transformer and gives insight into optimizing the location of the three windings to achieve high accuracy.

6.1.4 *Three Winding Transformer Modeling*

The three winding transformer is a three port (six terminal) component containing self-inductance and mutual inductance as well as resistance (again, ignoring capacitance). From a circuit analysis standpoint, the three winding transformer is captured in Figure 6-8.

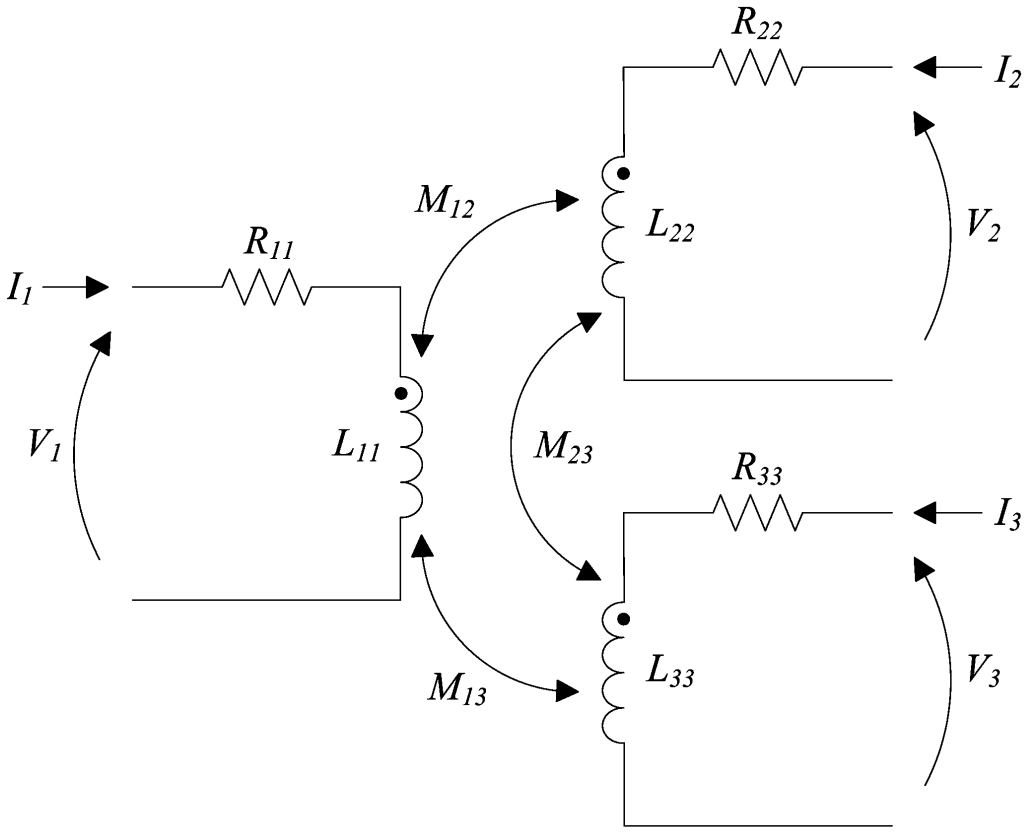

Figure 6-8: Three winding transformer circuit model.

The linear equation defining the relationship of the voltage and currents can be written in matrix form as:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_2 \end{bmatrix} = \left(\begin{bmatrix} R_{11} & 0 & 0 \\ 0 & R_{22} & 0 \\ 0 & 0 & R_{33} \end{bmatrix} + \mathrm{j}\omega \begin{bmatrix} L_{11} & M_{12} & M_{13} \\ M_{21} & L_{22} & M_{23} \\ M_{31} & M_{32} & L_{33} \end{bmatrix} \right) \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \Rightarrow \mathbf{V} = \left(\mathbf{R} + \mathrm{j}\omega\mathbf{L}\right)\mathbf{I} . \quad (6\text{-}8)$$

Many three winding transformer circuit models are useful in simulations and circuit analysis [25] [26] [27]. However, a circuit model that is based on the actual magnetic flux gives useful insight into the magnetic coupling. Identifying the magnetic flux associated with a circuit inductance provides visual insight for improving the coupling accuracy for the Isolated Analog Selector transformer.

Consider three single turn coils in free space, Coil 1 (primary), Coil 2 (secondary) and Coil 3 (tertiary). Assume the coils to have the same *z*-axis of symmetry, with Coils 1 and 2 having a similar location to the previous two winding illustrative examples and Coil 3 being the same size as Coil 2 and directly below Coil 2. The various magnetic fluxes are shown in Figure 6-9.

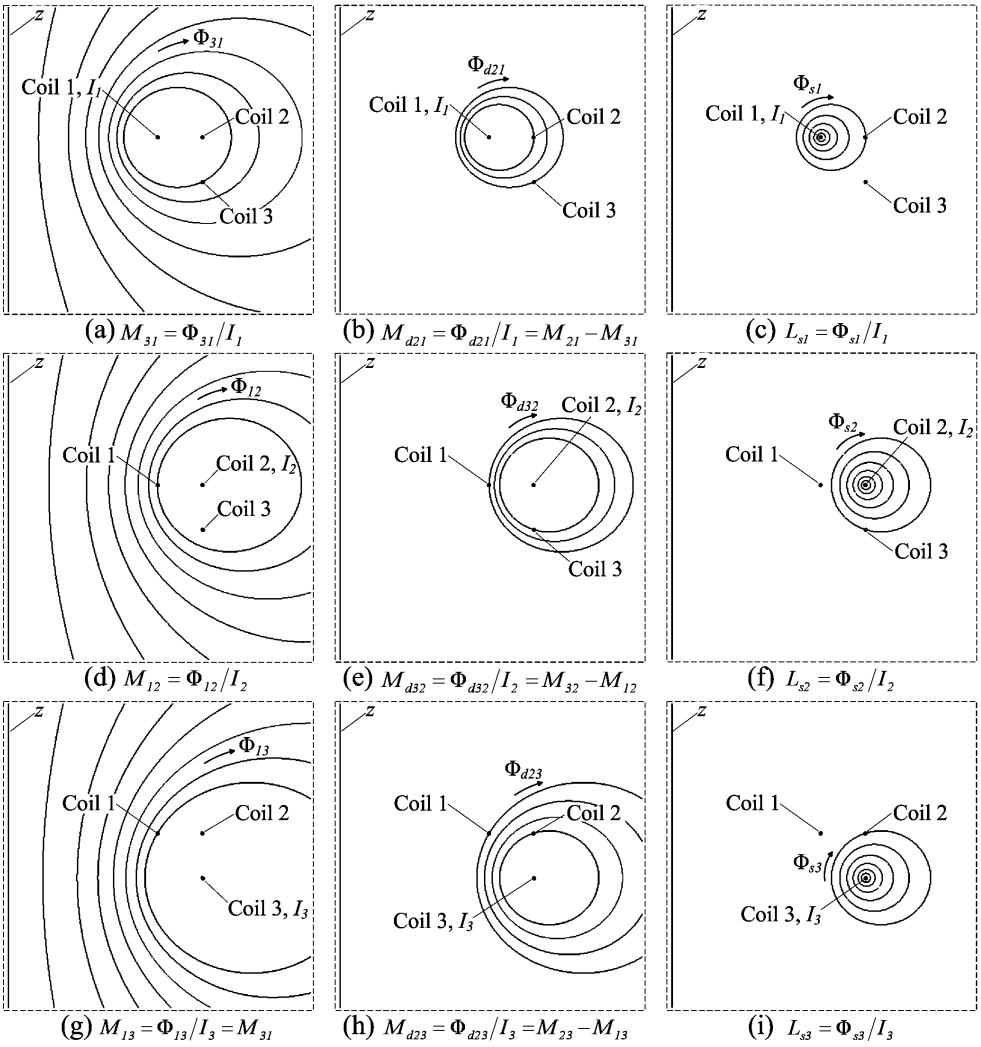

Figure 6-9: Magnetic flux and corresponding inductances associated with three single turn coils.

The leakage inductances, L_{s1}, L_{s2}, and L_{s3} are easily identified by the leakage fluxes Φ_{s1} (Figure 6-9(c)), Φ_{s2} (Figure 6-9(f)), and Φ_{s3} (Figure 6-9(i)). The magnetic flux of Figure 6-9(a) corresponds to the mutual inductance, M_{31}, between Coils 3 and 1 (from current solely in Coil 1). All of the magnetic flux of Figure 6-9(a) also couples to Coil 2. The additional magnetic flux that couples to Coil 2 (but not Coil 3) is shown in Figure 6-9(b) and corresponds to a difference inductance, $M_{d21} = M_{21} - M_{31}$.

Likewise, the magnetic flux of Figure 6-9(d) corresponds to the mutual inductance, M_{12}, coupling to Coil 1 from Coil 2. All of this magnetic flux also couples to Coil 3. The additional magnetic flux, Φ_{d32}, of Figure 6-9(e) couples to Coil 3 from Coil 2 (but not to Coil 1) and corresponds to a difference inductance, $M_{d32} = M_{32} - M_{12}$. And finally, the magnetic flux of Figure 6-9(g) corresponds to the mutual inductance, M_{13}, coupling to Coil 1 from Coil 3. By reciprocity, $M_{13} = M_{31}$. The additional magnetic flux, Φ_{d23}, of Figure 6-9(h) couples to Coil 2 from Coil 3 (but not to Coil 1) and corresponds to a difference inductance, $M_{d23} = M_{23} - M_{13}$.

Due to the reciprocity of the mutual terms, M_{12}, M_{13}, and M_{32}, there is always a relationship between the three difference fluxes, Φ_{d21}, Φ_{d32} and Φ_{d23}. For the three single turn coil example portrayed in Figure 6-9, the relationship between these three difference fluxes is: $\Phi_{d23} = \Phi_{d21} + \Phi_{d32}$. It is ideal if the three winding transformer circuit model is based on six inductances related to Figure 6-9.

One circuit model that makes physical sense and is usually straightforward to use for circuit simulation and analysis is the model shown in Figure 6-10 [28]. Just as with the two winding transformer, L_m is the magnetizing inductance and corresponds to magnetic flux essentially located in the core. However, with the three winding transformer the magnetizing inductance corresponds to flux that couples to all three windings for any combination of currents in the three windings.

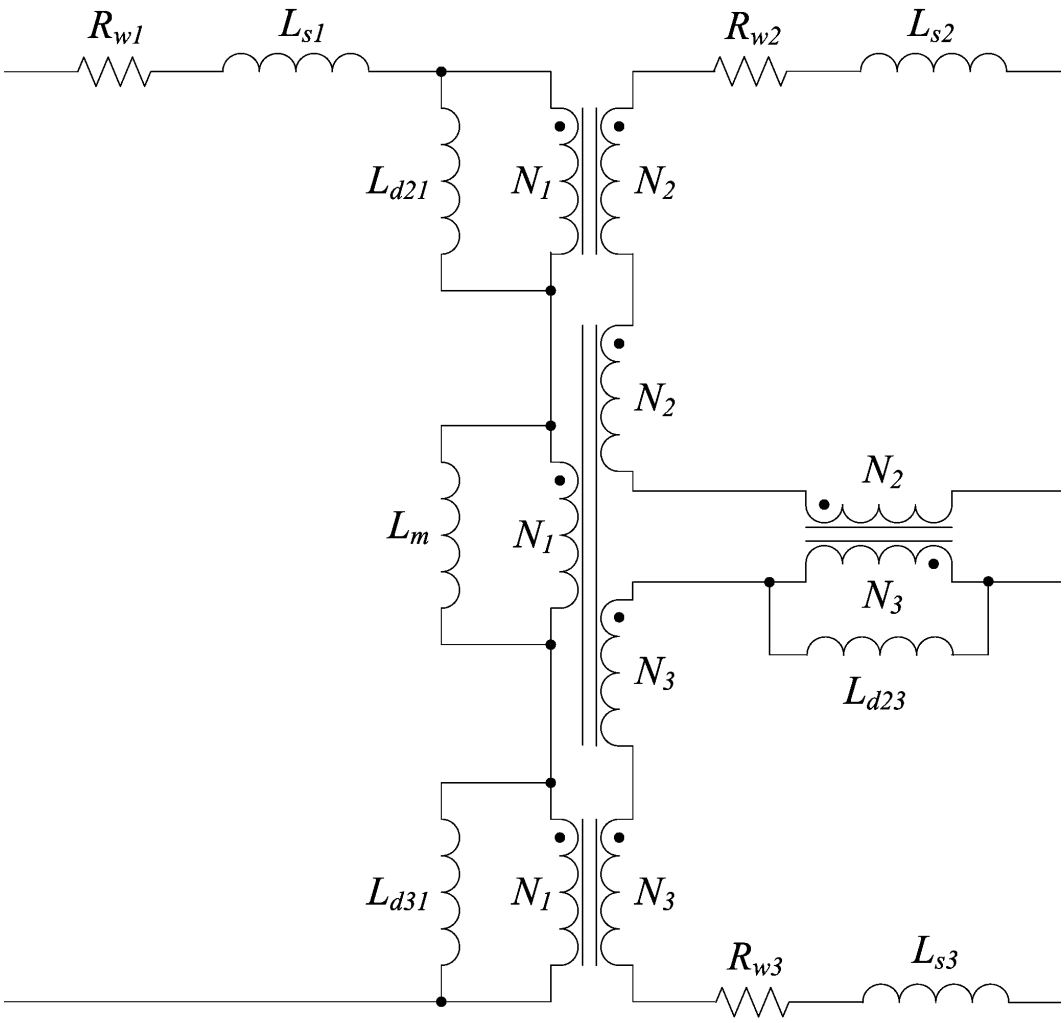

Figure 6-10: Three winding transformer equivalent circuit model.

L_m could be arbitrarily chosen to be any value (i.e., 0 to any large value). However, just as with the two winding model, certain values of L_m may result in negative inductance values for L_{d21}, L_{d31}, L_{d23}, L_{s1}, L_{s2}, or L_{s3}. The circuit model that makes the most physical sense is based on selecting L_m as:

$$L_m = \min\left(\frac{N_1}{N_2}M_{21}, \frac{N_1}{N_3}M_{31}, \frac{N_1^2}{N_2 N_3}M_{23}\right). \tag{6-9}$$

This will eliminate one of the inductance terms L_{d21}, L_{d31}, or L_{d23} leaving six inductances in the circuit model of Figure 6-10:

$$
\begin{aligned}
L_{d21} &= \frac{N_1}{N_2} M_{21} - L_m \\
L_{d31} &= \frac{N_1}{N_3} M_{31} - L_m \\
L_{d23} &= \frac{N_3}{N_2} M_{23} - \frac{N_3^2}{N_1^2} L_m \\
L_{s1} &= L_{11} - L_m - L_{d21} - L_{d31} \\
L_{s2} &= L_{22} - \frac{N_2^2}{N_1^2}\left(L_m + L_{d21}\right) - \frac{N_2^2}{N_3^2} L_{d23} \\
L_{s3} &= L_{33} - \frac{N_3^2}{N_1^2}\left(L_m + L_{d31}\right) - L_{d23}
\end{aligned}
\quad . \qquad \text{(6-10)}
$$

Using the circuit model of Figure 6-10, the coupling accuracy of the Isolated Analog Selector transformer of Figure 1-6 can be analyzed by assuming that winding 1 is the drive winding, winding 2 is the signal winding, and winding 3 is the sense winding. Since the compensation operational amplifier of Figure 1-6 will adjust the drive winding until the sense winding matches the LPF output voltage, the coupling error (assuming no error in the compensation operational amplifier circuit) is related to the flux that couples to the signal winding, but not the sense winding, corresponding to L_{d21} - L_{d31}, divided by the flux coupling to the sense winding, corresponding to $L_m + L_{d31}$:

$$
\text{Error} = \frac{L_{d21} - L_{d31}}{L_m + L_{d31}} = \frac{\frac{N_1}{N_2} M_{21} - \frac{N_1}{N_3} M_{31}}{\frac{N_1}{N_3} M_{31}} = \frac{N_3}{N_2} \frac{M_{21}}{M_{31}} - 1. \qquad \text{(6-11)}
$$

If $(N_1/N_2)M_{21} > (N_1/N_3)M_{31}$, then there is a positive error (more coupling to the signal winding than the sense winding resulting in a higher than ideal voltage on the signal winding). If $(N_1/N_3)M_{31} > (N_1/N_2)M_{21}$, then there is a negative error (less coupling to the

signal winding than the sense winding resulting in a lower than ideal voltage on the signal winding).

Using the FEA 2-D solver for the three single turn coil example portrayed in Figure 6-9, the resistance and inductance matrices are:

$$\mathbf{R} = \begin{bmatrix} R_{11} & 0 & 0 \\ 0 & R_{22} & 0 \\ 0 & 0 & R_{33} \end{bmatrix} = \begin{bmatrix} 0.108\,\Omega & 0 & 0 \\ 0 & 0.141\,\Omega & 0 \\ 0 & 0 & 0.141\,\Omega \end{bmatrix}$$
$$\mathbf{L} = \begin{bmatrix} L_{11} & M_{12} & M_{13} \\ M_{21} & L_{22} & M_{23} \\ M_{31} & M_{32} & L_{33} \end{bmatrix} = \begin{bmatrix} 32.4\,\text{nH} & 10.4\,\text{nH} & 8.2\,\text{nH} \\ 10.4\,\text{nH} & 44.2\,\text{nH} & 12.9\,\text{nH} \\ 8.2\,\text{nH} & 12.9\,\text{nH} & 44.2\,\text{nH} \end{bmatrix}, \quad \text{(6-12)}$$

and thus the transformer model element values are found and given in Figure 6-11.

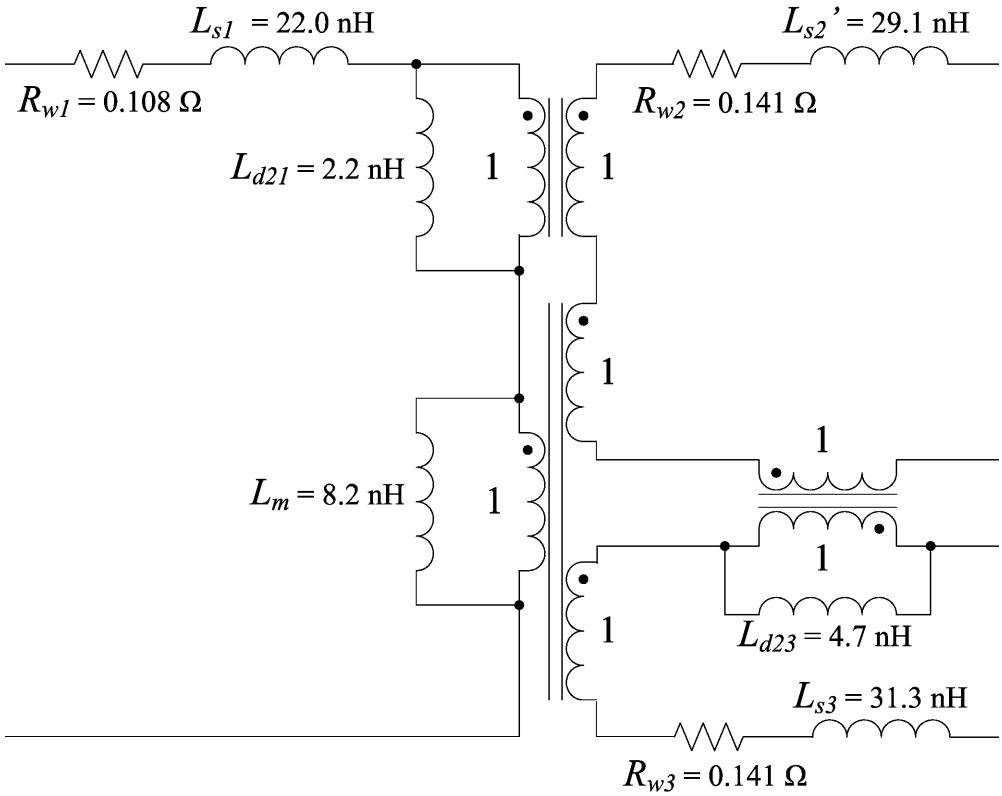

Figure 6-11: Transformer equivalent circuit model for three single turn coils.

Since L_m is chosen to be the minimum in (6-9), it is advantageous to indentify the flux corresponding to L_m when current is being driven by Coil 2. This flux along with the difference fluxes associated with Coil 2 is shown in Figure 6-12.

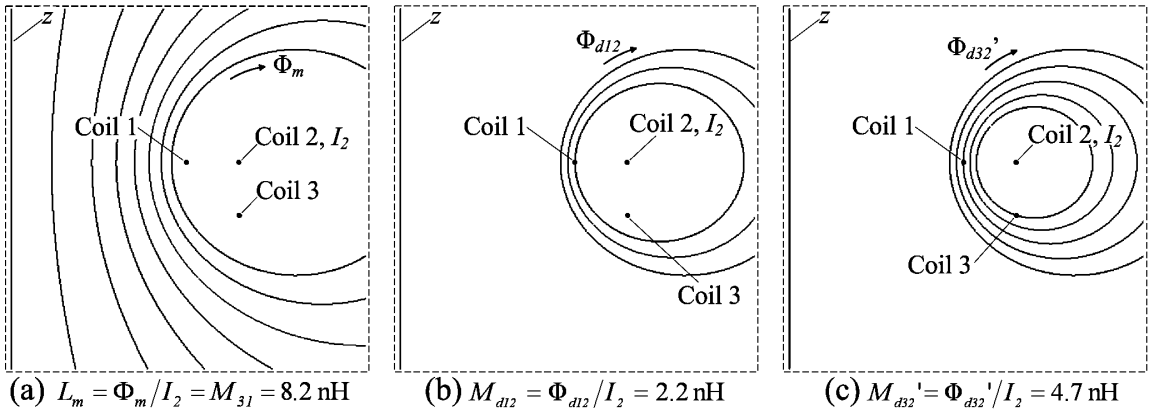

Figure 6-12: Magnetic flux associated with driving Coil 2 with I_2.

The inductances in the circuit model of Figure 6-11 correspond to the fluxes of Figure 6-9 and Figure 6-12. L_m corresponds to Figure 6-9(a), Figure 6-9(g), and Figure 6-12(a). L_{s1} corresponds to Figure 6-9(c) and L_{d21} corresponds to Figure 6-9(b) and Figure 6-12(b). L_{s3} corresponds to Figure 6-9(i) and L_{d23} corresponds to Figure 6-9(h) and Figure 6-12(c).

It turns out that L_{s2}' does not correspond to any of the fluxes of Figure 6-9 or Figure 6-12. Instead, it is related to the difference of the leakage flux of Figure 6-9(f), Φ_{s2}, minus the magnitude of the difference flux, Φ_{d12}, of Figure 6-12(b). This subtlety arises because the difference flux, Φ_{d12} (Figure 6-12(b)) couples all three windings and is also part of the difference flux, Φ_{d32}' (Figure 6-12(c)). It is also pictorially clear that $\Phi_{d32}' = \Phi_{d23} = \Phi_{d21} + \Phi_{d32}$ (the flux of Figure 6-12(c) is the combination of the fluxes of Figure 6-12(b) and Figure 6-9(e)).

In general, the circuit model of Figure 6-10 can be used for SPICE simulation for circuits containing a three winding transformer. However, there is a remote possibility that one of the leakage inductance terms (in the winding that has two difference inductances, L_{d21}, L_{d31}, or L_{d23}) may end up being slightly negative. A negative inductance is not possible to model in SPICE.

From (6-11), the magnetic coupling error for the Isolated Analog Selector transformer can be determined using two different methods. Given the inductance matrix, the error can be calculated as: Error = $1 - (N_2/N_3)(M_{31}/M_{21})$. This first method gives little insight into what can be done to reduce the error (other than the obvious: make M_{31} more equal to M_{21}).

The second method involves identifying the difference inductances, L_{d21} and L_{d31}, and the magnetizing inductance, L_m: Error = $(L_{d31} - L_{d21})/(L_m + L_{d21})$. This approach gives more insight into what can be done to reduce the error: 1) increase the magnetizing inductance, L_m (i.e. larger core cross-section, higher permeability or increased winding turns); or 2) move the windings around until the difference inductances, L_{d21} and L_{d31}, are nearly equal.

The Isolated Analog Selector transformer of Figure 3-2 has a minimum core size that still supports the volt-time product for bringing the voltage signal across the isolation barrier for enough time for proper A-D conversion. The number of drive, sense, and signal winding turns are also fixed based on the compensation operational amplifier circuit design and the number of printed circuit board traces that fit around the E-E core. And finally, the primary and secondary printed circuit boards are physically constrained by the plastic insulators and printed circuit board mounting hardware.

Therefore, the only degree of freedom to improve the magnetic coupling error (i.e., design L_{d21} to nearly equal L_{d31}) is to optimally locate the drive, sense and signal windings within the printed circuit board inner layers. The remainder of this chapter is devoted to analyzing and improving the magnetic coupling accuracy of the Isolated Analog Selector transformer.

6.2 Double 2-D Method

The FEA 2-D solver is used to analyze the coupling error between the drive to sense and drive to signal windings. This is accomplished by applying the double 2-D method [29] to the 3-D E-E core. The double 2-D method takes the 3-D E-E core and divides it into two rectangular 2-D models as shown in Figure 6-13.

Figure 6-13(a) shows how the windings are divided into two orthogonal segment sets. A 2-D model is constructed from these orthogonal segment sets as shown in Figure 6-13(b). The 2-D model on the left of Figure 6-13(b) is referred to as the lateral solution and the 2-D model on the right is referred to as the frontal solution. Each 2-D model is considered to be infinite in length in the third dimension. Therefore, the 2-D solver will result in fluxes and inductances that are per unit length.

The total 3-D solution is calculated by adding the results of the double 2-D solutions. For the flux (and corresponding inductance) associated with the E-E core, the per unit length 2-D frontal solution is multiplied by the thickness of the core material.

For the flux/inductance associated with the area outside the core (i.e. around the windings, E-E core window opening and sides of the core) the total 3-D solution is the sum of both double 2-D solutions. The per unit length frontal solution is multiplied by the mean length of the windings going through the windows (i.e., extends beyond the

thickness of the E-E core). This value is added to the per unit length lateral solution multiplied by the mean length of the windings on the side of the center leg of the E-E core (i.e., extends beyond the width of the center leg). The accuracy of the double 2-D method is better than 1.6% [29].

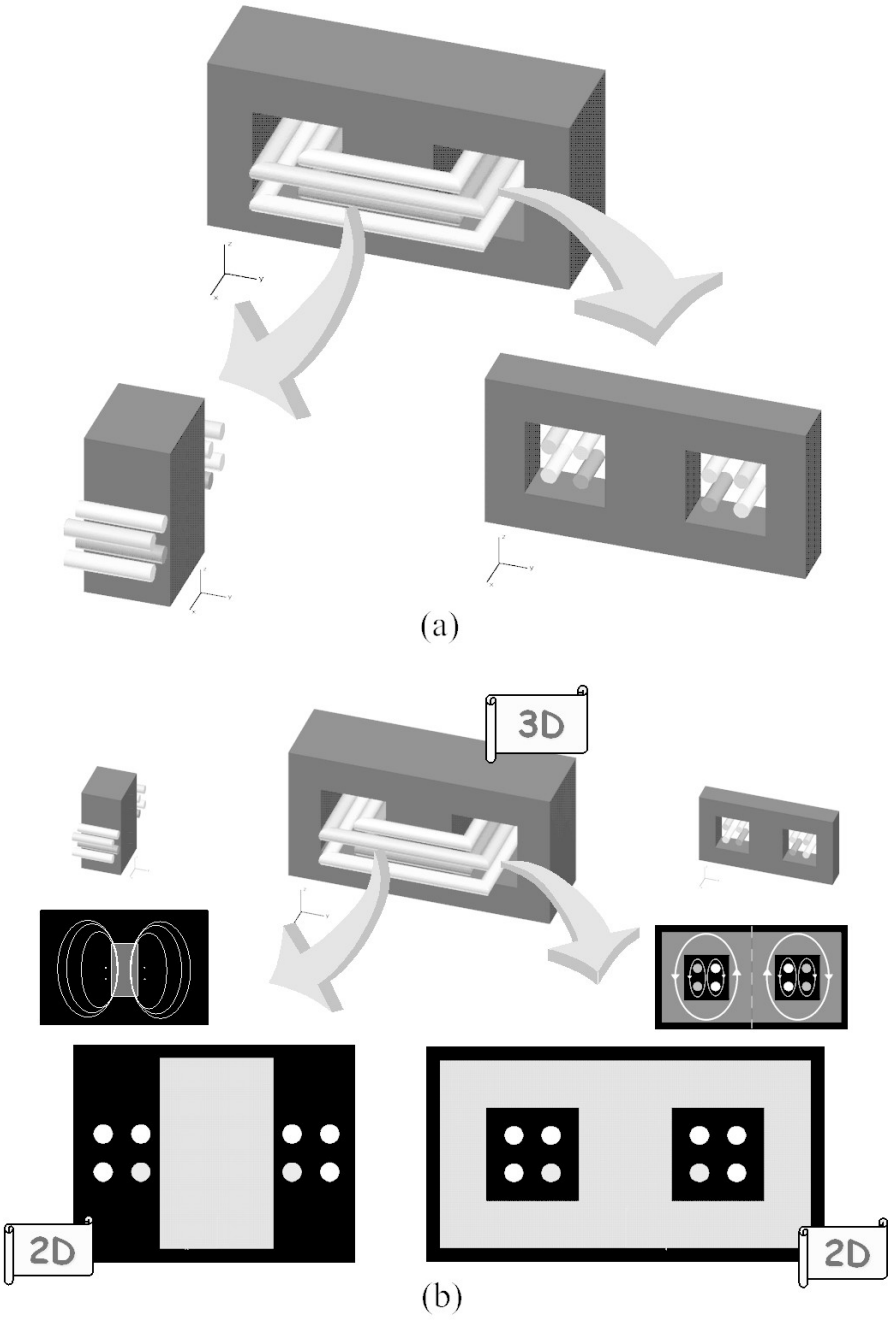

Figure 6-13: Double 2-D method: (a) division of windings and core into two orthogonal segment sets; (b) frontal and lateral 2-D solutions (Courtesy Roberto Prieto).

The frontal length for the Isolated Analog Selector transformer E-E ferrite core is 5.5 mm (thickness of the E-E core). The lateral length used is 10 mm, which is the mean length of the windings on the side of the center leg of the E-E core (even though the E-E core center leg width is only 4 mm).

6.3 Isolated Analog Selector Transformer Magnetic Coupling Accuracy Analysis

The FEA frontal and lateral models are constructed based on the physical dimensions of the E-E core, the physical placement of the windings within the printed circuit boards, the cross-section of printed circuit board traces, and the small gap between the two core halves as found in Table 4-1. The permeability of the core is set to the minimum value at –40 °C (μ_r = 2633). The magnetic coupling error is highest when the magnetizing inductance, L_m, is lowest.

Without the knowledge of the three winding transformer modeling presented earlier in this chapter, it may seem sensible to interleave the drive and sense windings in order to reduce the leakage inductance associated with these two windings. A double 2-D solution for this winding approach is shown in Figure 6-14.

Figure 6-14(a) shows the frontal solution and Figure 6-14(b) shows the lateral solution for the flux when current is flowing in the drive winding only. Since the drive and sense windings are interleaved, the magnetic coupling from the drive winding to the sense winding is going to be more than from the drive to signal windings, or $(N_1/N_3)M_{31} > (N_1/N_2)M_{21}$.

Figure 6-15 shows the mutual flux, Φ_{21} (Figure 6-15(a)), difference flux, Φ_{d31} (Figure 6-15(b)), and the leakage flux, Φ_{s1} (Figure 6-15(c)) for the frontal solution to the interleaved drive and sense windings. Figure 6-15(d), Figure 6-15(e) and Figure 6-15(f)

shows the same fluxes for the lateral solutions to the interleaved drive and sense windings. Since both solutions are symmetric about the plane of the vertical center, only the right half is shown in Figure 6-15.

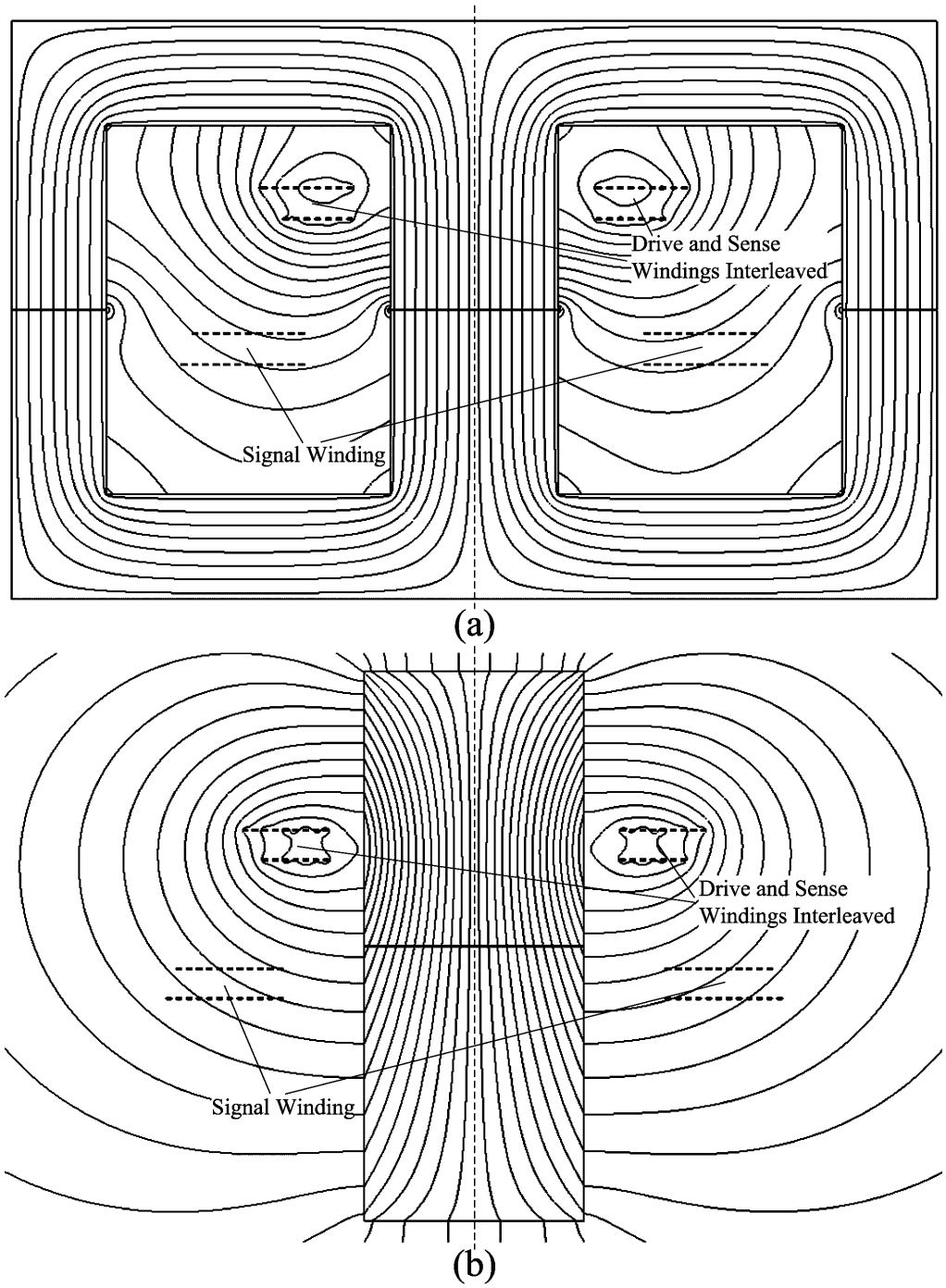

Figure 6-14: Double 2-D solution for Isolated Analog Selector transformer with interleaved drive and sense windings: (a) frontal solution; (b) lateral solution.

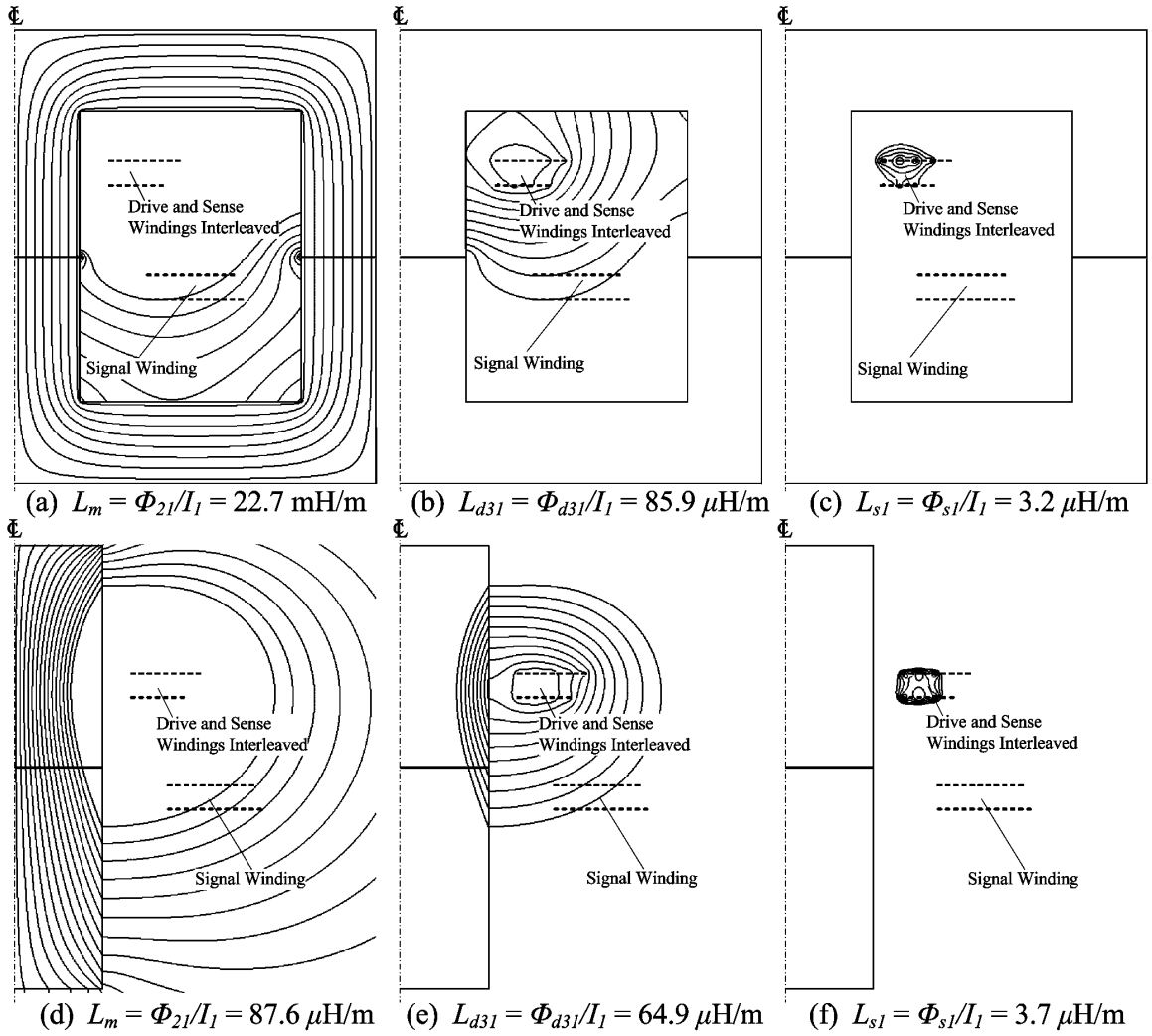

Figure 6-15: Magnetic flux and corresponding inductance associated with drive winding: (a), (b), (c) frontal solution; (d), (e), (f) lateral solution.

The frontal and lateral solutions of Figure 6-15 are combined first by multiplying the frontal solution by 5.5 mm (thickness of E-E core) and the lateral solution by 10 mm (mean length of the windings on the side of the center leg of the E-E core) and then adding the two results. The magnetic coupling error is calculated using (6-11): Error = $(L_{d31} - L_{d21})/(L_m + L_{d21})$. The results are shown in Table 6-1.

	Frontal	Lateral	Total
L_M	22.7 mH/m	87.6 μH/m	125.7 μH
L_{d31}	85.9 μH/m	64.9 μH/m	1.12 μH
L_{s1}	3.2 μH/m	3.7 μH/m	54 nH
Error	-0.38%	-0.29%	-0.88%

Table 6-1: Inductances and magnetic coupling error for interleaved drive and sense windings.

The total error shown in Table 6-1 of –0.88% represents a worst-case error at –40 °C. From Chapter 4, the magnetizing inductance, L_m, can range from 125 μH to 520 μH given the part-to-part variations, temperature variations, and the actual B-H characteristic path taken. The range of the error is therefore between –0.21% and –0.88%. Since the coupling error is dependent on the B-H characteristic path taken, it cannot be calibrated out. The only way to reduce this error is by adding more core material or changing the positioning of the windings.

The locations of the printed circuit boards are fixed by the plastic insulators of Figure 3-2. The signal winding takes up the entire two inner layers of the secondary printed circuit board of Figure 3-2, so there is no freedom to move the signal winding around. However, since there are additional power supply windings (shown in Figure 3-1), there is some freedom to move the drive and sense windings around on the inner two layers of the primary printed circuit board.

Figure 6-16 shows various placements of the drive and sense windings for the frontal and lateral solutions. Figure 6-16(a) and (d) shows the drive and sense windings interleaved near the center leg of the E-E core. Figure 6-16(b) and (e) shows the drive winding near the center leg of the E-E core and the sense winding close to the middle of the primary printed circuit board. And Figure 6-16(c) and (f) shows the optimum

placement of the drive and sense windings (drive winding near center leg, sense winding near output leg of the E-E core).

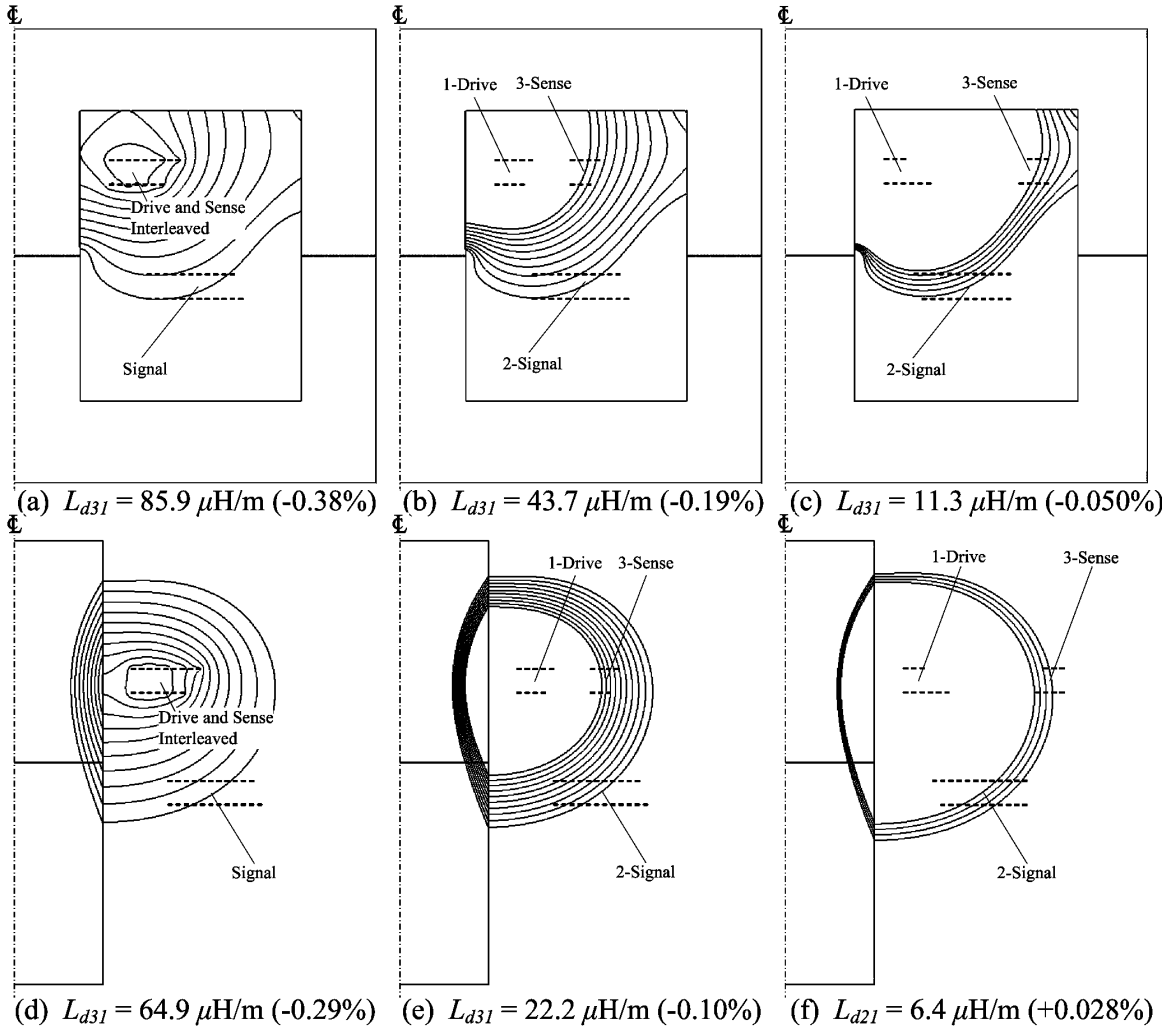

Figure 6-16: Magnetic flux associated with drive winding: (a), & (d) drive and sense windings interleaved; (b) & (e) sense winding near middle of printed circuit board; (c) & (f) sense winding near outer edge of printed circuit board (optimal).

As the sense winding is moved away from the drive winding, to a location where the flux coupling to the signal winding is also coupling to the sense winding, then the difference flux, Φ_{d31}, is minimized. Therefore, the optimum location for the drive and sense windings is iteratively determined by obtaining the frontal and lateral solutions and

combining the results to minimize the difference flux, Φ_{d21} or Φ_{d31}. The optimum location for the drive and sense windings is shown in Figure 6-16(c) and (f).

Sense Winding Location	Frontal	Lateral	Total
Interleaved	-0.38%	-0.29%	-0.88%
Middle	-0.19%	-0.10%	-0.37%
Optimal	-0.050%	+0.028%	0.002%

Table 6-2: Magnetic coupling error for various locations of the sense winding.

The magnetic coupling error associated with the optimum placement of the drive and sense winding is from 0.0005% to 0.002%, depending upon the part-to-part and temperature variations.

There are variations in the printed circuit board locations due to mechanical tolerances in the plastic insulators and printed circuit board mounting hardware. The printed circuit boards can move from side to side by ±10 mils and up and down by ± 5 mils. There is little variation in the location of the traces within the printed circuit boards themselves due to the printed circuit board etching process. Overall, the magnetic coupling error (widened further by the mechanical tolerances) is from –0.040% to +0.033%.

The overall magnetic coupling error is twice as large as the ±0.02% goal. However, once the isolation transformer has been assembled and the acquisition system calibrated, the change in error due to mechanical changes is minimal.

Chapter 7 Prototype Testing and Results

7.1 Prototype Overview

Two Isolated Analog Selector circuits were incorporated into an existing digital protective relay (the SEL-421 [2]). One internal VT (channel VAY) and one internal CT (channel ICX) were removed (conceptually shown in Figure 1-1). The VT was replaced with a voltage divider and an Isolated Analog Selector circuit and the CT was replaced with a shunt resistor and an Isolated Analog Selector circuit (conceptually shown in Figure 1-3).

A microcontroller was added to the SEL-421 digital protective relay. The purpose of the microcontroller is to synchronize to the SEL-421's acquisition system and generate the positive and negative switch control signals (shown in Figure 2-1 and Figure 2-2) for the two Isolated Analog Selector circuits. The inside of the SEL-421 with the added prototype circuitry is shown in Figure 7-1.

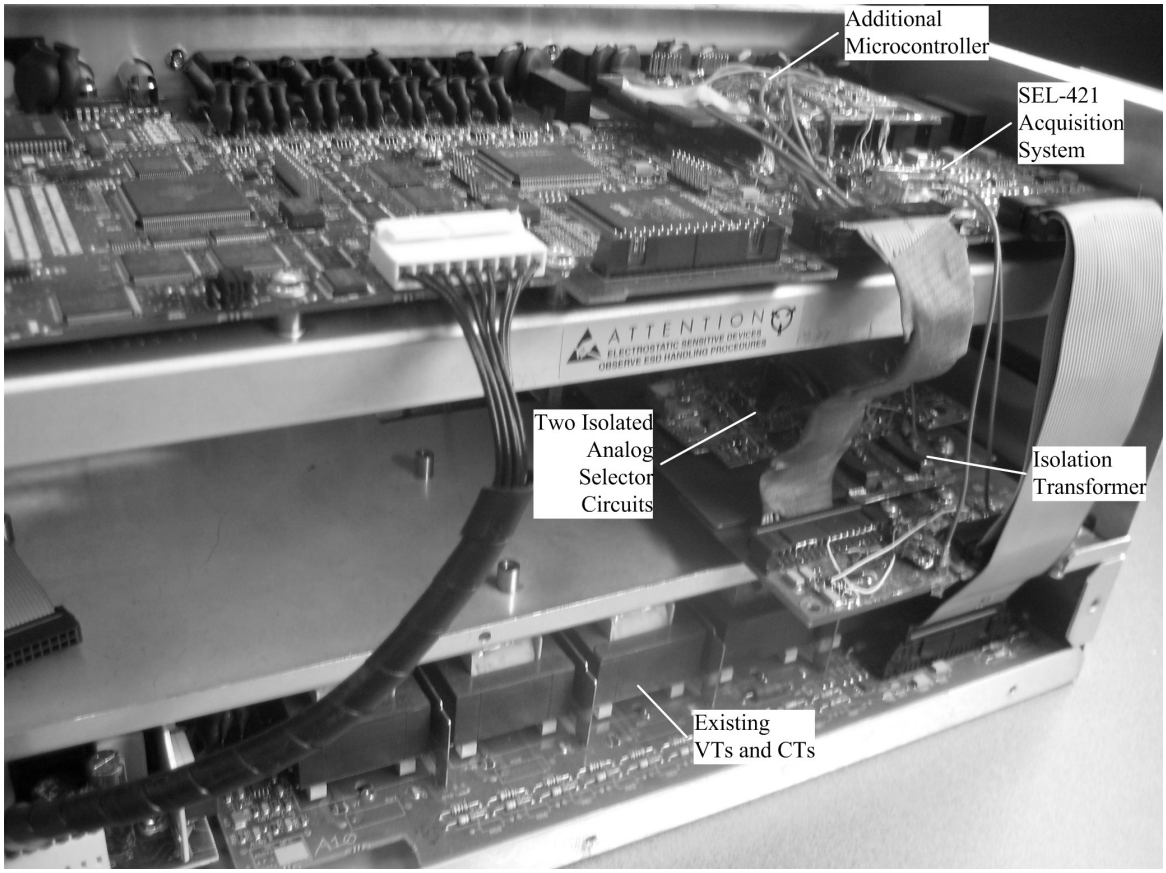

Figure 7-1: Two Isolated Analog Selector prototype circuits added to the SEL-421 (replacement of one VT and one CT).

The 60 Hz voltage signals, for the traditional SEL-421 VTs and CTs, are passed up the ribbon cable (located on the left of Figure 7-1) from the lower printed circuit board to the upper printed circuit board. The SEL-421 acquisition system (LPF and A-D converter) is located on this upper printed circuit baord.

The isolation transformer of Figure 3-2, used in Isolated Analog Selector prototype was constructed with a primary and secondary prototype printed circuit board. The prototype printed circuit board contains the necessary drive, sense, signal and power supply windings and Faraday shields. A single prototype plastic insulator (instead of the two shown in Figure 3-2) was constructed and used to provide the proper spacing

between the primary and secondary printed circuit boards. Conceptually, the isolation transformer is shown in Figure 7-2.

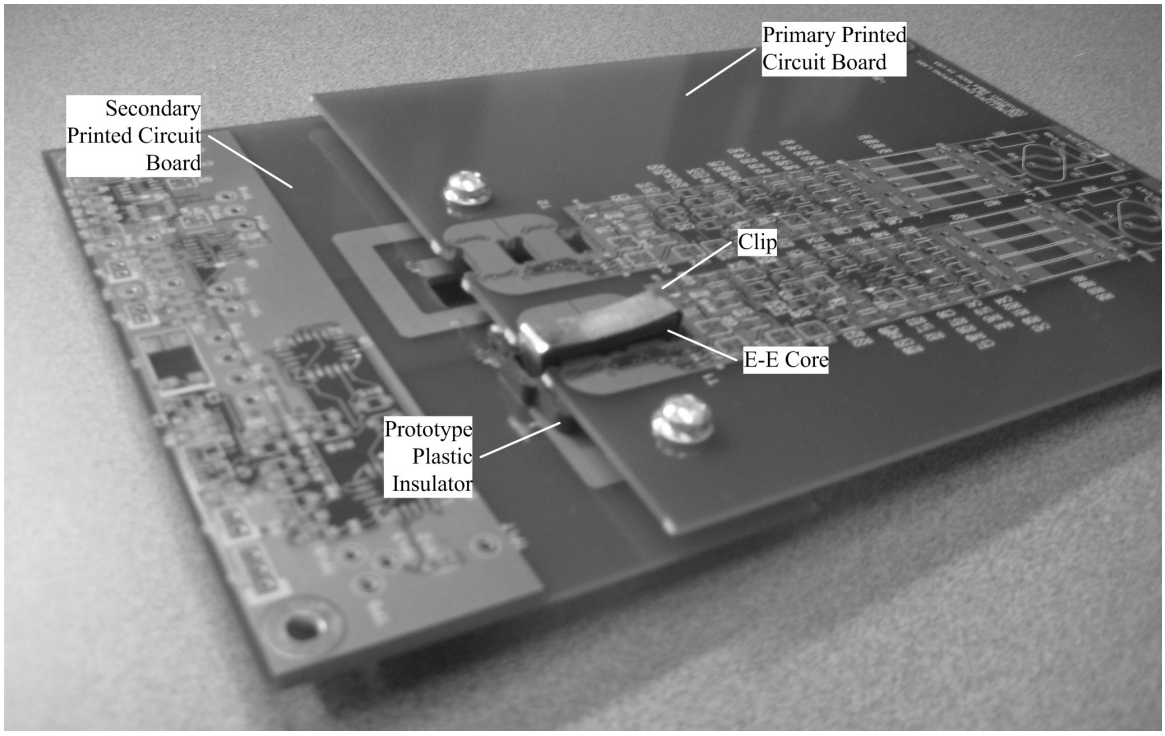

Figure 7-2: Isolation transformer conceptual prototype.

The circuitry for each Isolated Analog Selector is bread boarded on separate printed circuit boards and connected to the windings of the isolation transformer. Some of the key circuit blocks for the Isolated Analog Selector circuits are shown in Figure 7-3.

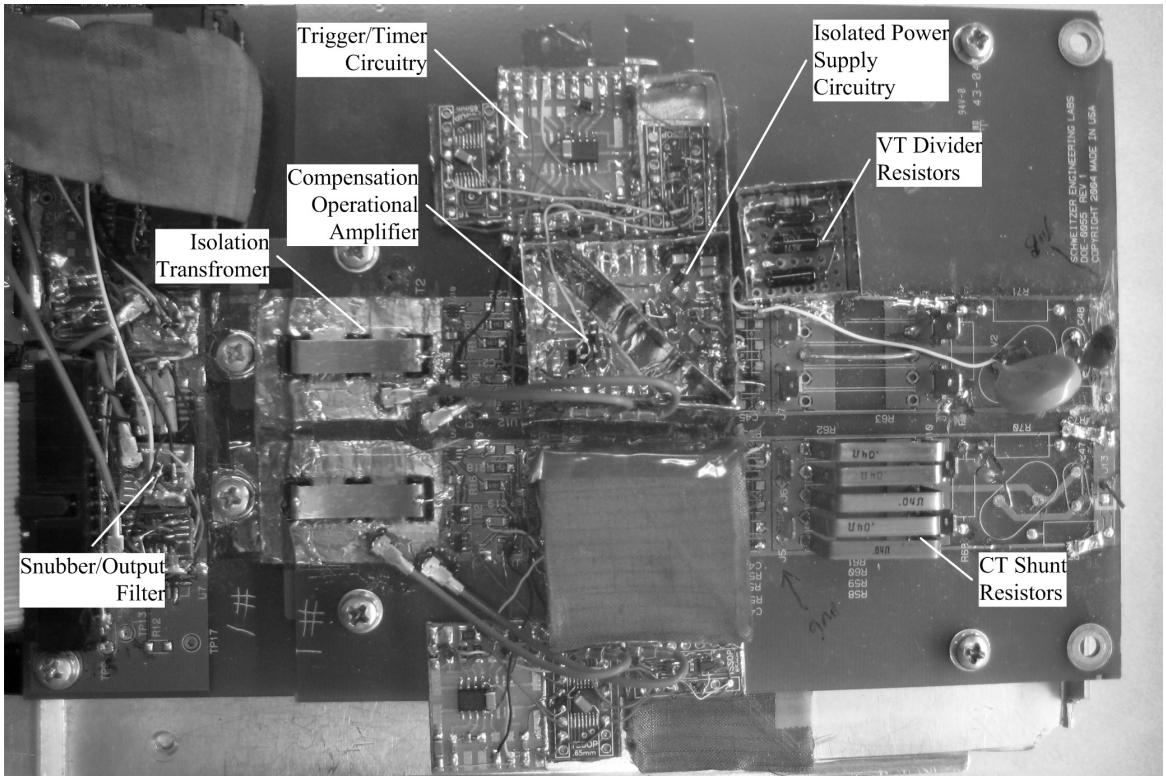

Figure 7-3: Isolated Analog Selector prototype circuitry.

The prototype circuit of Figure 7-3 shows the two Isolated Analog Selector circuits and isolation transformer. The top half shows the circuitry for the VT channel (VAY) and the bottom half shows the circuitry for the CT channel (ICX). Some oscilloscope captures of the Isolated Analog Selector signal winding (VAY) are shown in Figure 7-4. These signals are similar to the timing diagram shown in Figure 2-2. Figure 7-4(a) shows the signal winding when a positive full scale voltage is present at the output of the LPF, V_{LPF}. A-D conversion occurs after the signal has settled.

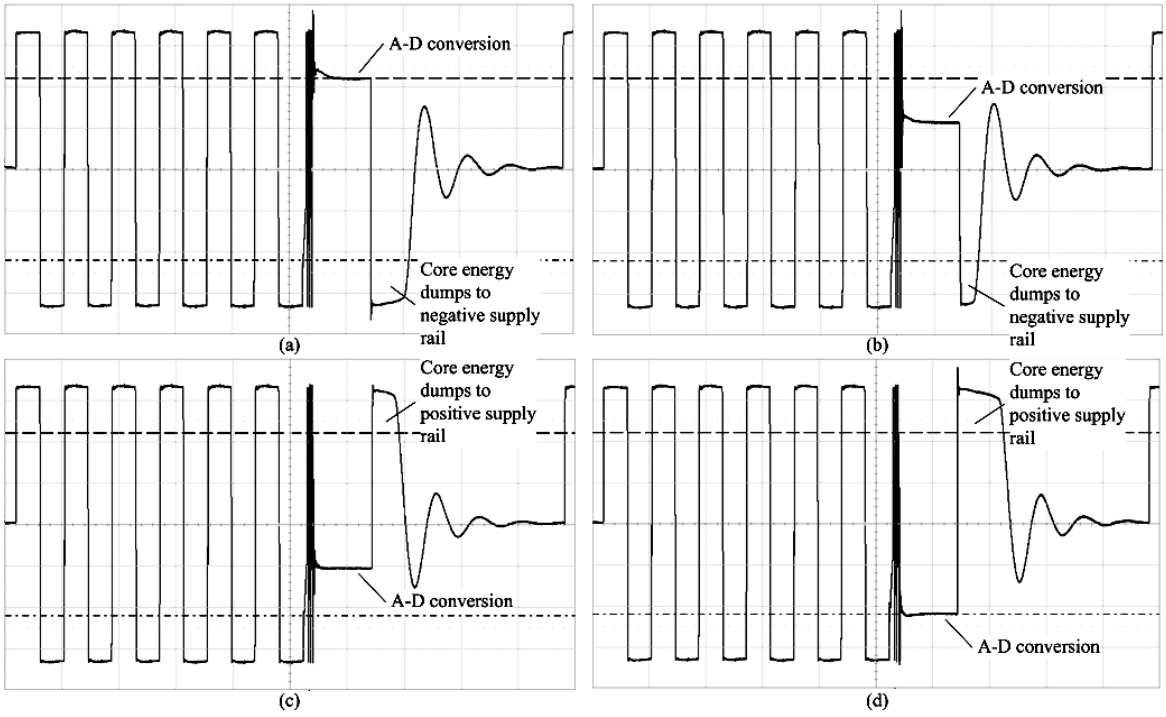

Figure 7-4: Oscilloscope captures of Isolated Analog Selector signal winding, V_{LPF} = : (a) + full scale; (b) +½ full scale; (c) –½ full scale; (d) – full scale.

Figure 7-4(b), (c), and (d) shows the signal winding when a positive ½ full scale, negative ½ full scale, and negative full scale are present at V_{LPF} respectively. Energy that is in the core, when the compensation operational amplifier is disabled, dumps into the positive or negative supply rail as shown in Figure 7-4. These supply rails are part of the power supply bridge rectifier and regulator circuit of Figure 2-1.

The oscilloscope capture of a step response (2.5 V) for the signal winding and output voltage of the Isolated Analog Selector is shown in Figure 7-5. These waveforms are very similar to the SPICE simulation waveforms of Figure 5-56. Therefore, the SPICE model schematic of Figure 5-54 adequately models the prototype circuitry.

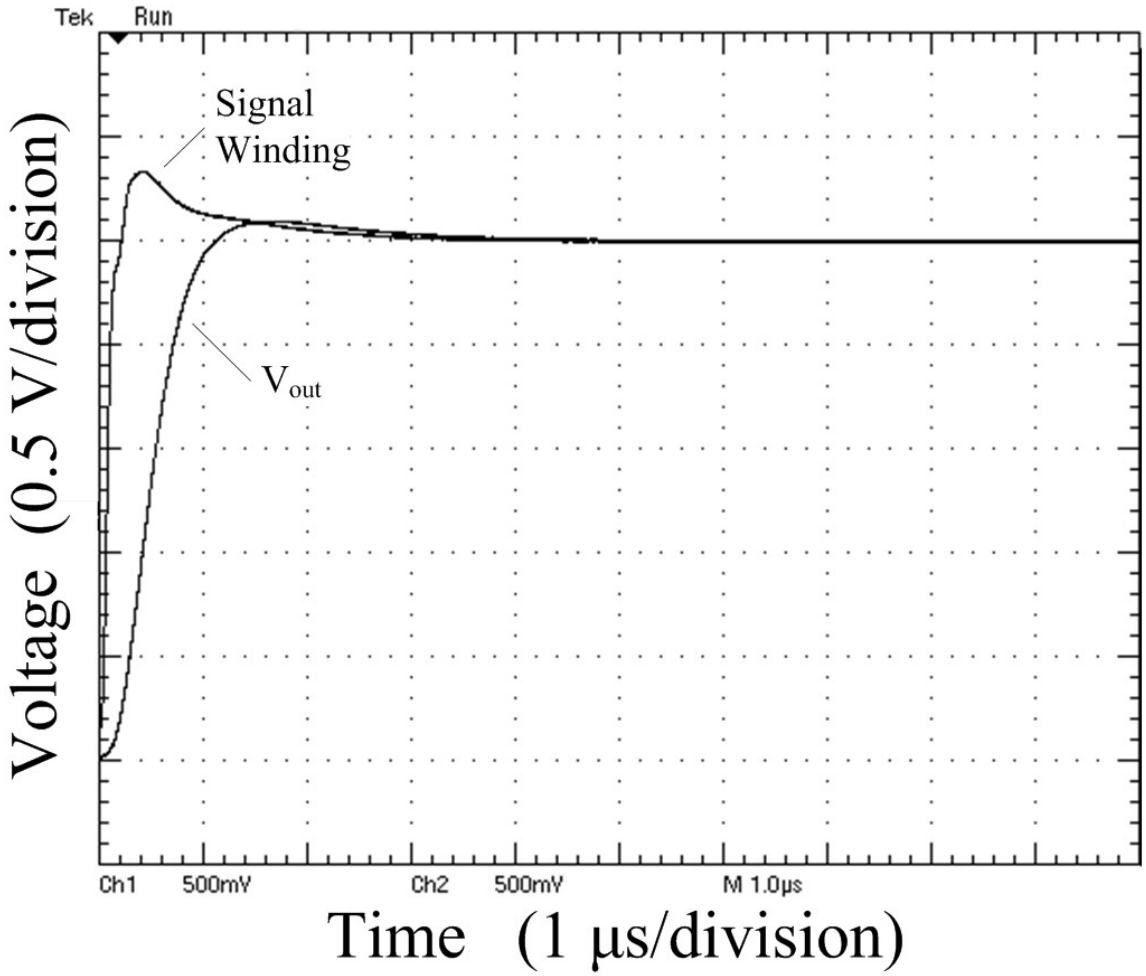

Figure 7-5: Oscilloscope capture: step response of signal winding and Isolated Analog Selector output voltage, V_{out} (2.5 V step, 10 µs).

The SEL-421 samples each channel at a rate of 8000 samples per second. For a 60 Hz VT signal, this corresponds to around 133 samples per cycle. Figure 7-6(a) shows the sampled data obtained from the SEL-421, VAY channel (Isolated Analog Selector circuit) for a VT signal of 350 V_{rms}. A spectral analysis of the sampled data is shown in Figure 7-6(b). There is virtually no difference between the spectral analysis of the Isolated Analog Selector VT channel and the traditional VT channel.

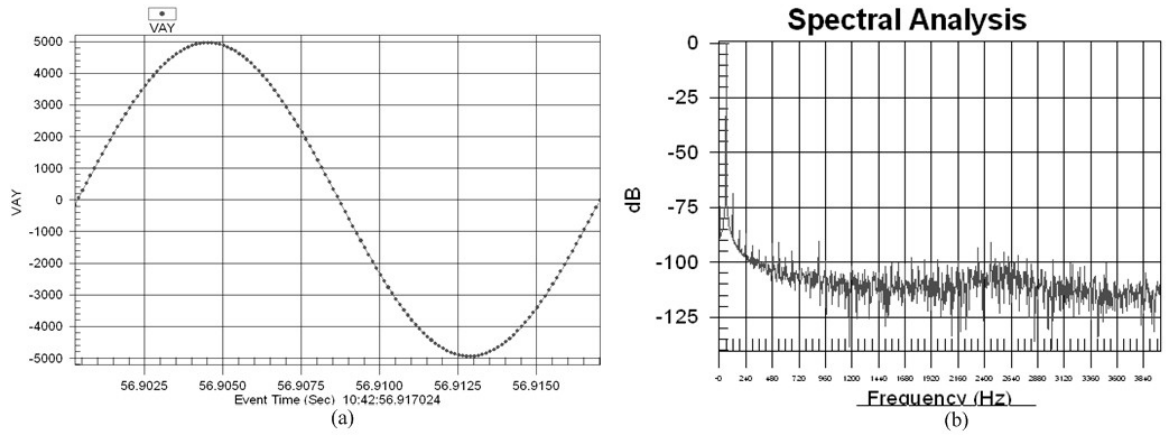

Figure 7-6: Sampled data from SEL-421 with 350 V_{rms} applied to VAY (Isolated Analog Selector channel).

Similarly, the Isolated Analog Selector signal for the CT channel closely resembles the traditional CT channel. The noise present in the A-D converter samples, when zero volts or amps are applied to VTs and CTs, are similar (about ± 3 to 4 A-D counts) for both the Isolated Analog Selector and traditional SEL-421 channels. The next section provides the test results of the Isolated Analog Selector, VT and CT channels compared to the traditional VT and CT channels at room temperature and the temperature extremes of –45 °C and 90 °C.

7.2 Accuracy Results Over Temperature

The overall metering accuracy requirement for the VT channel is ±0.1% ±8 mV ±60 ppm/°C (0 to 300 V_{rms}). The ±8 mV (rms) is almost ±2 counts of the 16-bit A-D converter. The VT channel is calibrated at room temperature at 60 V_{rms} (single point calibration). At the temperature extremes of –45 °C and 90 °C, the accuracy requirement is approximately ±0.5% ±8 mV (accounting for the ±60 ppm/°C and temperature deviation from room temperature). The prototype Isolated Analog Selector circuit, in combination with a VT resistor divider, and the traditional SEL-421 VT were tested at

the temperature extremes. The % error over the VT input range through 300 V_{rms} is shown in Figure 7-7.

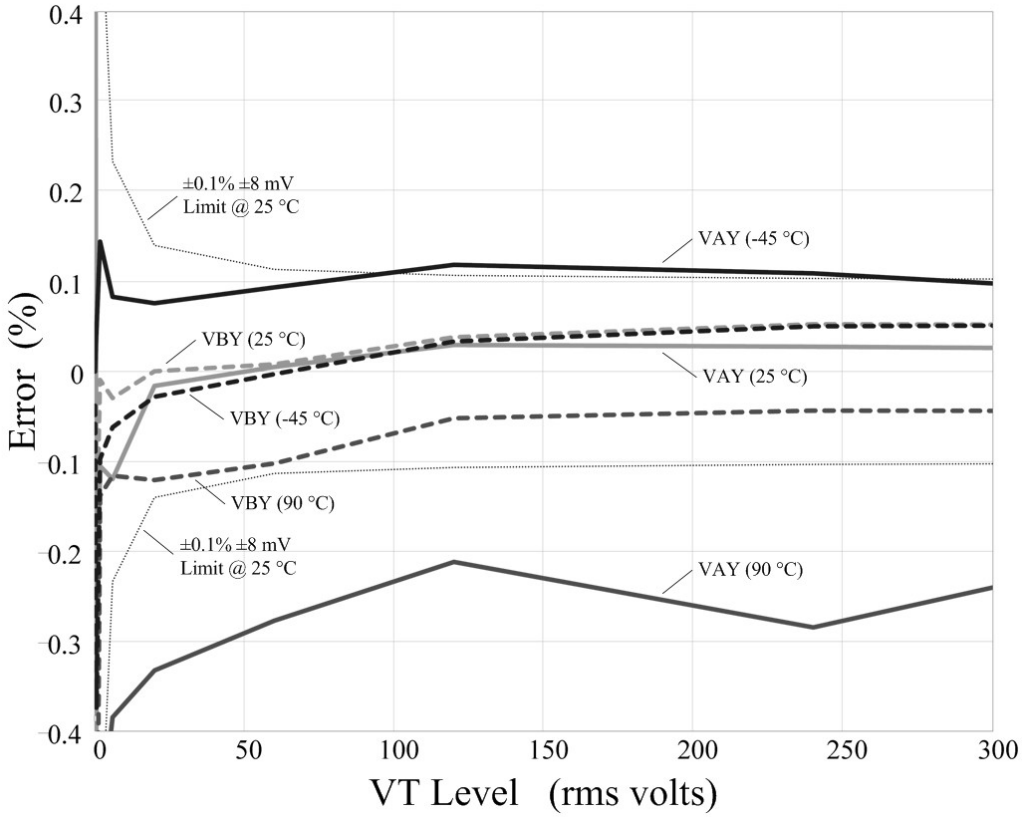

Figure 7-7: VT accuracy. VAY: Isolated Analog Selector VT, VBY: Traditional SEL-421 VT.

At room temperature (25 °C), the Isolated Analog Selector VT and traditional SEL-421 VT have similar errors and are both within the error limits. At temperature extremes, the Isolated Analog Selector VT has three to five times the error compared to the traditional SEL-421 VT. Most of the error at the temperature extremes is a result of the divider resistors used for the Isolated Analog Selector VT. These resistors have a temperature coefficient of ±50 ppm/°C.

The performance of the traditional SEL-421 VT is solid over the input voltage range and temperature extremes. Although the Isolated Analog Selector VT channel does not

achieve the same accuracy as the traditional VT channel, it is still well within the requirements of ±0.1% ±8 mV ±60 ppm/°C.

The overall metering accuracy requirement for the CT channel is ±0.1% ±4 mA ±60 ppm/°C (0 to 30 A_{rms}). The ±4 mA (rms) is almost ±2 counts of the 16-bit A-D converter. The CT channel is calibrated at room temperature at 10 A_{rms} (single point calibration). At the temperature extremes of –45 °C and 90 °C, the accuracy requirement is approximately ±0.5% ±4 mA (accounting for the ±60 ppm/°C and temperature deviation from room temperature). The prototype Isolated Analog Selector circuit, in combination with a CT shunt resistor, and the traditional SEL-421 CT were tested at the temperature extremes. The % error over the CT input range through 30 A_{rms} is shown in Figure 7-8.

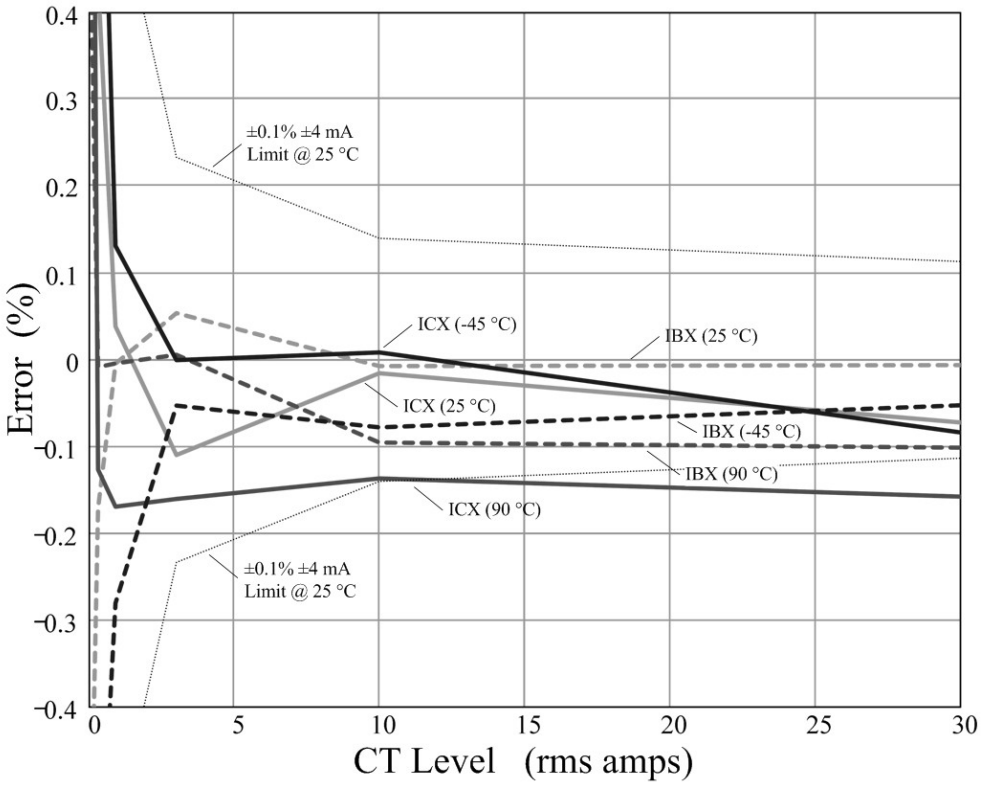

Figure 7-8: CT accuracy. ICX: Isolated Analog Selector CT, IBX: Traditional SEL-421 CT (through 30 A_{rms}).

At room temperature (25 °C), the Isolated Analog Selector CT and traditional SEL-421 CT have similar errors and are both within the error limits. At temperature extremes, the Isolated Analog Selector CT has a slightly greater error compared to the traditional SEL-421 CT. Most of the error at the temperature extremes is a result of the shunt resistor used for the Isolated Analog Selector CT. This resistor has a temperature coefficient of ±20 ppm/°C.

At around 10 to 15 A_{rms}, the shunt resistor begins to have a heat rise above the ambient temperature (due to the current flow), causing the resistance to decrease. To minimize the heat rise during test measurements, the current was applied for approximately 20 cycles for currents above 10 A_{rms}. Magnitude data for both CT channels were acquired from the SEL-421 every cycle and averaged for four cycles (after the magnitude data had risen to applied current level). The % error over the CT input range through 175 A_{rms}, at temperature extremes, is shown in Figure 7-9.

At 90 °C, the error is approaching the metering accuracy limit above 100 A_{rms}. However, the metering range is only through 30 A_{rms}. The accuracy requirement for the relaying elements associated with these type of current levels is ±3% ±0.05 A_{rms}.

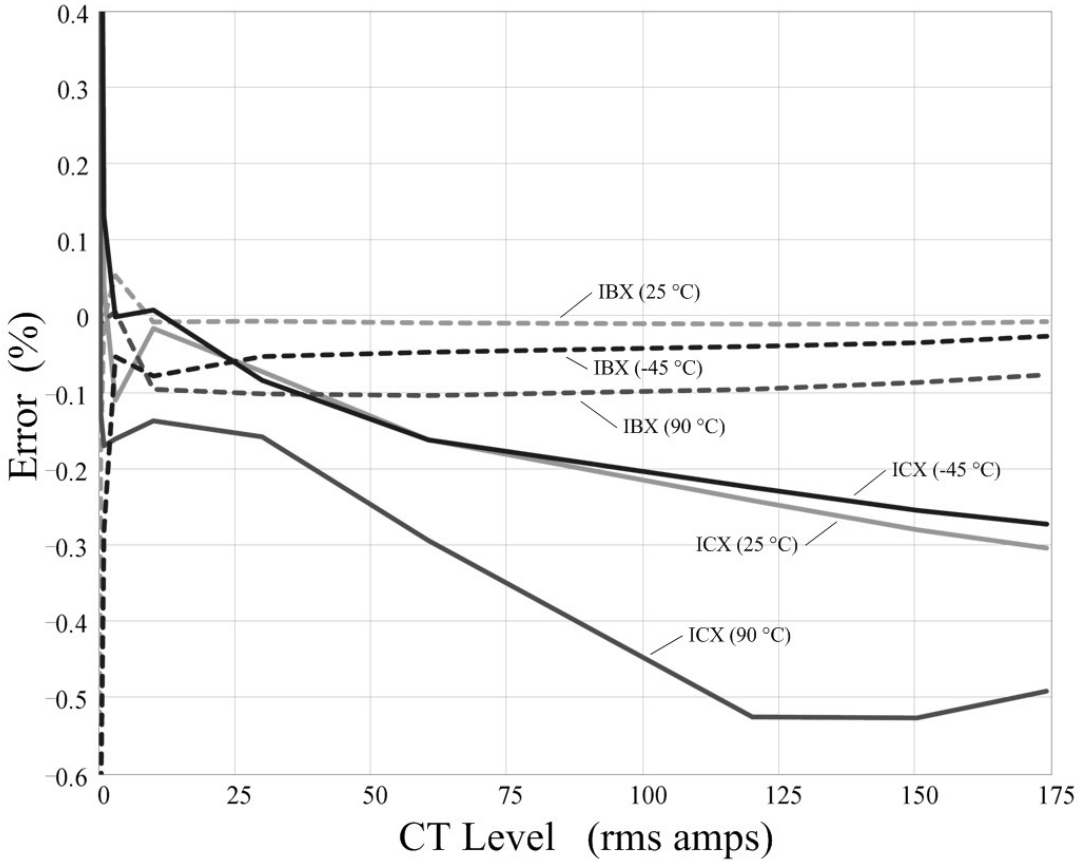

Figure 7-9: CT accuracy. ICX: Isolated Analog Selector CT, IBX: Traditional SEL-421 CT (through 175 A_{rms}).

7.3 Common Mode Rejection Performance

Common mode voltages present on the VT inputs appear across the isolation barrier of the isolation transformer (for both the traditional SEL-421 VT and the Isolated Analog Selector VT). A comparison between the common mode rejection performance of the traditional SEL-421 VT and the Isolated Analog Selector VT was made. The CMRR (Common Mode Rejection Ratio) was measured from 60 Hz through 30 MHz and the results are given in Figure 7-10.

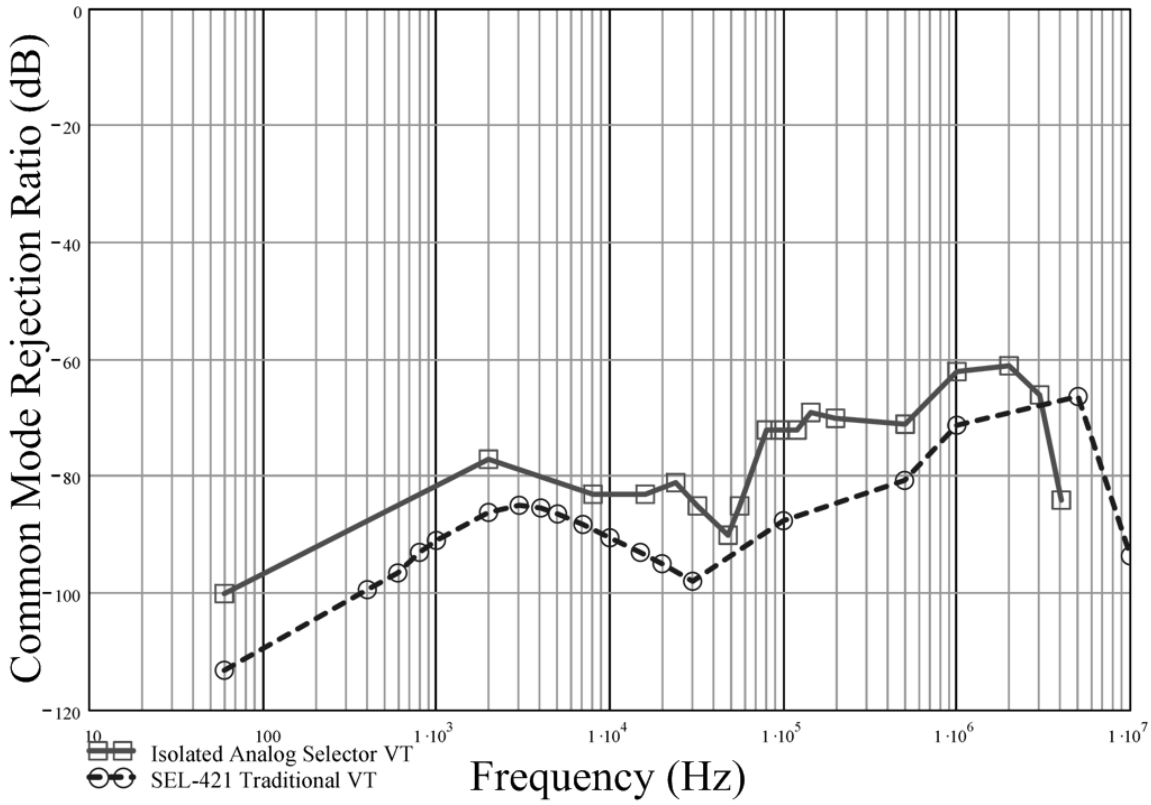

Figure 7-10: Common Mode Rejection Ratio for Isolated Analog Selector and traditional VT.

The traditional SEL-421 VT has excellent CMRR and is primarily a result of the construction of the voltage transformer. The Isolated Analog Selector also achieves good CMRR. The isolation transformer of the Isolated Analog Selector circuit must have the Faraday shields protecting the drive, sense, signal, and power supply windings as shown in Figure 3-1 and Figure 3-2.

The VT resistor divider, LPF, and compensation operational amplifier must also be placed in shields to achieve the CMRR shown in Figure 7-10. The prototype shields can be seen in Figure 7-3 (although the top lids have been removed for this picture).

It was also determined through testing that the symmetry of the E-E core's metal clip and the Faraday shield printed circuit board planes played a role in the common mode rejection performance. The Faraday shields cannot make a completed turn around any of

the legs of the E-E core (otherwise the core leg would be shorted out). Therefore, slits must be placed in the Faraday shields as shown in Figure 3-2.

When common mode signals are applied to the Isolated Analog Selector circuit, the common mode voltage appears across the isolation barrier. An isolation capacitance exists because of the overlapping of the primary and secondary printed circuit boards. Displacement current flows in this barrier capacitance due to the applied common mode voltage. The displacement current is supplied by conduction current flowing on the Faraday shields, E-E core clip (i.e. any conductive material). It is important that this conduction current is symmetrical about the E-E core, with the plane of symmetry lining up with the Faraday shield slits shown in Figure 3-2. Asymmetrical conduction current may result in magnetically inducing an unwanted signal on the sense or signal windings, resulting in a reduced CMRR.

7.4 Type Test Performance

Digital protective relays are required to pass a number of electrical disturbance type tests. ESD (Electrostatic Discharge), EFT/B (Electrical Fast Transient/Burst), RFI (Radio Frequency Interference), Surge Immunity, and SWC (Surge Withstand Capability) type tests were performed on the modified SEL-421 with the Isolated Analog Selector VT and CT channel. The type test, test standard performed, and severity level for each type test performed is given in Table 7-1.

Type Test	Standard	Severity Level
ESD	IEC 61000-4-2 IEEE C37.90.3	8 kV contact, 15 kV air
EFT/B	IEC 61000-4-4	4 kV at 2.5 and 5 kHz
RFI	IEEE C37.90.2	35 V/m (10 MHz to 3 GHz)
Surge Immunity	IEC 61000-4-5	0.5 and 1.0 kV Line-to Line 0.5, 1.0, and 2.0 kV Line-to-Earth
SWC	IEC 60255-22-1 IEEE C37.90.1	2.5 kV common mode 1 kV differential mode 2.5 kV Oscillatory 4 kV Fast Transient

Table 7-1: Type test performed on SEL-421 with Isolated Analog Selector prototype VT and CT channels.

The VT channels were tested by applying 67 V_{rms} and setting the protective relay over and under voltage elements to 70 V_{rms} and 64 V_{rms}, respectively. These over and under voltage settings are ± $3V_{rms}$ from the applied voltage (i.e. ±3% ±1 V_{rms}). The CT channels were tested by applying 3.75 A_{rms} and setting the protective relay over and under current element to 3.58 A_{rms} and 3.92 A_{rms}, respectively. These over and under current settings are ±0.17A_{rms} from the applied current (i.e. ± 3% ±0.05 A_{rms}).

The SEL-421, with the prototype Isolated Analog Selector circuits for the VAY and ICX channels, passed the electrical disturbance type tests of Table 7-1. Passing the type tests requires that none of the over/under voltage/current protective relay elements pick up while the electrical disturbance is applied.

Margin type testing was also performed on the prototype circuitry. For margin testing, the over voltage/current element settings are decreased and the under voltage/current element settings are increased until the relay element(s) pick up for the particular electric disturbance. The margin is considered the difference between original over/under element setting that passes and the new setting that does not pass.

The type test margins for the Isolated Analog Selector and SEL-421 traditional VT and CT channels were obtained and are given in Table 7-2.

Type Test	ISOLATED ANALOG SELECTOR		Traditional	
	VT (V_{rms})	CT (A_{rms})	VT (V_{rms})	CT (A_{rms})
ESD	2.5	0	2.85	0.15
EFT/B	1.5	0.07	2.7	0.15
RFI	2.75	0.15	2.85	0.15
Surge Immunity	1	0.12	0.5	0.15
SWC	2.5	0	2.85	0.15

Table 7-2: Type test margin results for the Isolated Analog Selector and SEL-421 traditional VT and CT channels.

Improving the type test margins is difficult using the prototype circuitry shown in Figure 7-3 and may not accurately reflect the performance in an actual product. Further type test margin improvements may be achieved once the Isolated Analog Selector circuitry is placed on printed circuit board assemblies within a given protective relay product.

7.5 Channel to Channel Crosstalk Performance

The isolation transformers of the Isolated Analog Selector prototype circuits for VAY and ICX have around one inch separation (center to center) shown in Figure 7-3. There is some magnetic coupling/crosstalk between VAY and ICX due to the proximity of the printed circuit board windings of both isolation transformers.

The SEL-421 acquisition system channels are sampled in a fixed order: IAW, IBW, ICW, IAX, IBX, ICX, VAY, VBY, VCY, VAZ, VBZ and VCZ. Since VAY follows ICX, it is enabled around 5.5 μs after VAY is enabled. Therefore, while ICX is being sampled by the A-D converter, VAY is enabled and in the process of settling.

The crosstalk from channel VAY to ICX was measured with an oscilloscope by zooming in on the ICX channel signal during the time the A-D converter is sampling, while varying the voltage applied to the VAY channel. The oscilloscope was set to infinite persistence to capture the crosstalk due to the varying VAY signal. The oscilloscope capture of the crosstalk from VAY to ICX is shown in Figure 7-11.

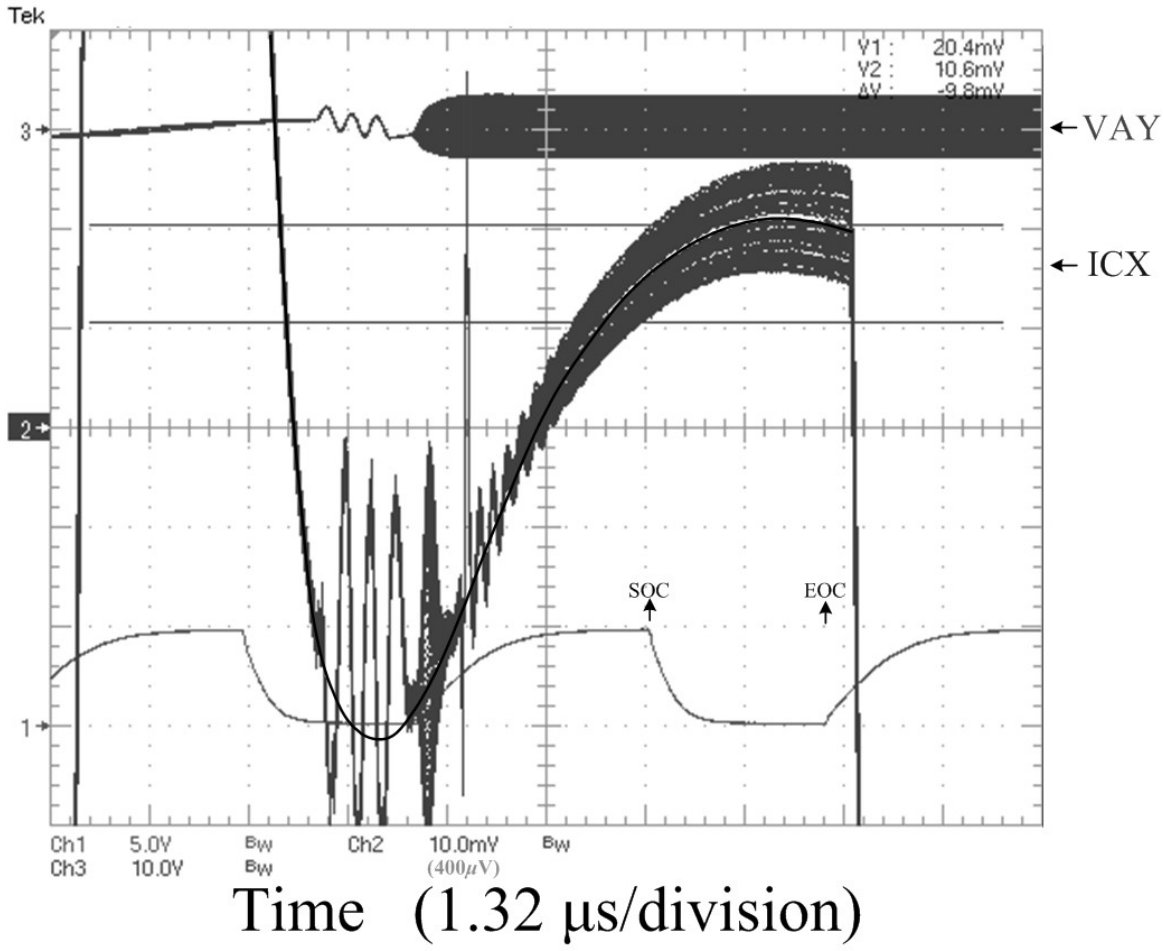

Figure 7-11: Crosstalk from VAY to ICX.

VAY is varying from positive full scale to negative full scale as shown at the top of Figure 7-11. VAY's compensation operational amplifier is enabled approximately 5.5µs prior to the SOC (start of conversion) of the A-D converter. The ICX channel is being sampled between the SOC and EOC (end of conversion) of the A-D converter. During

this time, the VAY channel is in the process of settling and is within 90% of its final value. The crosstalk is due to the magnetic field of VAY's drive winding coupling to the sense or signal windings of the ICX channel. The crosstalk is about ±200 μV (±2 counts of the A-D converter). For low current levels, the ±2 counts may slightly impact the metering accuracy. For the oscilloscope capture of Figure 7-11, the ICX channel is at positive full scale. Similar crosstalk occurs for different levels of ICX through negative full scale.

The ICX channel may also crosstalk to the VAY channel. The ICX channel's compensation operational amplifier is disabled around 2.5 μs prior to the VAY channel SOC. Once the ICX channel's compensation operational amplifier is disabled, any energy that is stored in the core causes the windings to fly back, dumping the energy into the isolated power supply rails. Therefore, while the A-D converter is sampling VAY, the ICX channel is in the transformer core reset mode of Figure 2-2.

The crosstalk from channel ICX to VAY was measured with an oscilloscope by zooming in on the VAY channel signal during the time the A-D converter is sampling, while varying the voltage applied to the ICX channel. The oscilloscope was set to infinite persistence to capture the crosstalk due to the varying ICX signal. The oscilloscope capture of the crosstalk from ICX to VAY is shown in Figure 7-12.

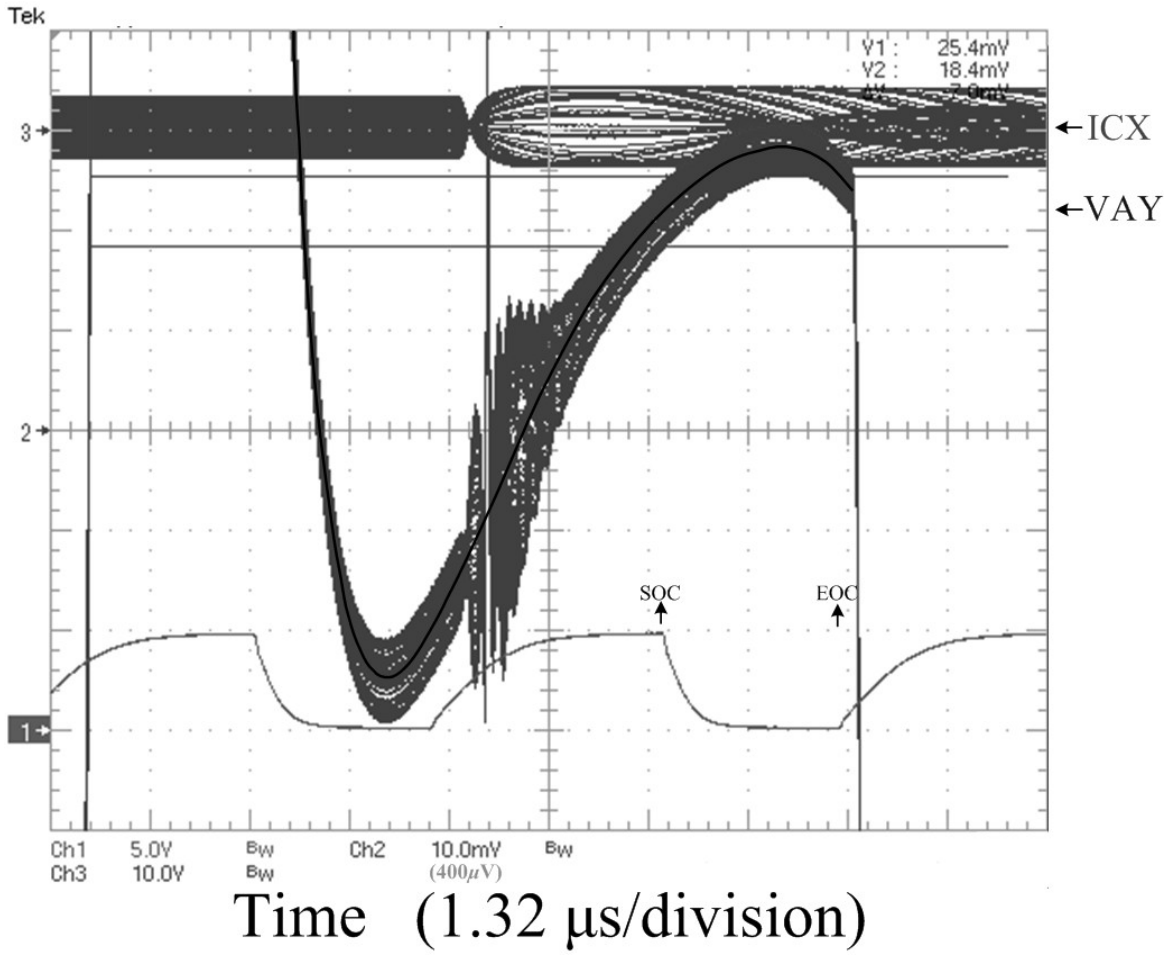

Figure 7-12: Crosstalk from ICX to VAY.

ICX is varying from positive full scale to negative full scale as shown at the top of Figure 7-12. Around 2.5 μs prior to VAY's SOC, ICX's compensation operational amplifier is disabled and the ICX signal, shown at the top of Figure 7-12 flies back to the opposite level. The crosstalk is due to the magnetic field of ICX's power supply windings coupling to the sense or signal windings of the ICX channel. The crosstalk is about ±200 μV (±2 counts of the A-D converter). For low voltage levels, the ±2 counts may slightly impact the metering accuracy. For the oscilloscope capture of Figure 7-12, the VAY channel is at positive full scale. Similar crosstalk occurs for different levels of VAY through negative full scale.

The crosstalk performance was achieved by having the primary and secondary printed circuit board Faraday shields (i.e. top and bottom side planes) complete a shorted ring about the outside of the E-E core as shown in Figure 3-2. Without these shorted rings, the crosstalk was nearly double. The crosstalk level of the prototype Isolated Analog Selector circuits may become an issue for lower level current and voltage metering. The crosstalk could be further reduced by placing the isolation transformer further apart, adding magnetic shielding, or by not having activity on adjacent channels during the A-D conversion process of a particular channel.

Chapter 8 Conclusions

A new isolated analog acquisition system is based on the Isolated Analog Selector circuit, which pulses the isolated analog signal through the isolation transformer only when the A-D converter needs to sample the corresponding channel. The size, weight, and cost of the isolation transformer is greatly reduced. For a digital protective relay, a weight reduction from 2/3 pound to around 0.2 ounces is a significant accomplishment.

The isolation transformer reduction is analogous to the switched mode power supply industry achievements. A single, bulky 50/60 Hz transformer is replaced with a smaller, high frequency, multi-winding transformer plus many additional electronic components for controlling the switching action and providing stability and accuracy to the control circuitry.

Greater attention must be given to the design and analysis details of the Isolated Analog Selector circuitry to achieve high accuracy of the sampled data. The decreased core size and increased complexity of the electronic circuitry results is some unique design challenges. High accuracy is achieved using a compensation operational amplifier with feedback from a sense winding. The isolation transformer is easily constructed with an E-E ferrite core and printed circuit board traces for windings.

SPICE is used to analyze the stability, settling and accuracy of the compensation operational amplifier control circuitry. SPICE models of the isolation transformer capture the part-to-part and temperature variations of the E-E core and printed circuit board windings. SPICE is used extensively to identify issues and improve the design of the Isolated Analog Selector control circuitry.

FEA is used to identify and improve the magnetic coupling accuracy of the isolation transformer. Strategically locating the drive and sense windings minimizes the magnetic coupling error between the drive-to-sense and drive-to-signal windings.

Testing of a digital protective relay with a prototype Isolated Analog Selector circuit (with one VT and one CT channel) validates the new isolated analog acquisition approach and design. The accuracy achieved is better than ±0.1% ±8 mV (or ±4 mA). The prototype Isolated Analog Selector circuit performs well over a temperature range from –45 to 90 °C, has good common mode rejection performance, passes electrical transient type tests, and has a slight crosstalk between adjacent Isolated Analog Selector channels.

Appendix A: SPICE Models

A.1 E-E Core Models

```
**********
* Tomita EE core:  2G1-EE-22x13.8B (2/15/08, TMM)
* 2G1 material @ 25 Degrees C
.model 2G1_material_typ  Core(MS=327K A=6 C=0.147 K=10.5
+                                Area=0.249 Path=3.81 GAP=0)
.model 2G1_material_min Core(MS=327K A=10.4 C=0.2 K=10.5
+                                Area=0.249 Path=3.81 GAP=0)
.model 2G1_material_max Core(MS=327K A=3.6 C=0.107 K=10.5
+                                Area=0.249 Path=3.81 GAP=0)
* 2G1 material @ 100 Degrees C
.model 2G1_material_100 Core(MS=183K A=1.3 C=0.081 K=4.2
+                                Area=0.249 Path=3.81 GAP=0)
.model 2G1_material_100_mn      Core(MS=183K A=2.55 C=0.124 K=4.2
+                                Area=0.249 Path=3.81 GAP=0)
.model 2G1_material_100_mx      Core(MS=183K A=.65 C=0.049 K=4.2
+                                Area=0.249 Path=3.81 GAP=0)
* 2G1 material @ -40 Degrees C
.model 2G1_material_40          Core(MS=384K A=36 C=0.49 K=11
+                                Area=0.249 Path=3.81 GAP=0)
.model 2G1_material_40_mn       Core(MS=384K A=51.5 C=0.545 K=11
+                                Area=0.249 Path=3.81 GAP=0)
.model 2G1_material_40_mx       Core(MS=384K A=27.2 C=0.45 K=11
+                                Area=0.249 Path=3.81 GAP=0)
* EE22x13_8_2G1 @ 25 Degrees C
.model EE22x13_8_2G1_typ        Core(MS=327K A=6 C=0.147 K=10.5
+                                Area=0.249 Path=3.81 GAP=4.94e-4)
.model EE22x13_8_2G1_min        Core(MS=327K A=10.4 C=0.2 K=10.5
+                                Area=0.249 Path=3.81 GAP=6.63e-4)
.model EE22x13_8_2G1_max        Core(MS=327K A=3.6 C=0.107 K=10.5
+                                Area=0.249 Path=3.81 GAP=3.89e-4)
* EE22x13_8_2G1 @ 100 Degrees C
.model EE22x13_8_2G1_100        Core(MS=183K A=1.3 C=0.081 K=4.2
+                                Area=0.249 Path=3.81 GAP=4.94e-4)
.model EE22x13_8_2G1_100_mn     Core(MS=183K A=2.55 C=0.124 K=4.2
+                                Area=0.249 Path=3.81 GAP=6.63e-4)
.model EE22x13_8_2G1_100_mx     Core(MS=183K A=0.65 C=0.049 K=4.2
+                                Area=0.249 Path=3.81 GAP=3.89e-4)
* EE22x13_8_2G1 @ -40 Degrees C
.model EE22x13_8_2G1_40         Core(MS=384K A=36 C=0.49 K=11
+                                Area=0.249 Path=3.81 GAP=4.94e-4)
.model EE22x13_8_2G1_40_mn      Core(MS=384K A=51.5 C=0.545 K=11
+                                Area=0.249 Path=3.81 GAP=6.63e-4)
.model EE22x13_8_2G1_40_mx      Core(MS=384K A=27.2 C=0.45 K=11
+                                Area=0.249 Path=3.81 GAP=3.89e-4)
```

A.2 OPA357 SPICE Model (Courtesy Texas Instruments)

```
* OPA357 SPICE Macro-model
*
*   Rev. A    12 January 2004, by W.K. Sands
*
*   Rev. B    4 January 2004 By Neil Albaugh: ADDED HEADER TEXT & EDITED TEXT
*
*          This macromodel has been optimized to model the AC, DC, and transient response
*      performance within the device data sheet specified limits.  Correct operation of this
*      macromodel has been verified on MicroSim P-Spice ver. 8.0 and on PENZAR
*      Development TopSPICE ver. 6.82d. For help with other analog simulation software,
*      please consult your software supplier.
*
*
*   Copyright 2004 by Texas Instruments Corporation
*
* BEGIN MODEL OPA357
*
* BEGIN NOTES
*
*
* MODEL TEMPERATURE RANGE IS -40 C TO +125 C, NOT ALL PARAMETERS
* ACCURATELY TRACK THOSE OF AN ACTUAL OPA357 OVER THE FULL
* TEMPERATURE RANGE BUT ARE AS CLOSE AS PRACTICAL
*
* END NOTES
*
*
* BEGIN MODEL OPA357
*
.SUBCKT OPA357 1 2 3 4 5 6
* PINOUT ORDER OUT -V +IN -IN EN +V
* PINOUT ORDER  1   2   3  4   5  6
*
*
* BEGIN SIMULATION NOTES
*
* FOR BEST RESULTS WHEN LOOKING AT INPUT BIAS CURRENTS
* SET ABSTOL FROM 1E-13 TO 3E-13
* FOR AID IN DC CONVERGENCE SET ITL1 FROM 400 TO 4000
* FOR AID IN TRANSIENT ANALYSIS SET ITL4 FROM 50 TO 500
*
* END SIMULATION NOTES
*
*
* BEGIN MODEL FEATURES
*
* OPEN LOOP GAIN AND PHASE
* INPUT OFFSET VOLTAGE CHANGE AT THE
* RAIL-TO-RAIL INPUT TRANSITION POINT
* INPUT VOLTAGE NOISE WITH 1/F
* INPUT CURRENT NOISE
* INPUT BIAS CURRENT
* INPUT CAPACITANCE
```

```
* INPUT COMMON MODE VOLTAGE RANGE
* INPUT CLAMPS TO RAILS
* CMRR WITH FREQUENCY EFFECTS
* PSRR WITH FREQUENCY EFFECTS
* SLEW RATE
* QUIESCENT CURRENT
* RAIL TO RAIL OUTPUT STAGE
* HIGH CLOAD EFFECTS
* CLASS AB BIAS IN OUTPUT STAGE
* OUTPUT CURRENT THROUGH SUPPLIES
* OUTPUT CURRENT LIMITING
* OUTPUT CLAMPS TO RAILS
* OUTPUT SWING VS OUTPUT CURRENT
* SHUTDOWN
* QUIESCENT CURRENT IN SHUTDOWN
*
* END MODEL FEATURES
*
*
Q20 7 8 9 QLN
R3 10 11 20
R4 12 11 20
R10 8 13 1E3
R11 14 15 1E3
R12 15 6 2.5
R13 2 13 2.5
R16 16 17 1E3
R17 18 19 2.5
R18 9 20 2.5
D5 21 6 DD
D6 2 21 DD
D7 22 0 DIN
D8 23 0 DIN
I8 0 22 0.1E-3
I9 0 23 0.1E-3
E2 9 0 2 0 1
E3 19 0 6 0 1
D9 24 0 DVN
D10 25 0 DVN
I10 0 24 0.1E-3
I11 0 25 0.1E-3
E4 26 4 24 25 0.18
G2 27 4 22 23 5E-7
R22 2 6 100E6
E5 28 0 19 0 1
E6 29 0 9 0 1
E7 30 0 31 0 1
R30 28 32 1E4
R31 29 33 1E5
R32 30 34 1E5
R33 0 32 1
R34 0 33 10
R35 0 34 10
E10 35 3 34 0 0.4
R36 36 31 1K
R37 31 37 1K
```

```
C6 28 32 0.2E-12
C7 29 33 100E-12
C8 30 34 2E-12
E11 38 35 33 0 0.5
E12 27 38 32 0 3.3
E14 39 9 19 9 0.5
D11 16 19 DD
D12 9 16 DD
M1 40 41 13 13 NOUT L=3U W=800U
M2 42 43 15 15 POUT L=3U W=800U
M3 44 44 18 18 POUT L=3U W=800U
M4 45 46 10 10 PIN L=3U W=160U
M5 47 26 12 12 PIN L=3U W=160U
M8 48 48 20 20 NOUT L=3U W=800U
R43 49 43 100
R44 50 41 100
G3 16 39 51 39 0.2E-3
R45 39 16 200E6
C12 17 21 1E-12
R46 9 45 2E3
R47 9 47 2E3
C13 45 47 0.125E-12
C14 27 0 0.68E-12
C15 26 0 0.68E-12
C16 21 0 0.5E-12
D13 41 7 DD
D14 52 43 DD
Q15 52 14 19 QLP
V18 27 46 0.7E-3
M16 53 54 55 55 NIN L=3U W=160U
R53 56 55 20
M17 57 26 58 58 NIN L=3U W=160U
R54 56 58 20
R55 53 19 2E3
R56 57 19 2E3
C20 53 57 0.125E-12
V19 46 54 -2E-3
M18 59 60 61 61 PIN L=6U W=500U
M19 62 63 19 19 PIN L=6U W=500U
V20 19 60 1.3
M21 56 59 9 9 NIN L=6U W=500U
M22 59 59 9 9 NIN L=6U W=500U
G6 16 39 64 39 0.2E-3
E17 37 0 27 0 1
E18 36 0 4 0 1
M23 63 63 19 19 PIN L=6U W=500U
V21 62 11 0
R59 21 42 5
R60 40 21 5
J1 65 27 65 JNC
J2 65 26 65 JNC
J3 26 66 26 JNC
J4 27 66 27 JNC
C21 27 26 0.5E-12
E19 67 39 57 53 1
R61 67 64 1E4
```

```
C22 64 39 0.125E-12
E20 68 39 47 45 1
R62 68 51 1E4
C23 51 39 0.125E-12
G7 69 39 16 39 -1E-3
G8 39 70 16 39 1E-3
G9 39 71 48 9 1E-3
G10 72 39 19 44 1E-3
D17 72 69 DD
D18 70 71 DD
R66 69 72 100E6
R67 71 70 100E6
R68 72 19 1E3
R69 9 71 1E3
E23 19 49 19 72 1
E24 50 9 71 9 1
R70 70 39 1E6
R71 71 39 1E6
R72 39 72 1E6
R73 39 69 1E6
G11 6 2 73 0 3.55E-3
R75 38 27 1E9
R76 35 38 1E9
R77 3 35 1E9
R78 4 26 1E9
R79 39 51 1E9
R80 39 64 1E9
R81 49 19 1E9
R82 9 50 1E9
R83 31 0 1E9
R85 61 62 1E3
G14 63 9 74 0 400E-6
G15 44 48 74 0 1.35E-3
E48 75 16 74 0 30
E49 76 39 74 0 -30
V49 77 76 15
V50 78 75 -15
R127 75 0 1E12
R128 76 0 1E12
M41 39 78 16 79 PSW L=1.5U W=150U
M42 16 77 39 80 NSW L=1.5U
R129 79 0 1E12
R130 80 0 1E12
M43 81 5 9 9 NEN L=3U W=300U
M44 82 81 9 9 NEN L=3U W=3000U
R131 81 19 1E4
R132 82 83 1E6
V51 83 9 1
M45 84 84 19 19 PEN L=6U W=60U
M46 5 84 19 19 PEN L=6U W=60U
I20 84 9 0.2E-6
C26 5 0 1E-12
E50 74 0 85 9 1
V52 82 85 1.111E-6
R133 9 85 1E12
C32 19 81 15E-12
```

```
        C33 83 82 0.15E-12
        I21 6 2 3.4E-6
        L1 21 1 4E-9
        R150 21 1 400
        V78 19 65 0
        V79 66 9 0
        I22 26 0 1E-12
        I23 27 0 1E-12
        M47 86 81 9 9 NEN L=3U W=3000U
        R152 86 83 1E6
        C34 83 86 0.005E-12
        V80 86 87 1.111E-6
        R153 9 87 1E12
        E53 73 0 87 9 1
        R154 0 73 1E12
        R155 44 19 1E9
        R156 9 48 1E9
        R157 13 41 1E9
        R158 15 43 1E9
        RG1 74 0 1E9
        .MODEL DVN D KF=8E-12 IS=1E-16
        .MODEL DD D
        .MODEL DIN D
        .MODEL QLN NPN
        .MODEL QLP PNP
        .MODEL JNC NJF
        .MODEL POUT PMOS KP=200U VTO=-0.7
        .MODEL NOUT NMOS KP=200U VTO=0.7
        .MODEL PIN PMOS KP=200U VTO=-0.7
        .MODEL NIN NMOS KP=200U VTO=0.7
        .MODEL NEN NMOS KP=200U VTO=0.5 IS=1E-18
        .MODEL PEN PMOS KP=200U VTO=-0.7 IS=1E-18
        .MODEL PSW PMOS KP=200U VTO=-7.5 IS=1E-18
        .MODEL NSW NMOS KP=200U VTO=7.5 IS=1E-18
        .ENDS
* END MODEL OPA357
```

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