A 5 GHz DIGITALLY CONTROLLED SYNTHESIZER IN 90NM CMOS

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ABSTRACT

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This thesis presents the implementation of a self-calibrating low-power Digitally Controlled Synthesizer (DCS) operating at 5 GHz in the IBM 90nm process. The DCS has high tolerance to device and process variations because of its mostly digital design. It provides an extremely wide tuning range with fine resolution. The DCS also has low power consumption and a small layout area.

A novel time-to-delay accumulator is used that prevents the need to propagate the carries of a digital adder using two separate delay lines. A 5GHz three bit Johnson counter is described and its use as a frequency divider. A second 10-bit, 5 GHz synchronous counter using complementary logic is also described. The 24-bit time-to-delay accumulator provides 300 Hz frequency resolution and incorporates single-event upset (SEU) mitigation circuitry. The use of Reverse Body Biasing is also discussed to reduce the effects of Total Ionizing Dose (TID) radiation.

The implementation of capacitive loaded 0-300ps delay lines is covered in detail as well as a novel calibration scheme for the delay lines. The DCS has a built-in calibrator to correct for process and environmental variations in the delay. The DCS is also designed so that the added delay can be calibrated to within 2ps of resolution without interfering with normal operation of the DCS.

The paper includes a brief description of the conditions for oscillation, Phase Locked Loops (PLL), ring oscillator VCO, LC VCO, and Discrete Digital Frequency Synthesizer (DDFS). The simulation results for the operation of the DCS, which was simulated using Synopsis HSPICE, and Mentor ADMS. Future test procedures of the actual chip using scan chain flip flops are covered as well. The paper concludes with a discussion of future work and project contributions.

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Dedication

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1. Introduction

All modern communication systems require a stable periodic signal to provide the timing base for functions such as sampling, synchronization, and frequency synthesis. In many applications, the clock signal is created using either an off-chip crystal oscillator or an integrated oscillator. In other applications the clock signal can be extracted from the input signal. However even if the signal has the clock data encoded within, it is often necessary to generate a local clock signal at a different phase or frequency. It may also be necessary to retiming the data for data recovery applications and clock synchronization/ deskewing in clock distribution applications.

Current technology trends indicate a preference for the use of Complimentary Metal –Oxide Semiconductor (CMOS) to develop fully monolithic designs. CMOS designs can take advantage of the scaling factor that allows for a reduction in the power consumption, consistent cost scaling, and reduction in silicon die area when compared to compound semiconductor technology. Shrinking gate sizes allow for higher operation frequencies without modification of the design. Full integration would also reduce the number of outside components to just an antenna to receive or transmit an RF signal, a power supply, and a crystal reference to provide a clean reference signal.

In applications like clock generation, clock recovery networks, and frequency synthesizers, the generated clock is the output. As the data transfer speed increases, the clock period becomes shorter, decreasing the absolute timing uncertainty, or jitter, that can be tolerated at the output for such applications. Clock edges are used to determine the moment of sampling in applications such as Analog to Digital Converters (ADCs), data recovery networks, or mixers. Random and

systematic variations in the sampling time degrade the performance of the system by limiting the maximum resolution.

Phase Locked Loops (PLLs) are used to create the required local clock signal to reference to the input clock or when precise control of the output frequency is necessary. PLLs are one of the few practical ways to generate a low phase noise reference frequency with no frequency drift at above a few GHz. PLL applications include clock/ data recovery networks used in fiber optic data transceivers, disk drive channels, local area network transceivers and DSL transceivers. They have also found extensive use as clock generators for microprocessors, DSP systems and DRAM because of their stable clock generation when referenced to a crystal oscillator.

The most common types of oscillators currently found in PLLs are LC VCOs, Ring VCOs, and Discrete Digital Frequency Synthesizers (DDFSs). All Digital Phase Locked Loops (ADPLLs) are now becoming very popular. The LC VCO is commonly used in RF frequency synthesis and frequency modulation. They enjoy very low phase noise because of the very large quality factor (Q) achievable with the resonant network and excellent frequency performance [1, 2]. Unfortunately, LC oscillators have a very narrow bandwidth when compared to other types of oscillators which limits their usefulness for many communication schemes.

LC oscillators are often implemented using external parts increasing the cost of the system. It is very difficult to develop high Q components because of the low substrate resistivity in the silicon process. Thus adding high quality integrated inductors to the CMOS process flow increases the cost and complexity of the chip. It also can introduce problems such as the control of eddy currents in the substrate.

Ring oscillators are also found in many PLL implementations. Ring oscillators are commonly used in application such as frequency synthesizers and oversampling circuits. They are used extensively because their ease of implementation and simplicity of design.

They can be added to any digital CMOS fabrication process and require less die area when compared to the LC oscillator because of the lack of area consuming inductors and varactors. Ring oscillators have a wide tuning range when compared to LC oscillators. They also offer the availability of multiple phases at output.

On the negative side, the noise performance of ring oscillators is generally worse than LC designs because of the low Q of the ring structure [3]. For a similar reason, ring oscillators also have difficulty obtaining sufficient noise and frequency performance for high frequency RF applications [4].

Discrete Digital Frequency Synthesizers (DDFSs) use a combination of digital data and mixed/ analog signal processing blocks to generate periodic signal waveforms. These oscillators are known for fast frequency switching and high resolution. DDFS also have very wide bandwidth. The DDFS provides linear phase and frequency shifting with good spectral purity. They are commonly found in applications that requires a precise, high frequency or a tunable phase output. They are found in applications such as cable modems, measurement equipment, arbitrary waveform generators, cellular base stations, and wireless local loop base stations. DDFSs are starting to become popular in for digital waveform and clock generation, and modulation.

While the DDFS uses digital components for a large part of the system, it still requires a Digital-to-Analog Converter (DAC) to create the actual output waveform and an analog filter to smooth the output signal. These analog devices are not scalable in the CMOS process and must

be redesigned to take advantage of the smaller gate sizes. The DDFS suffers from quantization errors associated with the lookup table and the DAC. Many DDFS also requires a large ROM to increase the accuracy of the generated output.

1.1 Project Description

The proposed digital-controlled clock synthesizer (DCS) has many of the desired qualities of the other types of oscillators without many of the problems. The DCS has a large bandwidth with low phase noise. The DCS uses a fixed frequency clock reference as an input. Because there is no jitter accumulation in the DCS, the jitter can be nearly the same as the clock reference. Since the clock reference is at a fixed frequency and does not need to be tunable, lower jitter is easier to implement on-chip. A fixed external reference with very low jitter can also be used and the synthesizer can generate all other frequencies needed by the IC and maintain the very low-jitter.

Like the DDFS, the DCS uses digital logic to set the period of the output to be an integer number of reference clocks plus an interpolated value between clock transitions by delaying the output using a digital-to-delay converter (DDC) [5]. This is similar to the operation of a direct digital frequency synthesizer without the digital-to-analog converter. The only analog component required is the digital-to-delay converter which will have trimmable delay elements that can be calibrated for reduced sensitivity to process and device variations. Other advantages of this approach are the immediate frequency hopping ability and no jitter accumulation. .

The result of this research is a DCS circuit that is reconfigurable for operation at any frequency between 5 MHz and 5 GHz with very low jitter, is robust to radiation effects,

temperature, and process variations, scales with process for low area, and has low power dissipation.

1.2 Organization of Thesis

The thesis is organized to provide the reader with a clear understanding of the development process. Chapter 2 provides insight into the operation of PLL. It provides a brief overview of the operation of oscillators with a description of the main types of oscillators. It discusses the current state of each type oscillator. Chapter 3 discusses the operating principle behind the DCS, the overall design architecture, and specifications. Chapter 4 provides insight into the component design. Chapter 5 discusses the simulation results and the layout of the circuit. Chapter 6 includes a brief summary of the work, along with a discussion of the major contributions of this work and recommendation for future work and enhancements.

2. Background

In this chapter a discussion of the operation and uses of Phase Locked Loops (PLLs) is presented. Next a basic discussion of the criteria for oscillation is covered. The next section will cover the most common types of oscillators found in PLLs with a discussion of different types of topologies. Chapter 2 provides the background necessary to understand the presented design and how it compares to current technology.

2.1 PLL

Phase Locked Loops (PLLs) have been in use since the 1930s when it was used as an alternative architecture for receiving and demodulating AM signals [6]. PLLs have found uses in carrier recovery, clock recovery, phase modulation, phase/frequency demodulation, clock synchronization, frequency synthesis, duty cycle correction, and jitter reduction.

A PLL can be used to embed a less accurate RF oscillator in a feedback loop whose frequency can be controlled with a control signal. The resulting oscillator output frequency is then locked to an accurate low frequency reference. This synchronizes the oscillator's output to a reference or input signal in both frequency and phase.

A PLL consists of three basic components as seen in Figure 1: a Phase Frequency Detector (PFD); a low pass filter; and an oscillator. The PFD acts as a comparator. It compares the reference phase and/or frequency with the oscillator signal. The low pass filter integrates the current pulse generated by the PFD. The oscillator frequency is controlled by the output of the low pass filter.

A PLL operates on phase deviation rather than signal amplitude. As the output signal deviates from the input signal, the PLL response will depend on two nonlinear devices, the oscillator and phase detector. The phase error between oscillator output and reference signal is constant, not necessarily equal to zero, when the PLL is locked. If the phase error increases, the feedback control mechanism acts on the oscillator to reduce the phase error.

Figure 1 Block diagram of Phase Locked Loop (PLL)

2.1.1 Components

Phase/Frequency Detector

The Phase/Frequency Detector (PFD) compares the reference phase and/or frequency of the input signal with the phase of the generated signal. The PFD generates an error signal proportional to the phase difference of the two signals.

Low pass filter

The low pass filter takes the control value, either current or voltage, from the PFD and filters out the high frequency components to be applied to the oscillator.

Oscillator

The oscillator generates a sinusoidal signal with a frequency based on its input signal, the filtered phase difference from the PFD. The type of oscillator will vary with the type of PLL. In a linear PLL the control signal for the oscillator is usually a voltage and the oscillator is called a voltage controlled oscillator. In an All Digital PLL (ADPLL) the control signal is a digital word.

The oscillator is extremely important to the operation of a PLL. The primary source of timing jitter in a PLL when compared to the other loop components is the oscillator [3, 4, 7, 8]. Oscillators will be the focus of the remainder of this section.

2.2 Oscillator

Two conditions are necessary for steady oscillation. The first is that the magnitude of the loop gain should be equal to unity. The second condition is that the phase of the loop gain is an integer multiple of 2π for the feedback loop to provide stable oscillation. These conditions are known as the Barkhausen criterion.

The criterion only guarantees that the oscillation will be sustained after it starts. It does not guarantee that oscillation will start. In real systems the magnitude of the loop gain should be slightly larger than unity for oscillation to start.

Any possible oscillation will grow indefinitely because of the positive feedback loop unless a nonlinear mechanism is used to stop the growth. In older systems, a nonlinear amplitude control circuit was used. Integrated circuit oscillators use hard-limiting of the power supplies and the

gain drop of the FETs at large signal levels to control growth. Any internal noise in the system at the specific oscillation frequency will be amplified with the positive feedback gain creating a periodic signal at the output. The gain of the feedback will then drop to unity as the signals get larger because of the amplitude limiting mechanism. This yields a steady-state oscillatory signal.

While the amount of gain will determine if the oscillator will start or not, the phase characteristics of the feedback loop determine the oscillation frequency. The frequency stability of an oscillator depends on how the phase characteristic, $\phi(\omega)$, of the loop varies with changing frequencies. Large values of $\frac{d\phi(\omega)}{d\omega}$ indicates that the oscillator will have a stable output frequency because any change in the loop phase, which can occur due to a slight variance in the one of the circuit parameters or temperature, will correspond to a small disturbance at frequency and vice-versa [3].

The application of an oscillator will dictate which characteristics are the most important. Oscillators designed for RF communications are the most difficult. One of the reasons is that air is an extremely lossy transmission media. The receiver circuitry is required to have exceptionally low noise levels to reduce the Bit Error Rate (BER) of the received signal. LC oscillators are often used in these systems because of their low noise characteristic. The design of clock and data recovery networks or frequency synthesizers employing PLLs is extremely difficult in RF applications.

Fiber-optic transmission systems have an almost ideal transmission media which eases the noise specifications [8]. Clock generators used to supply timing information to microprocessors, digital signal processing systems, and dynamic random-access memory arrays do not have strict noise specification and modern ring oscillators are usually sufficient for these applications. The

maximum frequency required from the oscillator depends on the data transmission and/or data processing rate specifications of the system. Many problems exist as the oscillator's frequency becomes higher. As data speeds have increased, the clock period has become shorter. This decreases the absolute timing uncertainty (jitter) that can be tolerated at the output. Skin effects become more noticeable at high frequencies as well as problems associated with bulk-node currents.

Figure 2 Comparison of a perfect signal to one with variable jitter

Faster systems dissipate more power. The dynamic power dissipation equation is

$$P = V_P^2 C_L f \quad (2.1)$$

where P is the power that is dissipated on a node with capacitance of C_L oscillating at a frequency of f with a peak voltage amplitude of V_P . As the frequency of oscillation increases so does the power consumption.

The noise characteristics of the system also depend on the maximum available power. Large signal levels correspond to better Signal-to-Noise Ratio (SNR) improving the phase noise

of the oscillator. Unfortunately large power consumption is not desirable for hand-held applications.

Multiple output phases of the clock generator are useful for ADCs or oversampling networks. Some of these networks use sampling circuitry with multiple clock inputs, with each individually triggering the sampling event at the signal transitions. This technique multiplies the sampling rate by the number of available phases. Multiple phases are naturally available from ring oscillators and some ring LC designs [9, 10].

The tuning range of an oscillator is very important in many applications. Narrow tuning range can create problems meeting the frequency specification of a system with a single fabrication run and multiple iterations may be necessary. Wide tuning range increases the gain of the oscillator resulting in a higher sensitivity to control line noise. Generally ring oscillators have a much wider tuning range than LC oscillators although there are different design techniques available to implement wide tuning range LC oscillators [11].

One of the most significant factors in oscillator designs is controlling or reducing the undesired and uncontrolled fluctuation of the phase of the oscillator signal, or phase noise. Phase noise and jitter are the same phenomenon. Phase noise is defined in the frequency domain and jitter is defined as the uncertainty in the time domain.

There are two main categories that contribute to phase noise. The first is random factors that create random variations of the timing of the signal edges. Most jitter originates from thermal noise and flicker noise of active and passive devices. The second main category is the systematic factors that can generally be avoided by careful design of the system. This category of phase noise can usually be attributed to interfering signals in other parts of the system. One common

way that these signals propagate through the system is between power supplies and ground lines although signals can leak through the substrate if circuits are located in close proximity. Inputs to control signals are also susceptible to noise. Other considerations include mismatches between devices and delays of different stages. All these things must be considered in order to minimize phase noise.

These principles apply to all oscillators. This paper will now discuss some of the specific characteristics of the most common types of oscillators.

2.2.1 Ring VCO

The Ring oscillator has a wide tuning range and the availability of multiple phases at the output. This makes them very useful for applications such as frequency synthesizers and oversampling circuits. They require less die area when compared to the LC oscillator because they do not use area-consuming passive parts, inductors and varactors. Unfortunately the noise performance is generally worse than LC designs because of the low quality factor (Q) of the ring structure [3, 4]. In addition, the low Q factor makes it difficult to generate the frequency performance necessary for RF applications.

Ring oscillators can be added to any digital CMOS fabrication process because of their use of standard digital cells. The design is straight forward using integrated circuit design techniques. The design process is also simplified by the large number of CAD based tool available to minimize area and timing issues of digital cells.

Figure 3 Amplifier stages of single ended ring oscillator

The simplest type of ring oscillator consists of an odd number, N , of inverter stages connected in a positive feedback loop, Figure 3. The odd number of inverter stages creates an inversion in the loop. If one node is excited, the pulse will propagate through all the stages and will reverse the polarity of the initial node. This type of oscillator meets the Barkhausen criterion for oscillation by closing the positive feedback loop around the amplifier stage without the need for a frequency-selective network found in LC oscillators.

The maximum oscillation frequency is limited by the minimum delay time through an inverter stage.

$$f_{max} = \frac{1}{2 * N * T_d} \quad (2.2)$$

where N is equal to the number of stages in the ring oscillator and T_d is equal to the propagation delay of a single stage. The minimum number of stages for a single ended ring oscillator is three. This limits the maximum achievable frequency for this type of oscillator. Differential designs can be made with two stages and will be discussed later.

2.2.1.1 Single-ended Ring Oscillator

A basic ring oscillator can be constructed using single ended inverters to act as the amplification stage. An odd number of inverter stages is necessary for steady oscillation. Otherwise the oscillator will latch up at a DC level which satisfies the Barkhausen criterion at zero frequency. One way to think of it is when an odd number of stages is implemented and one of the nodes experiences an excitation, the pulse will propagate through all the stages and will reverse the polarity of the initially excited node starting oscillation. When an even number of stages is implemented, the pulse will still propagate through all the stages but will not reverse the polarity of the initial node resulting in a steady state condition.

The frequency of oscillation can be controlled by changing the strength of an inverter in the loop, either by changing the loads seen by the inverter or altering V_{DD} . Load tuning is not widely used for single-ended ring oscillators because of the difficulty in implementing controllable resistors and capacitors in CMOS. Although power supply manipulation can be used in both single-ended and differential designs, use of a low power supply voltage results in smaller output signal swings reducing the phase noise performance and making the circuit more susceptible to supply and ground disturbances.

Single-ended structures are usually preferred over the differential architectures whenever power dissipation is the most important consideration since they include less active elements to dissipate power. However, single-ended structures are rarely used in high frequency design. Single-ended constructions are very susceptible to common mode problems such as power supply and substrate bounces. The signal output does not provide a 50% duty cycle under practical conditions, and it is more susceptible to process and temperature variations when compared to differential oscillators.

2.2.1.2 Differential Ring Oscillator

Differential architectures have inherit advantages over single-ended. Differential architecture provides the circuit a better immunity against common mode disturbances such as power supply and substrate bounces. It also improves the spectral purity and has a 50% duty cycle at the output.

Differential ring oscillators can be constructed with an even number of stages. The required extra phase shift can be obtained by reversing one of the connections in the architecture introducing a DC phase shift, Figure 4.

Figure 4 Differential four stage ring oscillator

The most widely used architecture for a differential stage is a differential pair with active loads and a tail current supply, Figure 5. The delay for each stage is given by

$$T_D = \frac{C_L V_{P-P}}{I_{Control}} \quad (2.3)$$

Where C_L is the total load capacitance at each node, V_{P-P} is the voltage swing the output, and $I_{Control}$ is the mirrored current, Figure 5. From this, the frequency of oscillation can be determined by

$$f_{osc} = \frac{1}{2 * N * T_D} \quad (2.4)$$

The oscillation frequency can be controlled linearly by varying the mirrored current. Unfortunately this structure does not offer any way to control the output DC voltage levels or the output signal amplitude. As control currents are varied, the DC level of the output will fluctuate. This can create problems if the output signal is used to drive circuitry that is sensitive to input DC levels. One improvement to limit the output DC levels or control the output amplitude is to use a symmetrical load, Figure 6 [12].

Simple Differential Pair

Differential Pair with Current Mirror

Figure 5 Schematic of simple differential pair and differential pair with current mirror

Figure 6 Differential pair with symmetric loads

2.2.1.3 State of the Art

The oscillation frequency is directly dependent upon the total delay around the loop. For a fixed number of stages, the maximum oscillation frequency is limited by the minimum delay of a single stage. While the delay can be reduced and the frequency increased by modifying the design of the stage, this is limited by the characteristics of the fabrication process.

Oscillation can also be increased by decreasing the number of stages. Most practical ring oscillators need at least three stages although [13-15] introduce ring oscillators using only two stages. The delay stages used in these oscillators cannot be approximated as having a dominant pole and the available number of phases is also limited. Other methods to increase the output frequency include feedforward architecture [4, 16-18] and output interpolation [19].

Two Stage Oscillators

To satisfy the Barkhausen oscillation criterion a minimum of three stages is necessary for a ring oscillator with single-pole delay stages. In some applications, such as image rejection and delay interpolation, the in-phase/ quadrature (I/Q) outputs are necessary. The minimum practical number of delay stages that can be used to obtain I/Q outputs is four. However, increasing the number of stages increases the power consumption and decreases the maximum frequency.

A two stage ring oscillator was designed employing a double differential gain stage to supply the required extra phase and gain [15]. The half circuits small signal characteristics are similar to a differential amplifier with a current mirror load. The current mirror load doubles the

gain of the differential amplifier by folding the small signal current on one side and combining it with the small signal current of the other side.

When this characteristic is compared to the standard differential pair stage, this design inhibits the additional pole-zero pair resulting from the extra nodes created at the drain/ gates of the unbalanced current mirror loads. This supplies the required extra phase shift to sustain oscillation.

Sub-feedback loops

A technique to increase the maximum frequency while retaining the number of phases at the output was developed by Sun [20]. The oscillator has N gain stages, with N intercoupled sub-feedback loops, Figure 7. These are created by nesting additional stages outside the main loop. The output frequency is controlled by altering the strength of the sub-feedback loops and the main loop by controlling the power distribution to the inverter stages. The stages for each feedback loop are minimized so oscillation can be tuned between the N-stage ring oscillator and the three stage ring oscillator. This technique makes an oscillator that has a wide tuning range, high oscillation frequency, and a large number of output phases available.

Figure 7 Sub-feedback loop architecture

Output interpolation

Output interpolation combines the outputs of several stages to create faster switching outputs. This is very useful if higher frequencies are required but the number of phases at the output is not critical. In the most common implementation, the output voltage of the delay cells is converted into current using a transconductance stage. At the output, two or more current signals are combined to give a higher frequency current signal. The output signal is then converted back to the voltage domain by passing it through a load [19]. A typical implementation is shown in Figure 8.

Figure 8 Output interpolation technique

2.2.2 LC VCO

LC oscillators have much better phase noise and frequency performance when compared to ring oscillators because of their use of passive resonant elements with high quality Q factors. LC oscillators can be connected using bonding wires, integrated inductors, or external inductors. External components raise the cost of the system and introduce problems such as increased parasitic levels and increased power dissipation. The problem with the use of bonding wires as a high Q inductor in LC oscillators is that it is very difficult to accurately control the inductance value. In CMOS processing, it is possible to fabricate integrated inductors with high quality factors, a Q around 85 [7]. These can be implemented monolithically at the expense of adding processing steps. The added process steps increase the cost and complexity of the system. Additional problems to adding inductors into the CMOS process include the control of eddy

currents in the substrate and magnetic coupling. Low substrate resistivity also reduces the quality factor of on-chip inductors.

Figure 9 LC resonator tank model

The LC oscillator stores energy in the form of a magnetic field and an electric field. The energy is stored in the magnetic field when the current flowing in the LC tank is at its maximum and there is no voltage across the tank. All the energy is then transferred and stored in the electric field when the voltage across the tank is at maximum level. Energy transfers between the magnetic field and the electric field, oscillate without energy loss with ideal components. Unfortunately, there is loss caused real components.

The resonator tank of a LC oscillator is constructed from inductors and varactors. The LC oscillator can be modeled as a parallel connected LC network along with the series parasitic resistance, R_s , of the inductor, Figure 9. Although the tank might have a very high Q factor, the tank alone is not sufficient for steady oscillations because of the energy loss due to parasitics. While a simple LC tank might oscillate, the resonator will only oscillate for approximately Q number of cycles after the excitation, until all the stored energy is dissipated through the parasitic resistance of the inductor. Every LC oscillator employs active circuitry to cancel the parasitic

resistance. The active circuitry generates an effective negative resistance by providing energy at each cycle to cancel the parasitic resistance, Figure 10.

Figure 10 LC Oscillator model

The frequency of the LC oscillators is strictly determined by the characteristics of the resonator.

$$\omega_r = \frac{1}{\sqrt{L_{EQ} C_{EQ}}} \quad (2.5)$$

where L_{EQ} and C_{EQ} is equal to the equivalent inductance and capacitance respectively of the tank. Ideally the resonator's characteristics will not be affected by the active circuitry so that the capacitive loading of the active element can be ignored. From EQ 2.5, the LC oscillator's center frequency seems to depend only on the inductance and the capacitance values, such that reducing them increases the frequency of oscillation. However, the maximum frequency for a

LC oscillator is limited by the reduction of the self-resonance frequency of the inductor and the parasitic capacitances of the system.

2.2.2.1 Single Transistor Topology

The simplest type of LC oscillator is the single transistor oscillator. The single transistor oscillator looks like an LC tank connected at the drain of the transistor with a feedback signal applied to the gate or the source of the transistor, Figure 11. These types of oscillators date back to early 1915.

At resonance the tank's impedance assumes a real value implying that the phase difference between the current and voltage is zero. The zero phase difference can be achieved if the feedback signal returns to the source of the transistor. This creates a resistive loading of $1/g_m$ which can be observed at the transistor's source. The resulting loading effect degrades the tank's loaded Q causing the loop gain to fall to less than unity and the system to stop oscillating.

The source impedance can be transformed to a higher value to overcome this loading effect and sustain oscillation [21]. The required impedance transformation can be accomplished by either a capacitive or inductive divider. An oscillator using a capacitive divider is known as a Colpitts oscillator while an oscillator using an inductive divider is known as a Hartley oscillator, Figure 12. The equivalent resistance is equal to $(1+C_1/C_2)^2/g_m$ and $(1+L_2/L_1)^2/g_m$ respectively.

The resonance frequency is equal to EQ 2.5. The equivalent parallel resistance is

$$R_p = \frac{(L_{EQ}\omega_r)^2}{R_s} \quad (2.6)$$

as seen through the inductor. R_p scales proportionally to the equivalent inductance, L_{eq} and at resonance the voltage swing for a given bias current increases by the same factor as impedance R_p .

By maximizing the inductance value of the LC tank, the self resonating frequency of the inductor will be reduced toward the frequency of interest and the tuning range of the oscillator will be reduced because of the dominance of the tank capacitance by the device parasitic capacitance. Transistor M_1 is the primary source of noise for this oscillator and must be carefully sized and biased. Thermal noise associated with the gate and the drain of the transistor can be minimized by increasing the gate length and decreasing the bias current of the transistor, although increasing the device size increases the parasitic capacitance of the transistor and decreasing the bias current lowers the output voltage swing.

There are many problem associated with the single ended topology. Primarily the ratio of the required inductor and capacitor should be large to offset their effect on loaded Q of the tank. Secondly the single ended oscillator only provides single ended output, while most modern transceivers use differential signals for such devices as double balanced mixers. Finally there is no common mode rejection of noise from the supply and the substrate. These deficiencies led to the development of the differential topologies.

Figure 11 Direct feedback from drain to source compared to feedback in the presence of an impedance transform

Figure 12 (a) Colpitts oscillator (b) Hartley oscillator

2.2.2.2 Cross-Coupled Differential Topology

Differential topologies overcome many of the single ended topology limitations. An active buffer can be used instead of the divider network to facilitate the impedance transformation necessary for oscillation. A source follower can be used as a buffer to present high impedance to the tank.

The gate of transistor M_1 is tied to V_{DD} to maintain the same DC voltage as the gate of transistor M_2 , Figure 13. This assumes that M_1 and M_2 are the same size. If a second inductor is added to the circuit, it adds the ability to the oscillator to be operated differentially. This configuration is commonly known as a cross-coupled differential oscillator or negative g_m oscillator.

Figure 13 Cross-coupled differential oscillator

When viewed as a single-port representation, the negative resistance seen at the drain of M_1 and M_2 can be computed as

$$R_{in} = \frac{-2}{g_m} \quad (2.7)$$

[21] The magnitude of R_{in} should be less than or equal to R_p in order to obtain sustained oscillation

NMOS or PMOS Cross-Coupled Oscillator

There are four different configurations possible for a strictly NMOS or PMOS oscillator depending on the MOS type and the bias current location, Figure 14. The operation is similar for all four configurations so only the first one will be covered in detail.

Figure 14 (a) NMOS-only oscillator, (b) PMOS-only oscillator, (c) NMOS-only oscillator with a tail current source, (d) PMOS-only oscillator with a tail current [21]

The DC bias point for the first configuration is established by setting V_{GS} and V_{DS} equal to V_{DD} . This causes the NMOS transistors to be driven into saturation. The saturation equation for the source current is given by

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right) (V_{GS} - V_{th})^2 \quad (2.8)$$

where μ_n is the surface mobility of the electrons in the NMOS transistor, C_{ox} is the gate oxide capacitance per unit area and V_{th} is the threshold voltage. The transconductance can be calculated from the low frequency model of a MOSFET given by

$$G_M = \frac{\partial I_{DS}}{\partial V_{GS}} \Big|_{Q_{point}} = \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{th}) \quad (2.9)$$

The magnitude of the negative resistance seen looking into the NMOS transistor is equal to $2/g_m$. The ratio of the magnitude of the negative resistance to the equivalent parallel resistance is known as the startup safety factor. It is a general practice to design the oscillators with a safety factor of at least 2.

PMOS cross-coupled pairs are sometimes employed for their low noise characteristics [21]. The flicker noise of a PMOS transistor is about 10 times smaller than that of a NMOS transistor of similar dimensions. The PMOS only circuit operation is very similar to that of the NMOS. However the mobility of holes μ_p is lower than electrons, so that the PMOS devices have to be twice the size of the NMOS devices to achieve similar transconductance performance.

From EQ 2.9, it is evident that the transconductance is directly proportional to the ratio of the size of the device, limiting the ways that the transconductance can be controlled. A current mirror is generally used to limit the supply current of the FETs to provide control over the negative resistance and the oscillation amplitude. The bias current that flows through the current mirrors sets the total power dissipation of the oscillator. Although in some cases

removing the bias current source has been shown to achieve better phase noise performance [22]. However the bias current source aids the designer by allowing a compromise between phase noise performance and power dissipation.

CMOS Cross-Coupled Differential Oscillator

The CMOS Cross-Coupled Differential Oscillator uses both NMOS and PMOS cross-coupled pairs. The same bias current flows through both the NMOS and PMOS devices in a simple CMOS $-G_M$ oscillator. This yields the same power consumption for twice the negative resistance.

The total negative resistance can be expressed as a combination of the NMOS and PMOS pair's negative resistance.

$$R_{Neg} = R_{in_n} \parallel R_{in_p} = \frac{-2}{G_{mn} + G_{mp}} \quad (2.10)$$

There are some advantages to the strictly NMOS or PMOS oscillators when compared to the complementary oscillator. In a complementary oscillator, the voltage swing is limited by the supply voltage and the bias current so that the PMOS transistor is driven into cutoff and the bias current is restricted to the NMOS transistor. However, in the NMOS or PMOS only circuits, the voltage swing is limited only by the bias current so that the NMOS or PMOS only oscillator can exhibit AC voltage swings that exceed V_{DD} . One further thing to note is that complementary oscillators have more active components which increase the number of noise sources and parasitics hurting the phase noise and frequency performance of the oscillator.

Figure 15 CMOS cross-coupled differential oscillator without and with tail current [28]

2.2.3 DDFS

The Discrete Digital Frequency Synthesizer (DDFS) is a device that produces analog waveforms, usually sine waves, by generating a time-varying signal in digital form and then performing a Digital-to-Analog Conversion (DAC). Also known as Direct Digital Synthesis or Numerically Controlled Oscillator, the operations of the DDFS is primarily digital. They can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies.

The DDFS provides good linear phase and frequency shifting with good spectral purity. They excel in applications that require a precise, high frequency and/or a phase tunable output. The DDFS is becoming popular in the roles of clock generation and modulation because the output frequency, phase and amplitude can be precisely and rapidly manipulated under a digital processor control [23].

Figure 16 shows the complete frequency generation process of a DDS. The Phase Accumulator (PA) receives the Frequency Control Word (FCW) and is incremented by it each clock period. The output of the PA is sent to a ROM Look Up Table (LUT) where the amplitude of the sine wave is determined from the phase. The amplitude signal is then sent to a Digital to Analog Converter (DAC) where the sine wave is formed. Finally the signal is processed through a filter to smooth the output.

Figure 16 DDS function blocks and signal flow diagrams [23]

A sine wave can be express as $a(t) = \sin(\omega t)$. This is not a linear function. However, the angular information is linear. The phase angle rotates through a fixed angle for each unit time. Angular rate depends on the frequency of the signal $\omega = 2\pi f$ with the phase increasing linearly from 0 to 2π .

Knowing that the phase of a sine wave is linear and depends on a reference clock period, the phase rotation, Δp , for that period can be determined by

$$\Delta p = \omega \Delta t \quad (2.11)$$

where Δp is the change in phase of the sine wave, ω is the angular frequency of the wave, and Δt is a small change in time.

The PA, clocked with f_{clk} , generates a phase value sequence where Δt is the minimum amount of change.

$$f_{clk} = \frac{1}{\Delta t} \quad (2.12)$$

The output frequency is then equal to

$$f_{out} = \frac{f_{clk} \Delta p}{2\pi} \quad (2.13)$$

For an n bit accumulator f_{out} becomes

$$f_{out} = \frac{f_{clk} \Delta p}{2^n} \quad (2.14)$$

A stable reference clock is necessary to define the times at which digital sinusoidal sample values are produced. The samples are converted from digital to analog format and smoothed by a reconstruction filter to produce the analog frequency signal. The frequency depends on the reference-clock frequency, the binary number programmed into the phase register's length, and the length of n -bit accumulator.

The frequency resolution of the DDS is equal to

$$f_{out} = \frac{f_{clk}}{2^n} \quad (2.15)$$

In practical DDFS systems, all the bits out of the phase accumulator are not passed to the LUT, but are truncated to about 13 to 15 most significant bits. However, this does not affect the frequency resolution. The phase truncation adds a small amount of phase noise to the final output.

Phase accumulator

The Frequency Control Word (FCW) is the input to the Phase Accumulator (PA) and determines the periodicity of the phase accumulation. The PA is updated by the FCW every clock period. The output of the PA is fed to the LUT. Any change to the FCW results in immediate changes to the output frequency while being continuous in phase.

The size of the LUT depends on the length of the N-bit PA. Large N will equate to a larger LUT, Figure 17, so techniques such as phase truncation are used. Part of the phase generated by the PA is truncated which gives rise to spurs in the output spectrum. A dither can be added to the system that will reduce the spurs in the output spectrum, see below. Clock jitter also introduces noise in the output spectrum

Figure 17 Digital phase wheel [24]

If the PA increment is large, the PA will step quickly through the sine look-up table and thus generate a high frequency sine wave. If the phase increment is small, the PA will require more steps and generate a slower waveform. The PA is updated each clock cycle. A 32 bit wide PA incremented by 1 each clock cycle will require 2^{32} clock cycles before the PA resets to zero and the cycle repeats.

As the output frequency is increased, the number of samples per cycle decreases. Sampling theory dictates that at least two samples per cycle are required to reconstruct the output waveform. The maximum frequency of the DDFS is $\frac{f_{clk}}{2}$. However the output frequency is less than this to improve the quality of the reconstructed waveform and allow filtering of the output.

Sine Lookup Table

The PA computes a phase angle address for the Look-Up Table (LUT), which outputs the digital amplitude. This corresponds to the sine of the phase angle. The DAC converts the number of into an analog voltage or current.

The output of the PA serves as the address to the LUT/ROM/phase-to-amplitude converter. Each address in a LUT corresponds to a phase point on the sine wave from 0° to 360° . The LUT maps the phase information for the PA to the digital amplitude word that drives the DAC.

DDFS systems can be implemented with ROM or without a ROM. The ROM stores the values of the phase amplitude while the without ROM architecture computes the phase amplitude. The ROM based LUTs are simple to implement. Without a ROM architectures can have higher bit accuracy. For more accuracy the ROM based LUT becomes very large, consumes more power, and becomes slow when compared to the without ROM architectures. ROM LUT provides better Spurious Free Dynamic Range (SFDR) than any without ROM architecture for the same bit width [23].

DAC and Filter

The final component of the DDFS is the DAC and filter. The DAC converts the digital value of the amplitude corresponding to the sine of the phase angle into an analog voltage or current. The DAC and system run at the same reference clock frequency. The DAC adds another stage of quantization error at the output to the sine wave.

Ideally a $\frac{\sin(x)}{x}$ transfer function is used to filter the output of the DAC [23]. It removes the extra frequency components added to the sine wave and hence produces a smooth sine wave.

2.2.3.1 State of the Art

Even an ideal DDFS system will produce harmonics. The amplitude of the harmonics is dependent of the ratio of the output frequency to the clock frequency. Adding a small amount of random noise to the input of the DDFS tends to randomize the quantization errors and reduce this effect. This is called dithering.

A pseudo-random digital noise generator output can be added to the DDFS sine amplitude word before being loaded into the DAC. The amplitude of the digital noise is set to $\frac{1}{2}$ LSB. This accomplishes the randomization process at the expense of a slight increase in the overall output noise floor. In most cases, there is enough flexibility in selecting various frequency ratios to prevent the need for dithering.

3. **Digitally Controlled Synthesizer**

This chapter describes the development and operation of a digital-controlled synthesizer (DCS). The DCS uses digital logic to set the period of the output signal to be an integer number of reference clocks plus an interpolated value between clock transitions by delaying the output using a digital-to-delay converter (DDC) [5]. This is similar to the operation of a direct digital frequency synthesizer without the digital-to-analog converter. The only analog component required is the digital-to-delay converter which has trimmable delay elements that are calibrated to reduce the sensitivity to process and device variations. Other advantages of this approach are immediate frequency hopping ability, wide tuning range, and no jitter accumulation. Die area is also reduced substantially since there is no analog filter required as found in the DDFS.

The DCS uses a fixed frequency clock reference as an input. Because there is no jitter accumulation in the DCS, the jitter is nearly the same as the clock reference. Fast rise and fall times in 90 nm technology aid in achieving the low-jitter goal for the DCS. Since the clock reference is at a fixed frequency and does not need to be tunable, lower jitter is easier to implement on-chip. A fixed external reference with very low jitter can also be used and the synthesizer can generate all other frequencies needed by the IC and maintain the very low-jitter.

Digital controlled oscillators have been designed using a time-to-digital phase detector and a digital filter to drive the digital-controlled oscillator [24]. However, the digital-controlled oscillator is typically a ring oscillator or an LC oscillator. Ring oscillators have a wide tuning range and require small area but have higher phase noise. LC oscillators have lower phase noise and a narrow tuning range but require larger area. Both of these approaches suffer from accumulated jitter.

3.1 Operation

The DCS requires an input reference clock with low jitter and a digital word representing the period T of the output clock divided by the reference clock period T_{clk} . The toggle period of the output is determined by

$$T = 2(N + R)T_{clk} \quad (3.1)$$

where N is a positive integer and R is the fractional remainder less than T_{clk} . The output can be generated by toggling the output after each delay of N reference clock periods plus $R \cdot T_{clk}$. For example, if T_{clk} is 200 ps (5 GHz) and T is 920 ps (1.0869 GHz), then $N = 2$ and $R = 0.3$. The output is toggled at times 0, 460ps, 920 ps, 1380 ps, etc, Figure 18 so that the output frequency will be $4.6 \cdot T_{clk}$. An accumulator is used to determine the fractional delays. The carry output of the fractional delay accumulator signals an extra cycle of delay T_{clk} .

Figure 18 Timing diagram showing the transition of the output signal controlled by the frequency divide and delay accumulator

A 10-bit value of N allows the clock period to range from $T_{\text{clk}}/1024$ to T_{clk} or from 5 MHz to 5 GHz with $T_{\text{clk}} = 200$ ps. A 24-bit delay accumulator provides a 300 Hz frequency resolution and a 7-bit vernier delay line provides picosecond resolution with $T_{\text{clk}} = 200$ ps. The output frequency can be changed instantly by changing the input control word. Figure 19 shows a complete block diagram of the DCS.

Figure 19 Block diagram of digitally-controlled clock synthesizer

There are many different ways to implement vernier delays. Common approaches modify the gate drive or the load capacitance to change the delay. For example, by switching in different load capacitances to control the delay, the gate drive is trimmed to calibrate the length of the delay element to be equal the T_{clk} period, Figure 20. To reduce jitter the delay line must be linear. A look-up table is used to trim the capacitances to linearize the vernier delay.

Figure 20 Block diagram of load capacitance to change delay

The fractional delay accumulator (DA) can dissipate a substantial amount of power. This is similar to the phase accumulator (PA) in a DDFS. The power dissipation of a 32-bit PA designed for a DDFS in 0.18 micron CMOS was over 100 mW at 2 GHz [25]. Although the power dissipation in general is lower in 90 nm technology, the speed has increased to 5 GHz. In the DCS, the output of the DA controls a vernier delay. Figure 21 shows a block diagram of the proposed phase accumulator and delay lines.

The PA in a DDFS is used to address a sine-function look-up table. In the DCS, the output of the DA controls a vernier delay. Unlike a sine-function, delays are linear. If the PA is implemented with only full adders with no carry propagation, the sum consists of the sum of two words, the output sum plus two times the carry output. If these two words control two delay lines in series, the delay will be the same as if the complete sum was generated. This technique cannot be used with the non-linear sine function. This approach greatly reduces the area and power dissipation. The CMOS accumulator in Figure 21 was designed and simulated to operate at 6.25 GHz with a power dissipation of only 80.7 mW.

Figure 21 Block diagram of delay accumulator and vernier delays

Each vernier delay line in Figure 21 needs to be 200 ps long for 5 GHz operation. To minimize jitter in the DCS, the delay of the delay line must be linear. The delay line is a series of CMOS inverters with switches to provide different load capacitances to control the delay. Figure 20 shows one stage of this delay line. Figure 22 shows the delay of a 6 GHz 4-stage CMOS delay line versus a 4-bit control signal with a delay range of about 150 ps. The circuit can be easily modified to provide higher digital resolution and look-up tables can be used to linearize the delay. However the delay is very sensitive to supply variations with 0.5 ps change in delay for each mV change in supply. Power supply noise of 10 mV causes jitter of 5 ps, which is much higher than desired.

Figure 22 Delay of a 6 GHz 4-stage CMOS delay line versus a 4-bit control signal with a delay range of about 150 ps

A divide-by-N circuit is also needed. A designed 10-bit CMOS down counter with preset provides this function. The maximum frequency of operation is near 5.5 GHz. The power dissipation is 5.6 mW.

The delay lines need to be calibrated for linearity and to set the maximum delays equal to T_{clk} . The DCS is designed so that calibration can proceed without interrupting normal operation. An extra delay line is incorporated on chip so that it can be switched in for the delay line to be calibrated. The calibration approach follows.

The delay line has a minimum delay T_{min} and a maximum delay T_{max} . T_{max} minus T_{min} should equal T_{clk} or 200ps for a 5GHz clock signal. In order to reduce the operating frequency of the calibration counters for easier measurement and less power consumption, a delay line with delay T_s of about 1 ns is added in series to the delay line under calibration. Additional logic to form an oscillator that is sensitive only to rising edges is also added. Delay lines typically have

different delays for rising versus falling edges. Only rising clock edges are used to avoid this issue. The output toggles based on accurate delays of the rising clock edges. Thus the output of the DCS is a half rate clock with rising and falling edges precisely controlled. With the delay line set to $T_{\min}$, the count $N_{\min}$ of the number of rising edges occurring during $P T_{\text{clk}}$ cycles is determined. P is several thousand cycles to provide picosecond resolution. The number of rising edges occurring during $P T_{\text{clk}}$ cycles when the delay line set to $T_{\max}$ should be

$$N_{\max} = \frac{N_{\min} \cdot P}{2N_{\min} + P} \quad (3.2)$$

The look-up table is used to obtain this value. The delay lines have a resolution of about 1 ps or $T_{\text{clk}}/128$ (7 bits). To calibrate each delay value i from 1 to 127 the number of oscillations occurring during $P T_{\text{clk}}$ cycles should be

$$N(i) = \frac{N_{\min} \cdot P \cdot 128}{2i \cdot N_{\min} + P \cdot 128} \quad (3.3)$$

This reduces to the $N_{\max}$ equation for $i = 128$ and $N_{\min}$ for $i = 0$. Since the calibration is off-line, speed is not an issue. The multiplications and division can be performed using bit-serial arithmetic to reduce complexity, area and power.

Figure 23 The effects of TID on the threshold voltage and the use of a reverse body bias to restore the threshold voltage

Total ionizing dose effects on modern integrated circuits can cause the threshold voltage of MOS transistors to change because of trapped charges in the silicon dioxide gate insulator. For sub-micron devices these trapped charges can potentially "escape" by tunneling effects. Leakage currents are also generated at the edge of NMOS transistors and potentially between neighbor N-type diffusions. To mitigate these effects reverse body bias (RBB) on the substrate is used to provide radiation hardness for total dose ionizing effects, Figure 23. This approach has been shown to provide up to 1 Mrad Si total ionizing dose hardness with 90 nm SRAMs [26].

Table 1 DCS specifications

Characteristic	
Power Consumption	124mW w/o calibration circuitry
Maximum Frequency	5.5 GHz
Frequency Tuning Range	4.8 MHz to 2.5GHz
Frequency Resolution	300 Hz with 24 bit Delay Accumulator
Layout Area	8mm X .36mm

4. Design of Components

The DCS is a digital design with the exception of the analog delay lines. Digital design techniques were used to optimize the design.

- Gates with more than 4 transistors in a row were avoided because delay grows quadratically with the number of transistors in series.

Figure 24 Detailed block diagram of DCS

- The latest arriving signal was connected to the transistor closest to the output node when possible, improving the transition speed of the circuit.
 - Diffusion nodes were shared in the layout wherever possible to reduce capacitance.
 - Multiple circuit families were considered to optimize the logic function of a circuit.
- The design explored Current Model Logic (CML), Pseudo-NMOS, and static CMOS.

Figure 24 shows a detailed block diagram of the DCS. The major components are discussed in the following section.

4.1 Delay Accumulator

The delay accumulator is a large adder. The sums and carries of the accumulator are handled separately. At each clock period, the delay accumulator sums its output to the loaded FCW. The output is used to control the amount of delay generated by the delay lines.

Since delays are linear they do not have to be propagated if two separate delay lines are used. This technique allows for higher speed operation without the need to pipeline the process. The amount of logic used is also reduced lowering the total power consumption.

The delay accumulator accepts a 24 bit FCW. While only the 8 MSB are used to control the delay lines, the system provides frequency resolution in the delay lines similar to a phase accumulator in a DDS. The frequency resolution is given by

$$f_{out} = \frac{f_{clk}}{2^n} \quad (2.15)$$

For $n = 24$, f_{out} equals 300 Hz.

Triple mode redundancy is used in the accumulator on the 8 MSBs. The sum and carry of each of these bits is voted in order to remove the effects of Single Event Upsets (SEU). A SEU occurs when the charge deposited on the surface of the FET is sufficient enough to flip the value of a digital signal.

Type	Power Consumption	Operating Frequency	Number of bits	Latency
Accumulator	86.113 mW	6.25 GHz	23	1 clk

4.2 Frequency Divider

A frequency divider is used in the DCS to create different frequency ranges. The delay accumulator controls the output frequency within each. The frequency divider is implemented using a digital counter with digital logic that resets the counter after a number of input clock

Figure 25 Johnson counter connected to ripple adder

cycles, equal to the division ratio, has been counted. This type of divider has been shown to successfully operate at speeds up to 10 GHz. This type of frequency divider also offers low power consumption and digital programmability. The binary counter consists of two separate parts; a high speed 3 bit synchronous counter, and a low speed semi-synchronous ripple counter, Figure 25.

A Johnson counter is used as the high speed 3 bit synchronous counter in the frequency divider because of its high speed operation and it provides access to the individual digits. The Johnson counter consists of 7 D-type master-slave flip-flops. An and-or-invert AOI22 multiplexer is attached to the front of each flip-flop. The multiplexer selects the input into the flip-flops resetting them to their initial configuration when a clear signal is present or at the start of each count.

4.2.1 Cell Design

Generating a counter that would operate at 10 GHz or 5GHz proved to be very difficult. The difficulty lay in finding a D-flip flop that was able to operate at 5GHz, and was low power. The main component in a binary counter is a D flip-flop. In a D flip-flop the input portion of the circuit is transparent when the clock is at logic 0. At this point the intermediate node is reproducing the incoming signal. When the clock switches to logic 1, the input of the circuit is no longer transparent. The intermediate node value is passed to Q. The reset logic is needed to load the initial state (zero) every time the counter reaches a number of cycles corresponding to the desired division ratio. The first design that was tested used current mode logic.

Current Mode Logic

Current Mode Logic (CML) flip-flops were explored as part of the design of the frequency divider. The CML flip-flop was much faster than the static CMOS designs and successfully operated at more than 11 GHz. CML logic has a very small voltage swing which increases the speed. The voltage difference is the voltage drop across the resistor. CML circuits usually do not use PMOS transistor which degrade the circuit maximum operation frequency (bandwidth) [30].

Figure 26 Schematic of CML D flip flop

CML flip-flops use differential pairs. A tail current provides an input-independent biasing for the circuit. The differential voltage swing of a CML flip-flop is around the device threshold voltage providing extremely high speed switching operation.

CML flip flops have several problems though. First the logic level must be converted to the standard complimentary level to be processed by other digital logic. Second CML flip flops take more layout area because resistors used for the voltage drop do not scale with technology. Finally the power consumption of the CML flip-flop is larger than the complementary logic. This is caused by the large tail current source used in the CML flip flop. A three bit CML counter consumed 10.7 mW at 5.5 GHz while the complementary logic design only used 7.44 mW at the same frequency.

Complementary Logic

A complementary logic cell was evaluated next. While the complementary cell could not operate at 10 GHz, an implementation was possible at 5GHz. Complimentary logic circuits offer good noise margins, are fast, low power, insensitive to device variations, easy to design, and widely supported by CAD tools [29].

Figure 27 Schematic of complimentary D flip-flop

A D flip flop can be created by wiring together 4 AOI22 gates, Figure 28. AOI22 is a compound gate that implements the AND/OR INVERTING function in a single stage. A simple reset can be implemented with a NMOS transistor connected to the intermediate node. The intermediate node has a small capacitive load, a NMOS device shunted to ground can discharge the node and reset the D flip flop quickly. While a PMOS device tied in the same way can pull the output to V_{DD} and preset the signal. Unfortunately the capacitive loading caused by the reset/preset circuitry prevented the AOI22 based flip-flop from properly dividing the 5 GHz signal down to 2.5 GHz.

4.2.2 Reset Control

A different approach was needed to implement a reset/preset for a high speed frequency divider. The complementary D flip flop would operate at 5 GHz without the reset/preset circuitry so a different method was needed to reset/preset the upper bits of the frequency divider that did not rely on pulling the output nodes to V_{DD} or GND.

A Johnson counter was implemented to handle this problem. A Johnson counter is essentially shift register with the output connected back to the input, Figure 28. A single pulse is passed through a cascade connection of flip flops. The position of the pulse determines the count. The reset/preset function was then implemented by controlling the value that is loaded into each D flip flop.

Figure 28 Block diagram showing the operation of a Johnson counter

A Pseudo –NMOS multiplexer is used to control the reset and preset of the Johnson counter. The pull-down network in Pseudo-NMOS logic is like that of a static gate, but the pull-up network is replaced with a single PMOS transistor that is grounded so it is always on. The

PMOS transistor width is selected to be about 1/4 the strength of the NMOS pull-down network to provide a compromise between noise margin and speed [29].

For a full 8 count, the Johnson counter is initialized to 0000001 at the start of each count. The 1 then propagates through each D flip flop until the counter is reset which takes 1 count.

0000001
0000010
0000100
0001000
.....
1000000

When a count of less than eight is needed, a control signal of the desired count enables the lower transistor. The transistor tied to the output is enabled by the D flip flop currently containing the pulse, Figure 30. So that when the desired D flip flop contains the pulse the counter is reset.

Figure 29 Pseudo-NMOS multiplexer used to reset Johnson counter.

Pseudo-NMOS gates will not operate correctly if $V_{OL} > V_{IL}$ of the receiving gate [29].

This can occur during corner simulations of a strong PMOS transistor and a weak NMOS transistor. A biasing circuit is used to reduce the process sensitivity. The biasing circuit delivers a V_{bias} that is independent on the relative nobilities of the NMOS and PMOS devices.

4.2.3 Ripple Adder

The ripple adder is a low performance counter that handles the higher order bits at lower frequency. This design uses JK flip-flops that are triggered by the enable signal from either the Johnson counter or the CMOS counter. Table 2 shows a truth table of a JK flip-flop.

Table 2 Truth table for JK Flip Flop

J	K	Q_{next}	
0	0	Q_{prev}	Hold State
0	1	0	Set
1	0	1	Reset
1	1	$\overline{Q}_{prev}$	Toggle

A JK flip-flop can be created using a standard D flip flop. A two input AND gate is used to tie the output, Q, of the D flip flop back into the input the J input. The complementary output, $\overline{Q}$, is then tied to the K input. Figure 30 shows the schematic of a JK flip flop that uses a single clock signal.

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Topic	January	Complementary	Review
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Number of bits	3	3	7
Latency (input to output)	6 clock periods	1.25 clock periods	1 clock period

4.3 Delay Lines

A delay line is used to delay a signal transmission for a fixed time. The delay line uses shunt capacitors and gate delays to generate the required delay, Figure 31. The delay line is designed to have 300ps of delay. While only 200ps are necessary for the delay line to function properly at 5GHz, the additional 100ps is added in case the chip is produced in a fast process. The calibration circuitry can then directly map the frequency control word to the correct amount of delay as long as 200ps of delay is still available.

Table 4 Delay line properties

Type	Power Consumption	Operating Frequency	Delay range	Propagation delay
Analog Delay Cell	5.3845mW	5 GHz	0-300ps	3 clock cycles

Figure 31 Block diagram of delay line structure

4.3.1 Vernier Delay Lines

The vernier delay line is constructed using a capacitive loaded inverter line. The capacitors are binary weighted and tied to the driving buffer with an NMOS switch. When the digital signal from the RAM activates the switch the capacitance is tied to the output of the signal. The time to charge and discharge the line becomes larger and increases the delay

This type of delay line is very susceptible to variation in the power supply. Supply variations can produce a 0.5ps change in delay for each mV of change. Power supply noise of 10 mV causes jitter of 5 ps, which is much higher than desired. A voltage regulator is necessary for the power supply driving the vernier delay lines to control this problem.

4.3.2 Block Delay Lines

The block delay is created by a series of inverters with output tied to a multiplexer. Each inverter has approximately a 15 ps gate delay. The inverters are organized to continue the binary sequence of the vernier block. Unfortunately the gate delay does not strictly adhere to the binary scheme. Outputs of the first block delay are 0ps, 30ps, 60ps and 90ps delay. The second block delay has outputs of 0ps, 120ps, 180ps, and 240ps. The actual gate delay will vary depending on the process and temperature variation. Fortunately, by calibrating the delay line and storing the values in a look-up table any desired amount of delay is possible by combining the output of the vernier delay block and the two block delays. For example, to obtain a delay of 176ps, 26ps would be obtained from the vernier delay block, 30ps is obtained from the first block delay, and 120ps is obtained from the second block delay. ($120 + 30 + 26 = 176\text{ps}$)

Figure 32 Example of delay line use to accomplish delay

4.3.2 RAM

Three RAMs are used in each delay line configuration. Each RAM consists of an address decoder and the block RAM. The block RAM for each vernier contains 192 bits and a 32 bit RAM is used for the delay block RAM. Each delay line will have a total 415 bits of RAM.

Figure 33 Schematic of single memory cell

Each memory cell is made up of two inverters, a weak inverter and a strong inverter. When the memory cell is written, the weak inverter is overpowered to set the desired logic state. The strong inverter is used to control the NFET that writes to the bus. An AND gate acts as a write enable signal between the address and the write signal, Figure 33.

Table 5 RAM properties

Type	Power Consumption/ Delay line	Operating Frequency	Read time	Write time
Memory	2.34 mW	1 GHz	175.8ps	173.4ps

4.3.3 Control

As the modified clock travels down the delay lines, it accumulates both desired controlled delay and undesired delay caused by the processing in the digital logic. This delay affects the timing of the control signal from the RAM. The control signals must be delayed to match the propagation of the modified clock signal.

The control signals from the accumulator are clocked at half clock rate because of the ping-pong nature of using two delay lines. In the DCS, the reduced clock rate is 2.5 GHz. That gives the signal 400ps to propagate through the delay line. The time to propagate through a delay block can vary from 320ps to 485ps depending on the amount of capacitance added to the line. This is too large of a variation for the control pulse to accurately set the modified clock period.

To help correct this problem, digital delay was added to the block delay lines. The digital delay matched the delay in the control signal to the delay received by the modified clock. This reduces the delay variation seen by a single delay block to 130ps to 180ps. But this does not address the propagation delay of the system.

The time for a single pulse to propagate through the sum and carry delay lines can vary from 1.04ns to 2.45ns. That is from 2 to 6 clock cycles. Figure 34 show the block delays and their respective clock variations from the initial pulse. The amount of block delay depends on the position in the system and the amount of control delay added to the pulse. In the case of the first delay block, no addition control signal delay is necessary. But the fourth delay block needs from 2 to 5 clock cycles of delay on its eight control lines.

Figure 34 Block diagram showing the propagation of the control signal to the delay blocks

Digital delay has to be added to the control lines to match the propagation of the modified clock signal. The delay has to be variable to match the change caused by the addition of delay in

previous parts of the delay line. Multiplexers are used to choose the amount of delay. The multiplexers are controlled by the RAM output.

4.4 Calibrator

Calibration of the delay lines is necessary for several reasons. First, local variations will make the delay lines non-linear if they are not calibrated. Variations in process and temperature will affect the total amount of delay different delay lines can produce.

The calibration process begins on power up of the chip. The minimum delay of all the delay lines is measured. The delay line under test is connected to a ring oscillator with about 800ps of additional delay. This reduces the oscillation frequency of the delay line to about 1 GHz. The 5 GHz count- down counter is initialized to 8192 or 2^{13} . The number of pulses passing through the ring oscillator is counted. Once all the delay lines have been measured, the delay lines are set to the highest minimum delay plus 15 ps. The 15ps will allow the circuit to be adjusted in the case where the minimum delay shifts.

The calibrator then takes the first delay line and calibrates the initial delay again. This initial delay is again compared to the minimum delay to insure that it is still valid. If it is no longer valid the calibration cycle will start over again.

If the minimum delay is still valid, the calibrator will initialize the RAM at the 1ps address with 1ps of delay. There is 7-bits address space on the delay line that provides approximately 1ps of resolution. The number of pulses is measured again and if 1ps of delay has

been added correctly the count will increase by one. For each control value $i=0-128$, the count on the ring oscillator should be given by EQ 3.3.

$$N(i) = \frac{N_{\min} \cdot P \cdot 128}{2 \cdot i \cdot N_{\min} + P \cdot 128} \quad (3.3)$$

where: $P = 8192$.

A high P achieves 1ps resolution in the delay line.

Two sets of carry and sum delay lines are calibrated before the DDFS can be placed in operation. The clock signal is split between to two lines to allow the change of the capacitance in the delay line to settle between pulses. The accumulator control signal is clocked alternately into each delay line updating each at a 2.5GHz rate.

A third set of delay lines is provided for calibration while the circuit is in operation. This delay line is switched into the circuit and the first delay line is calibrated again. In this way the circuit is constantly being calibrated.

4.5 Design for testability

While this paper focuses on the design and simulation of the DCS, testability of the physical design was built into the design process. A scan-design strategy for testing was implemented at the important control points of the system. Registers designed with scan operate in two modes. In normal mode the register operates in the expected way. However, during scan they are connected to form a shift register. If there are N bits in the scan chain, N clock pulses are applied in scan mode, so that all N bits of state in the system can be shifted out and a new N

bits could be shifted in. This makes it possible to observe the operation of the important control bits in the system, facilitating easy debugging.

The scan chain used in this system is made up of a D flip flop preceded by a multiplexer, Figure 35. When the SCAN signal is deasserted the register behaves as a conventional register, storing the value on the D input. When the SCAN signal is asserted, the data is loaded from the ACC_SER_IN pin, which is connected in shift register fashion to the previous register Q output in the scan chain.

At control points where inserting a multiplexer into the line negatively affects the operation of the system (i.e. the delay accumulator output), a small buffer is used to connect the control line to the input of a scan chain flip flop. At high speed the small buffer limits the amount of additional capacitive loading seen by the control line. However, the buffer will not be able to process the signal. If the system clock rate is slowed down though, the buffer will be able to process the signal and the value of the control line can be scan chained out. Full scan chains are placed at the control points between the RAM and delay lines, and between the calibration unit and the RAM. A read only scan chain was placed between the delay accumulator and the RAM address decoder.

Figure 35 Scan chain used to output values of delay accumulator

5. Simulation and Layout

This section describes the simulation and layout of the DCS. The simulation of the system was conducted in two parts. The individual components were designed and simulated using Cadence Design Tool and Synopsis HSPICE. The calibration algorithm and delay line operation were simulated using Mentor Graphics ADMS.

The standard cells were generated using a layout generator called LGen. LGen was developed at WSU and consists of a hierarchical database and associated routines in C++ [27]. Foundry and process independence is achieved by coding directly using design rules. The complexity of using design rules directly is hidden somewhat by using functions and objects in the C++ language to generate transistors, guard rings, standard cells, etc. This approach allows the designer to achieve identical results to full custom layout for maximum density.

LGen is planned to be released as open-source software with no proprietary software needed. CMOS standard cell generators were modified by adding an option to lay out cells with a separate reverse body bias to provide radiation hardness. Design rules for IBM's 90 nm process were placed into the LGen database and CMOS NAND, NOR, inverters, some and-or-invert gates and latches were generated.

The layout was then generated using Mentor Graphics IC Station. Parasitic EXtraction (PEX) was then run to prove that the layout functioned correctly.

5.1 Simulation

Simulation began by verifying the functionality of each logic block. Measurements were taken of power consumption and operation speed. The total delay of each component was of particular importance because of the nature of the system.

5.1.1 Simulation of components

Accumulator

The delay accumulator was first measured for functionality. A FCW is loaded into the delay accumulator and correct output should be available at the correct clock cycle. Figure 36 shows the simulated output of the delay accumulator with a FCW of 30000 HEX or the 16th and 17th bit set to 1. The output is the accumulated delay at each clock cycle. Notice that the carry is propagated to the next incremental sum bit on the next clock cycle. This is the proper function of the delay accumulator.

Figure 36 Simulation of delay accumulator output for a FCW of 3

The delay accumulator also has triple mode redundancy on the 8 MSB. This system was tested to insure that the proper vote was performed. In Figure 37, a distorted sine wave was input to one of the voting cells. As the bottom cell clearly illustrates the voter circuitry ignores this anomaly as long as the other two results are in sync.

Figure 37 Delay accumulator voting when a errant signal is introduce for one of the cells.

Frequency Divider

The frequency divider was tested to insure that the counter functioned properly. The time to reset the counter and the correct preset operation were also important. Figure 38 shows the correct operations of all the bits in the 7 bit ripple counter used in the frequency divider.

Figure 38 Output of counter

The transition points of the counts are very important. As Figure 39 demonstrates the synchronization of the 3rd and the 9th bit are nearly perfect. This is important for the total accuracy of the system by making it easier to synchronize the two counters.

Figure 39 Transition point of the 3rd and 9th bit of ripple counter

The Johnson counter output was also plotted, Figure 40. The first signal represents a count by two; the second signal represents a count by three; and so on. The correct operation of the Johnson counter is highlighted by the fact that the 6th count of the count by 2 and count by 3 signals overlap perfectly. The same is true for the 8th count for the count by 2 and count by 4.

Figure 40 Johnson counter output

Delay line

Delay line operation was tested to insure that the correct delay was achievable for a given control word. It was also important that the signal not be degraded to the point that was not useful to drive the output. It was also imperative that NMOS and PMOS FETs of the digital delay line be balanced so that the modified clock signals did not grow while they are in the separate delay lines. This would prevent them from being successfully recombined to drive the output.

5.1.2 Simulation of calibration algorithm

The calibration algorithm was tested using Mentor Graphics ADMS. The calibration begins by determining the initial count through the delay line, Figure 41, 320. The RAM location is then set to position 1. The delay is incremented until the count is decreased by one. This technique gives less than 2ps of resolution.

Figure 41 Output of Calibration of Delay lines

5.1.3 Simulation of system

Timing is the most critical part of the system. The flip signal from the frequency divider must be timed so that it corresponds to the correct modified clock pulse. The control signal from the delay accumulator must be timed to correspond to the propagation of the modified clock pulse. The signal from the RAM must be delayed to correspond to the delay within a single delay line. As Figure 42 shows the modified clock signal used to time the output of the frequency divider when the delay accumulator is loaded with a 3.

Figure 42 Output clock signal when FCW of delay accumulator is loaded with 3

Figure 43 shows the output of the DCS, the output is a digital pulse with a frequency of 357 MHz.

Figure 43 Output of DCS with the frequency divided by 8 and a FCW of 3 in the delay accumulator

Figure 44 Output of DCS when delay accumulator is changed during operation

Figure 44 shows the effects of changing the control word of the DCS. When a new control word is loaded into the delay accumulator, the capacitance on the delay line is changed. At the top of Figure 44, it is possible to see the effect on the modified clock signal. The bottom of Figure 44 shows how these modified clock signals change the output of the DCS.

5.2 Layout

The following figures show the layout of the DCS with a close up view of the most important components. Figure 45 shows a system view of the three delay lines, the frequency divider, and the delay accumulator.

Figure 45 Layout of system

Figure 46 Delay line layout

Figure 46 shows the layout of the delay line. The largest component of the delay line is the memory blocks.

Figure 47 Delay accumulator layout

Figure 47 and Figure 48 show the delay accumulator and frequency divider layout respectively.

Figure 48 Frequency divider layout

6. Conclusion

This thesis discusses the implementation of a digitally controlled synthesizer (DCS) that operates at 5GHz in the IBM 90nm process. A digital counter is used to set the period of the output signal to be an integer number of reference clocks while the time-to-delay accumulator creates an interpolated value between clock transitions by delaying the output. The system has an on-chip calibrator to linearize the analog delay lines and provides 1ps resolution from the delay accumulator.

The DCS frequency is controlled by the Frequency Control Word (FCW). The output frequency can be quickly changed by simply changing the FCW to provide an immediate frequency hopping ability like a DDFS. However unlike the DDFS, the DCS does not require large analog filters to smooth the output signal.

The DCS has a wide tuning range like a ring oscillator. It has low jitter like a LC oscillator. But both of these approaches suffer from accumulated jitter. Because the DCS uses a fixed frequency clock reference as an input there is no jitter accumulation. The jitter is nearly the same as the clock reference.

6.1 Major contributions

- Design and layout of a 5GHz Digitally Controlled Synthesizer (DCS)
- Design of a 10 bit CML counter that operates at 10GHz
- Design and layout of a 3 bit Johnson counter that operates at 5 GHz
- Design and layout of a 24 bit novel delay accumulator

- Design and layout of 32ps vernier delay line that uses shunt capacitors.
- Design and layout of digital line from 32ps-240ps
- Comparison of different types of VCO and frequency synthesizers
- Discussion of CML, Pseudo-NMOS, and static CMOS families

6.2 Future Work

The work presents many avenues for future research. The initial design of the DCS is a proof of concept. While digital controlled oscillators have been designed using a time-to-digital phase detector and a digital filter to drive a digital-controlled oscillator [24]. The use of a delay accumulator to control the vernier delay lines is new. The DCS still needs to be fabricated and the simulated results compared to the measured chip values.

Further research into the use of CML gates to maximize the frequency of operation is also recommended. CML gates show the potential to operate above 25GHz in the 90nm process. This type of gate would be very useful if a way to limit the high power consumption could be found. Increasing the frequency of operation reduces the amount of delay necessary for the delay line. Use of CML gates at higher frequency could potentially save power by reducing the need for large driver buffers for the capacitance of the delay lines and the digital time delay necessary to synchronize the delay accumulator control signal to the modified clock signal.

Several simple improvements include things like increasing the size of time-to-delay accumulator for finer resolution. The calibration algorithm could also be explored and optimized to increase performance and reduce power consumption. An on-chip voltage regulator design

could also be explored as well as other techniques to reduce the effects of power supply fluctuations on delay.

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