A LOW INPUT VOLTAGE ENERGY HARVESTING CHARGE PUMP WITH LOAD-ADAPTIVE PUMPING FREQUENCY

By

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To the Faculty of Washington State University:

The members of the Committee appointed to examine the thesis of EVAN ANDREW JURAS find it satisfactory and recommend that it be accepted.

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A LOW INPUT VOLTAGE ENERGY HARVESTING CHARGE PUMP

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Abstract

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Harvesting energy from ambient sources is becoming a promising method of powering new Internet-of-things (IoT), wireless sensor networks (WSN), and implantable biometric sensor technologies. However, the voltage produced by energy harvesters such as thermoelectric generators, piezoelectric generators, and RF harvesters is typically too low to be used for analog and wireless circuits. A key component to enable energy harvesting's application to IoT and other technologies is a high-efficiency voltage upconverter that can reliably transform low voltages produced by energy scavengers into higher voltages that are more useful. Switched-capacitor circuits such as charge pumps are compact and can be implemented fully in an integrated circuit, so they are ideal voltage upconverters for volume-constrained applications.

This thesis presents a load-adaptive charge pump with wide input voltage range that allows it to provide high-efficiency performance with a variety of energy harvesting sources in multiple system applications. A novel method of controlling the pumping frequency by comparing the output voltage to a self-generated reference voltage is implemented. The load-adaptive functionality reduces the charge pumping frequency at light loading conditions to avoid

unnecessary switching loss, and increases pumping frequency at heavy conditions to provide more current to the output. The layout of the circuit, which is implemented in the TowerJazz SBC13HX 0.18μm, is presented and post-layout simulations are performed. The circuit achieves an operating voltage range of 0.2 – 0.8V, has a peak efficiency of 64%, and a high throughput power of up to 1.8mW at 0.8V. The efficiency is maintained above 60% over a range of loading conditions, and efficiency at light load conditions is improved compared to standard fixed-frequency charge pumps.

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1. INTRODUCTION

1.1. Charge Pump Applications in Energy Harvesting

Recent improvements in energy harvesting technologies and the development of ultra low-power electronics have enabled the creation of devices that are powered by ambient energy from their surroundings [1]. These devices, which can range from biometric sensors, to wireless sensor networks (WSNs), to Internet-of-things (IoT) nodes, add intelligence to autonomous systems and increase remote monitoring capability in areas that are difficult to physically access. A key component of these devices is an efficient DC-DC converter that can take the lower voltages produced by energy harvesters and boost them to higher voltages that are usable by the sensor, control, and communication portions of the system. There are two types of circuits that can implement a low voltage up-converter: a capacitive type, such as a charge pump, and an inductive type, such as a boost converter. Inductive converters that are able to up-convert input voltages as low as 20mV have been developed [2]. However, inductive converters require bulky off-chip inductors or transformers that prevent their use in extremely volume-constrained applications. A charge pump can be fully implemented in a small silicon integrated circuit, allowing it to be utilized in applications where small form-factor is required.

Energy harvesting systems can be designed to work with a multitude of energy harvesting sources. Four primary energy harvesting technologies that exist today are: i) solar, ii) thermoelectric, iii) sediment microbial fuel cells, and iv) RF harvesters. Each of these sources have different power, open-circuit voltage, and impedance characteristics. Table 1 gives a summary of expected power densities and open-circuit voltage ranges of these four energy harvesting sources.

Table 1. Energy Harvesting Sources

Source	Open-Circuit Voltage Range	Maximum Power Density	Reference
Small Solar Cell ($11cm^2$)	0 – 0.63V @ 200 Lux	70 mW/cm^2 @ 200 Lux	[3]
Thermoeletric Generator	0 – 0.75V @ $\Delta T = 5K$	10.84 mW/cm^2 @ 0.38V ($\Delta T = 5K$)	[4]
Sediment Microbial Fuel Cell	0 – 0.91V	12 mW/m^2 @ 0.5V	[5], [6]
RF Harvester	0 – 1V @-22.44dBm	88.9 uW/cm^2 * @ 0.6V, -18dBm	[7]

*Not including antenna area

Table 1 shows that the voltage produced by energy harvesting sources is minimal and can vary significantly depending on the amount of power received by the source. A charge pump which has been designed to operate over a small range of input voltages (for example, 450mV – 550mV) will have limited application. A charge pump that is able to function over a wide range of input voltages will be able to be used with multiple types of energy harvesting sources over a range of power conditions. This motivates the development of a charge pump that can operate efficiently at low and high input voltages.

1.2. Design Challenges

The primary challenge facing energy harvesting charge pumps is the need to operate at low input voltages. As seen in Table 1, some power sources will only develop tenths of volts at the output, and have optimal operation at low voltages. Difficulties arise when the input voltage drops below the standard threshold voltage for the MOSFETs used in the integrated charge pump, because the MOSFET switches are not able to be completely turned on and off. Various

state-of-the-art charge pumps have implemented techniques to allow operation at sub-threshold voltages; these are discussed in Section 2.2 of this thesis.

A second challenge is that the voltage produced by the energy scavenging source varies significantly with the amount of power being received by the source. For example, Table 1 shows that a microbial fuel cell will produce a voltage ranging from 0 – 910mV. As the input voltage increases past the threshold voltage, transistor drive strength changes significantly. This causes a problem with ring oscillator circuits, whose frequency is given as

$$f_{osc} = \frac{I_{SS}}{2NC_{osc}V_{DD}} \tag{1.1}$$

where N is the number of inverter stages, C_{osc} is load capacitance of each stage, I_{SS} is the current through the transistors (essentially drive strength), and V_{DD} is the supply voltage (and the peak to peak amplitude of the voltage waveform) [8]. If a charge pump uses a self-contained oscillator rather than an external oscillator to generate the pumping frequency, then the pumping frequency will vary significantly due to the change in drive strength. Figure 1 shows a typical five-stage ring oscillator and the simulated frequency when V_{DD} is varied from 300mV – 800mV.

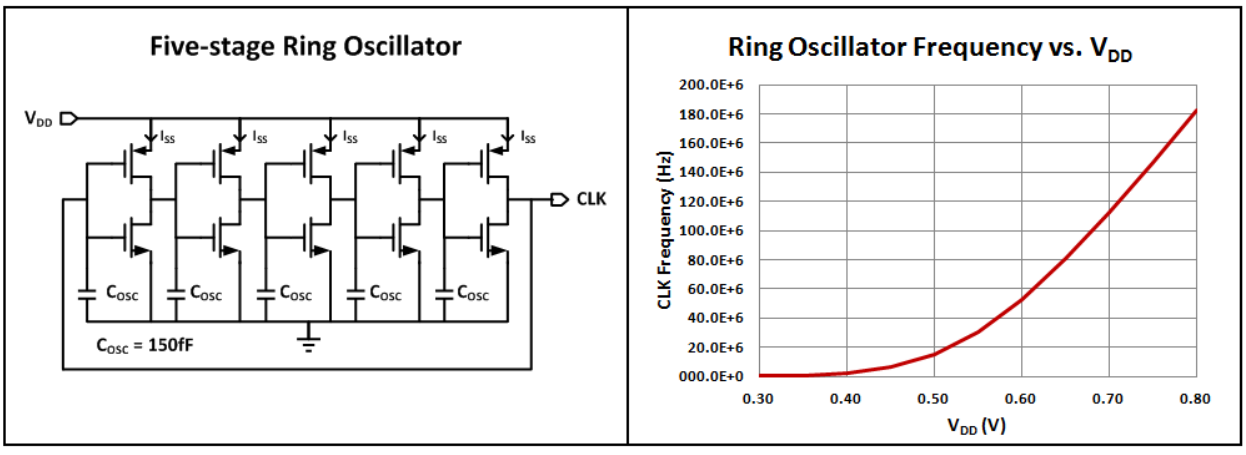

Figure 1. Ring oscillator frequency variation with VDD

The CLK frequency is 286.5kHz at V_{DD} = 300mV, and 182.5MHz at V_{DD} = 800mV. This wide range of frequencies presents a design challenge. If the frequency is too fast at high V_{DD}, the output voltage will be near ideal levels but efficiency will be unnecessarily degraded by switching loss. Conversely, if it is too slow at low V_{DD}, switching loss will be minimal but output voltage will be low. The optimal pumping frequency for charge pumps depends on loading conditions, desired output voltage, and switching loss, as will be discussed in Section 3.2.

A third challenge is that loading conditions at the output of the charge pump vary significantly depending on the state of the system it is powering. For example, in a wireless sensor node, the sensor is in an idle state for a majority of the time, but it periodically powers up to take a reading and transmit wireless data [9]. This activity requires a large amount of power and represents a sudden increase in load to the charge pump. When the power requirement is high, the pumping frequency should be fast to provide more current to the load and maintain output voltage. However, when the system is in a low-power idle state, pumping frequency should be low to avoid wasting energy through unnecessary switching loss.

Simulation data from parametric sweeps of pumping frequency done on a basic pump topology over a range of input voltages and loading conditions are shown in Figure 2.

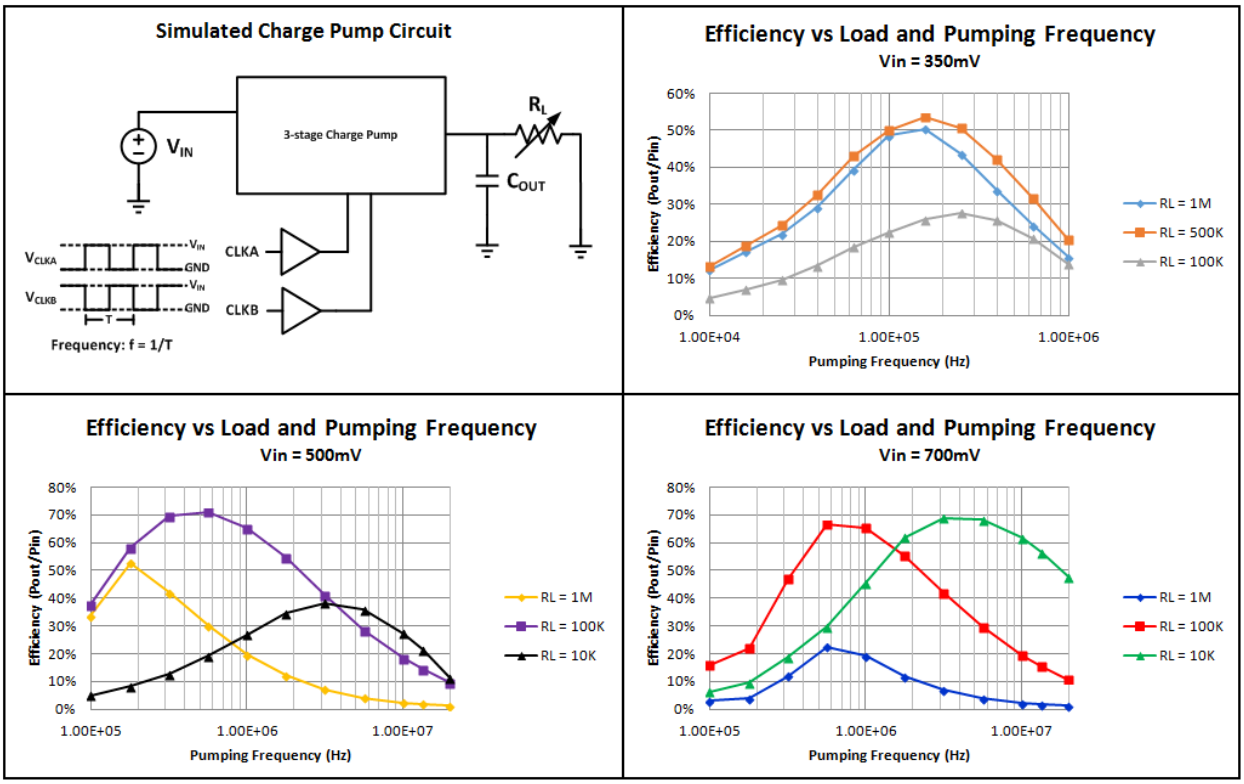

Figure 2. Charge pump efficiency vs. frequency for various loads and input voltages

The data shows that efficiency varies widely with frequency, and that the optimal pumping frequency (the frequency at which the pump operates with the highest efficiency) changes depending on output load and input voltage. This promotes the need for a charge pump with a controlled pumping frequency that responds to changes in load and input voltage.

1.3. Proposed Charge Pump Topology

To address the challenges, this thesis proposes a charge pump topology with a load-adaptive pumping frequency and wide input voltage range. The proposed circuit (shown in Figure 3) uses feedback to cause the pumping frequency to increase when the output load increases, and to decrease when load decreases.

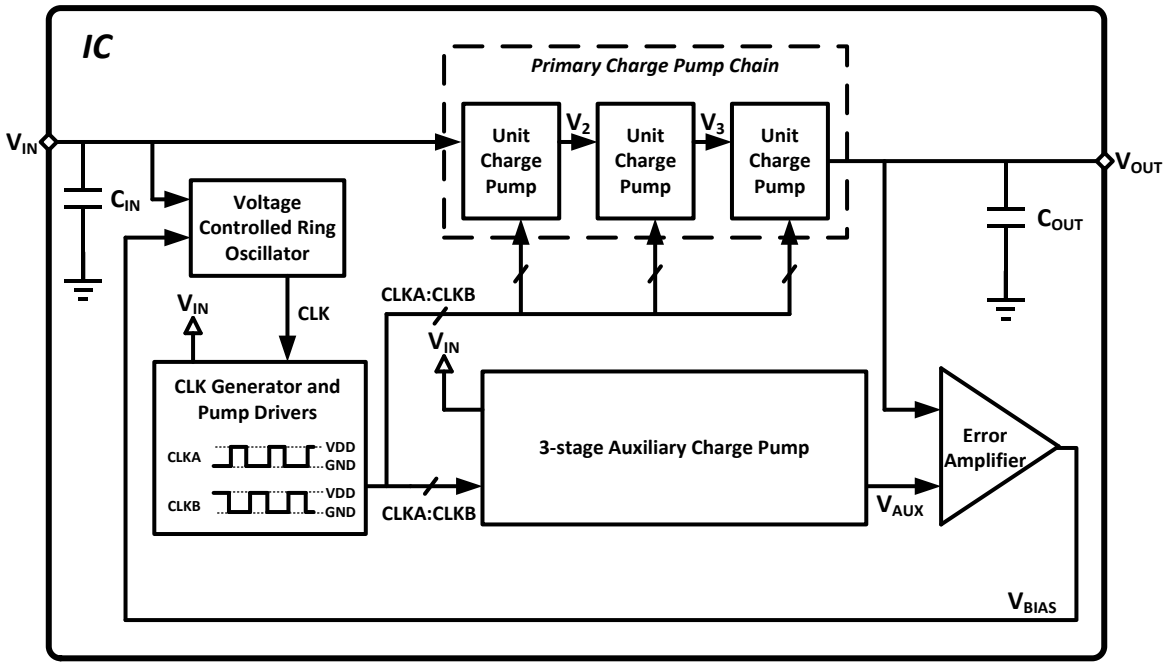

Figure 3. Block diagram of proposed load-adaptive charge pump

This is achieved by comparing the output voltage (V_{OUT}) to a self-generated low-power reference voltage (V_{AUX}), and generating a bias voltage (V_{BIAS}). V_{BIAS} is fed to a voltage controlled ring oscillator to control the pumping frequency. Under heavy loading conditions, V_{OUT} will be below V_{AUX}, causing V_{BIAS} to increase, and increasing the pumping frequency to provide more current to the load. Under light loading conditions, V_{OUT} will be near V_{AUX}, causing V_{BIAS} to decrease, and decreasing the pumping frequency to avoid unnecessary

switching loss. The proposed circuit improves efficiency at light load conditions while maintaining good performance at heavy load conditions over a wide range of input voltages.

1.4. Thesis Organization

This thesis is divided into five sections. The first section introduces energy harvesting charge pumps and their design challenges. The second section is a literature review that reviews state-of-the-art charge pumps, presents existing theory on charge redistribution loss (switching loss), and discusses charge pump figures of merit. Section three presents the principles of operation of the proposed charge pump and the design and layout of each sub-block: the primary charge pump, auxiliary charge pump, voltage controlled ring oscillator, clock generator, and error amplifier. Section four presents post-layout simulation results of the charge pump's performance and a comparison to state-of-the-art charge pumps. Section five concludes the thesis and is followed by a bibliography.

2. LITERATURE REVIEW

2.1. Principles of Charge Pump Operation: Dickson Charge Pump

The fundamentals of how a charge pump boosts a low voltage to a high output voltage can be understood by studying the basic Dickson charge pump, a widely used charge pump topology that was published in 1976. A Dickson charge pump [10] is shown in Figure 4. The pump uses two antiphase clocks to pass packets of charge along the chain of diode-connected NMOS as the pumping capacitors are charged and discharged during each half clock cycle.

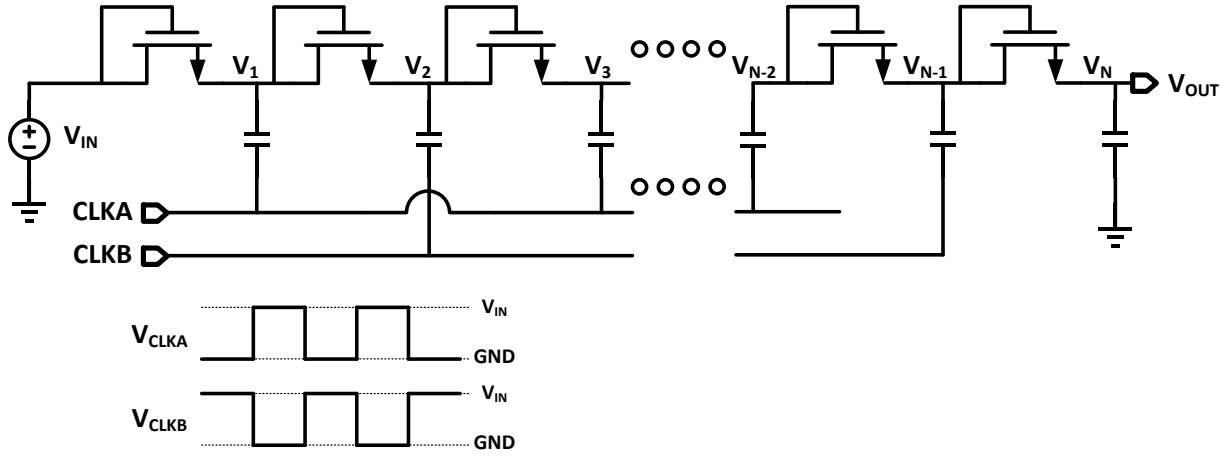

Figure 4. Dickson charge pump

Assuming ideal components and that all internal node voltages ($V_1 – V_N$) start at 0V, node V_1 will charge to $V_1 = V_{IN} - V_T$, where V_T is the NMOS threshold voltage, during the clock phase when CLKA is 0V. The instant CLKA switches from 0V to V_{IN}, the voltage at V_1 will be boosted to $V_1 = (V_{IN} - V_T) + V_{IN} = 2V_{IN} - V_T$, because voltage across a capacitor cannot change instantaneously. During this phase, current is prevented from flowing backwards from V_1 into the input node by the diode-connected NMOS, and the charge in C_1 is shared with C_2. The voltage at V_2 charges to $V_2 = 0.5(V_1)$, assuming $C_1 = C_2$ and that perfect change transfer occurs. In the second half of the clock phase, when CLKB switches from 0V to V_{IN}, V_1 is once again

charged to V_{IN} - V_T, while V_2 is boosted to $V_2 = 0.5(V_1) + V_{IN}$, and the charge in C_2 is shared with C_3. The process repeats itself, passing packets of charge further down the capacitor chain, charging each of the internal nodes and C_{OUT}. When charge equilibrium is reached, the voltage at the output of the N-stage charge pump can be expressed as,

$$V_{out} = (N + 1)(V_{in} - V_T) \tag{2.1}$$

If a load is attached to the output, the charge pump will continuously supply an output current I_{OUT}, which can represented as an amount of charge per pumping period, $I_{OUT} = \Delta Q*f$, where f is the pumping frequency. The charge ΔQ is supplied from each stage to the following stage, dropping the voltage of each internal capacitor by $\Delta V = \Delta Q/C$, or $\Delta V = I_{OUT}/(C*f)$. Thus, the output voltage of a N-stage charge pump with pumping capacitors of size C when supplying an output current of I_{OUT} can be expressed as,

$$V_{out} = (N + 1)(V_{in} - V_T) - \frac{NI_{OUT}}{Cf} \tag{2.2}$$

A ripple voltage also develops at the output, because the load resistance R_L constantly discharges the output capacitance, C_{OUT}. Assuming C_{OUT} is large compared to C, the voltage ripple V_R is given as,

$$V_R = \frac{I_{OUT}}{fC_{OUT}} = \frac{V_{OUT}}{fR_LC_{OUT}} \tag{2.3}$$

Since its publication in 1976, the Dickson charge pump has been widely used in CMOS devices to generate high on-chip from a lower supply voltage for operations such as charge storage in nonvolatile memory.

2.2. State-of-the-Art Energy Harvesting Charge Pump Topologies

As submicron processes developed and supply voltages became closer to process threshold voltages, the V_T drop and body effect of the Dickson charge pump rendered it unsuitable [11]. A V_T cancelling cross-coupled charge pump topology where the internal nodes of two opposite-phase parallel pump chains are used as gate voltages for NMOS switches (rather than having them diode-connected) was introduced to allow voltage boosting of low supply voltages [12]. However, in energy harvesting applications, the supply voltage may be lower than the threshold voltage, causing the charge pump switches to operate in the subthreshold region where conduction loss becomes a large factor in performance. Several state of the art topologies have been published to improve performance by reducing conduction loss. The following two topologies are reviewed because they were used as inspiration for the load-adaptive topology proposed in this thesis.

2.2.1. "A 0.15 V Input Energy Harvesting Charge Pump With Dynamic Body Biasing and Adaptive Dead-Time for Efficiency Improvement"

The topology published in [13] uses boosted switch gate voltages, dynamic body biasing, and adaptive dead time to achieve high power conversion efficiency and a minimum input voltage of 150mV. A block diagram of the topology is shown in Figure 5.a, and a unit charge pump cell is shown in Figure 5.b.

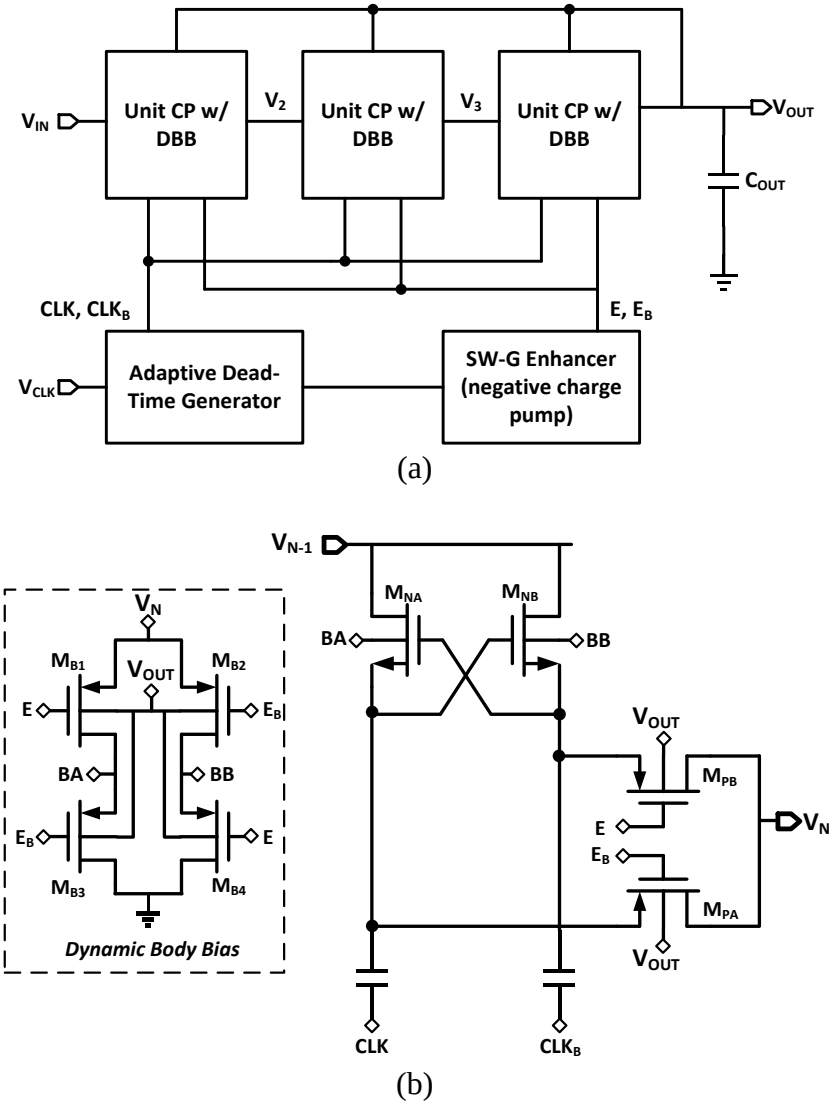

Figure 5. Charge pump with dynamic body biasing and adaptive dead-time [13]

The charge pump circuit includes a negative auxiliary charge pump to generate the boosted PMOS gate voltages (E, E_B). E and E_B are opposite-phase clocks that switch between $-V_{IN}$ during the conducting phase and V_{OUT} during the off phase. Driving the gate voltage to $-V_{IN}$ pushes $|V_{GS}|$ of the switch higher, increasing the conductance and on-current I_D of the switch while reducing conduction loss.

The circuit implements a dynamic body biasing (VTCMOS) technique to modulate the NMOS transistor threshold voltage, lowering it to improve conduction through the NMOS during the on-state and increasing it to prevent reverse leakage during the off-state. This is accomplished by tying the NMOS bodies in deep n-well to a node that is switched to ground during the conducting phase and to the stage output voltage during the off phase.

Finally, the circuit uses an adaptive dead-time technique to maintain a sufficient non-overlapping period between pumping phases. Dead-time, or the period where neither CLK signal is high, is critical for cross-coupled charge pumps to prevent the output voltage from being shorted to lower voltage internal nodes. The non-overlapping period must be short enough to maximize current transfer during each phase, but must also be long enough to avoid large short-circuit currents between pump stages. The dead-time is generated by delay cells, which are highly sensitive to transistor drive strength. As input voltage increases above subthreshold levels, drive strength increases significantly and dead-time is shorted. This circuit uses an adaptive dead-time generating circuit that uses a short delay path when the input voltage is low, and switches to a long delay path when the input voltage rises above a certain threshold. This allows dead-time to be maintained over a wide range of input voltages.

This circuit is able to achieve high throughput power at low input voltage, and good efficiency over a wide operating range. However, it requires off-chip capacitors and an external clock signal, so it cannot be implemented as a fully integrated circuit and has limited use in volume-constrained applications.

2.2.2. "An Inductorless DC-DC Converter for Energy Harvesting With a 1.2-µW Bandgap-Referenced Output Controller"

A second published charge pump circuit [14] uses a four-phase topology with a bootstrapped path and an auxiliary switch path in a fully integrated circuit (no external components). It also uses a low-power bandgap reference voltage to perform skip mode regulation to maintain the output at 1.4V. A diagram of the topology is shown in Figure 6.

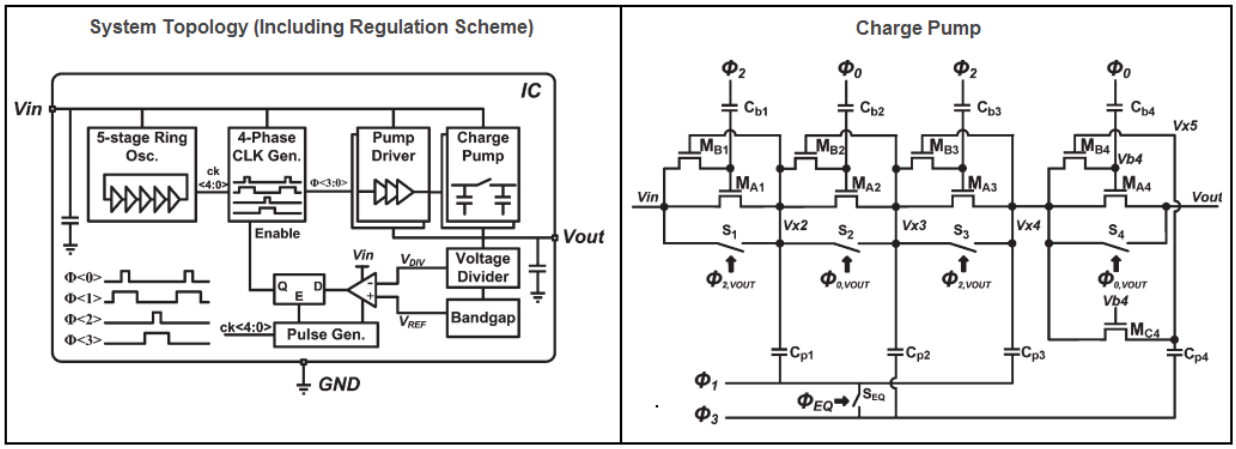

Figure 6. Regulated charge pump topology with bootstrap startup path

During startup, the current flows through zero- and low- V_T transistors M_{A1} – M_{A4}, which are gated by boosted voltages from the input. The low threshold voltages allow the charge pump to operate at low input voltages. However, these transistors do not work as efficiently because their low V_T does not allow them to be turned off as well, which causes significant leakage

current. To improve efficiency, higher efficiency switches $S_1 – S_4$ are placed in parallel with $M_{A1} – M_{A4}$. These switches are clocked by a boosted signal generated from the output voltage. As the output voltage rises, $S_1 – S_4$ begin to carry the majority of the current so high efficiency can be achieved.

An output regulation scheme is implemented by compared the divided output voltage (V_{DIV}) to a reference voltage (V_{REF}) through a latch comparator. If V_{DIV} is higher than V_{REF} (i.e., if the output voltage is higher than the desired regulated voltage), the pumping clock is disabled so that current is no longer transferred to the output. This allows switching loss to be decreased at light load conditions while providing a stable 1.4V output voltage.

Some drawbacks to this circuit are that it requires a power-consuming bandgap reference voltage, and draws continuous power through the resistor divider at the output, degrading efficiency. It also requires high cost zero- and low- V_T devices.

2.3. Charge Pump Figures of Merit

For charge pumps used in energy harvesting applications, there are several key performance parameters. The important figures of merit are: minimum operating input voltage, power efficiency, voltage conversion efficiency, input voltage range, and silicon area required.

Minimum operating input voltage

The lower the voltage the charge pump is able to operate at, the less power that needs to be received by the source for system operation. Thus, minimum operating voltage directly reduces the input sensitivity (dBm) of a system, which is a key figure of merit for wireless sensor nodes and other energy harvesting applications.

Power conversion efficiency (PCE)

Due to the limited amount of ambient energy available in energy harvesting applications, the power available to the source is typically on the order of microwatts. Any power lost to voltage conversion will significantly reduce the power available to the system. Charge pumps must be as efficient as possible (even in lossy subthreshold conditions) so energy from the source is not wasted.

Voltage conversion efficiency (VCE)

Voltage conversion efficiency is defined as the actual charge pump output voltage divided by the ideal output voltage ($VCE = V_{OUT}/V_{OUT,ideal}$).

Input voltage range

As seen in Table 1, energy harvesting sources can produce a wide range of voltages depending on the amount of power received by the source. Increasing the input voltage range of a charge pump gives it the flexibility to be used with various types of sources over a range of power conditions. The maximum input voltage is typically limited by the breakdown voltage of

the process. The TowerJazz 0.18μm SBC13HX process has 3.3V breakdown transistors available, so the maximum input voltage for the proposed charge pump is limited to 0.8V, so the output voltage does not exceed 3.2V.

Silicon area

Energy harvesting systems are typically targeted for extremely volume-constrained applications such as biomedical implants, dust-mote sized sensors, or wearables [1], [14], where even 2x2mm ICs push the allowable size limit. The less area that is required for the charge pump, the smaller the system can be, which allows it to be applied in more volume-constrained areas.

3. CHARGE PUMP SWITCHING LOSS AND OPTIMAL PUMPING FREQUENCY

An exhaustive review of published charge pumps revealed that little research exists on evaluating the optimal pumping frequency for a charge pump circuit. Most charge pump designs choose a specific pumping frequency based on voltage ripple requirements and available area [14] or use an existing system clock or as the pump frequency [13], [15]. However, the simulation results shown in Figure 2 indicate there is an optimal frequency at which a charge pump circuit operates at the highest efficiency. The optimal frequency is dependent on load and the amount of switching loss present in the circuit. A goal of this thesis is to analyze sources of charge pump switching loss and use the analysis to determine an expression for optimal pumping frequency based on output load.

3.1. Charge Pump Switching Loss

In this thesis, switching loss is defined as the energy that is not transferred from the input to the output during each switching cycle, but instead is dissipated in components in the circuit. There are four chief contributors to switching loss: i) Charge redistribution loss (E_{rds}), ii) charging and discharging of parasitic capacitances (E_{par}), iii) conduction loss due to power dissipated in switch resistances (E_{cond}) , and iv) reversion loss caused by backwards current flow (E_{rev}). In the proposed charge pump, the total charge lost in each switching cycle due to these effects is expressed in (3.1).

$$E_{loss} = E_{rds} + E_{par} + \sum E_{cond} + \sum E_{rev} \tag{3.1}$$

3.1.1. Charge redistribution loss

This section reviews the discussion on charge redistribution loss presented in [16]. If two capacitors C_1 and C_2, with initial voltages V_1 and V_2, are suddenly connected in parallel through

an ideal switch as shown in Figure 7, charge redistribution occurs and the potential across both capacitors settles to V_F.

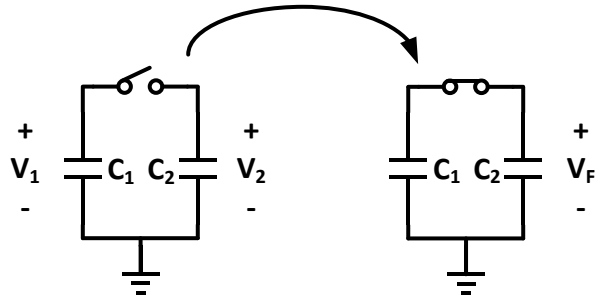

Figure 7. Basic redistribution loss

Using the law of conservation of charge and performing an analysis on the overall energy stored before and after the capacitors are placed in parallel,

$$C_1V_1 + C_2V_2 = (C_1 + C_2)V_F \tag{3.2}$$

$$\mathrm{V_F} = \frac{\mathrm{C_1V_1 + C_2V_2}}{\mathrm{C_1 + C_2}} \tag{3.3}$$

Considering the initial and final energy stored in the circuit by applying $E = ½C*V^{2,}$

$$E_i = \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2 \tag{3.4}$$

$$E_f = \frac{1}{2}(C_1 + C_2)V_F^2 \tag{3.5}$$

$$\mathrm{E_{rds} = E_i - E_f = \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2 - \frac{1}{2}(C_1 + C_2)V_F^2} \tag{3.6}$$

Substituting (3.3) into (3.6) and simplifying,

$$\mathrm{E_{rds} = \frac{1}{2}\frac{C_1C_2}{C_1 + C_2}(V_1 - V_2)^2} \tag{3.7}$$

Equation (3.7) is an expression for the amount of energy lost to charge redistribution. In a charge pump circuit, the same redistribution loss occurs during each switching cycle. Figure 8 shows a representation of the charge redistribution that occurs in each stage of the charge pump.

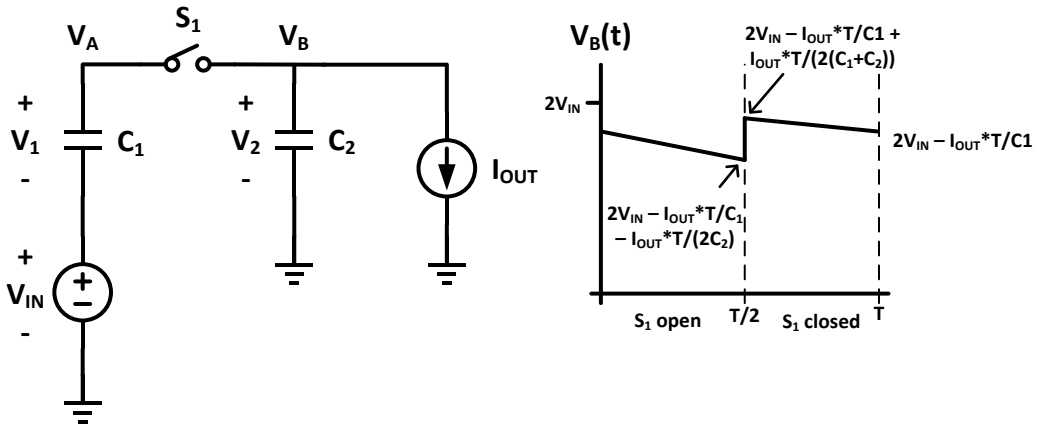

Figure 8. Charge redistribution in a charge pump stage

While S_1 is open, the current load drains C_2, reducing V_2 at a constant rate. The instant S_1 closes, V_2 is boosted by the additional charge from C_1, causing charge redistribution loss proportional to the voltage difference between nodes V_A and V_B at that instant. The voltages before and after S_1 closes are indicated in the graph; these are derived in [16]. Using the same approach that is used to derive (3.7), and assuming $V_A = 2V_{IN}$ before S_1 closes, the expression for the redistribution energy loss in each stage of the charge pump circuit is derived as:

$$E_{rds} = \frac{1}{2}\frac{C_1 C_2}{C_1 + C_2}\frac{V_{OUT}}{R_L}T\left(\frac{1}{C_1} + \frac{1}{2C_2}\right)\left(2V_{IN} - \frac{V_{OUT}}{R_L}T\left(\frac{1}{C_1} + \frac{1}{2C_2}\right)\right) \tag{3.8}$$

Equation (3.8) and the voltage equations shown in Figure 8 are derived in [16]. To obtain the total energy lost to charge redistribution, (3.8) must be multiplied by 2(N-1) to account for the number of stages with two parallel phases, where two redistributions occur in each switching cycle in each stage. The last stage has a large output capacitor (1nF), so the redistribution loss is

negligible compared to the first two stages, hence the (N-1) term. The proposed charge pump uses 220pF pumping capacitors, so $C_1 = C_2 = 220pF$, and has three two-phase stages.

3.1.2. Charging of Parasitic Capacitances

The overall capacitance that will be charged and discharged in each cycle can be quantified by considering the transistor capacitances and the wire capacitances. The inverter and logic stages in the ring oscillator circuit, clock dead time generator, and clock power buffers all have node voltages that switch from 0V to V_{IN} on every clock cycle. Figure 9 shows the capacitances associated with an inverter stage (an inverter is analyzed because the clock-related circuitry consists primarily of inverters).

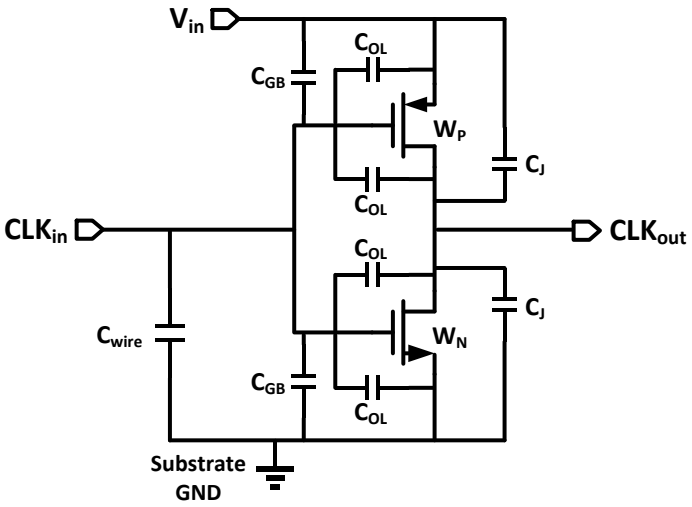

Figure 9. Capacitances associated with inverter stage

The total parasitic capacitance (C_L) for a transistor include the gate-to-body (C_{GB}), gate-to-drain or gate-to-source overlap capacitance (C_{OL}), and the junction capacitance (C_J). C_{GB} capacitance is dependent on bias voltage, but $C_{GB} = C_{ox}WL$ can be used to determine a worst-case value, where C_{ox} is the thin oxide capacitance term ($F/\mu m^2$) [17]. C_{OL} can be determined from the drain/source overlap capacitance term C_{ol} ($F/\mu m$) as $C_{OL} = C_{ol}W$. The drain (output)

junctions of each transistor also contribute to overall capacitance, because in each cycle, the drain switches from 0V to V_{IN}. The junction capacitance is expressed as $C_J = C_jWY$, where C_j is the junction area capacitance term ($F/\mu m^2$) and Y is the effective length of the junction (measured as 0.58μm for a typical transistor in the proposed circuit). The TowerJazz 0.18μm SBC13HX process datasheet gives values for thin oxide (C_{ox}), drain/source overlap (C_{ol}), and junction area (C_j) capacitances; these are shown in Table II. The total parasitic capacitance for each transistor is

$$C_L = C_{GB} + 2C_{OL} + C_J = C_{ox}WL + 2C_{ol}W + C_jWY \quad (3.9)$$

Each inverter stage has two transistors, so the total parasitic capacitance is the sum of C_{Ln} (NMOS parasitic capacitance) + C_{Lp} (PMOS parasitic capacitance).

A simple expression for lumped wire capacitance is

$$\mathrm{C_{wire}} = \mathrm{C_{int}W_wL_w} \quad (3.10)$$

where C_{int} is the wire capacitance to substrate ($F/\mu m^2$), W_w is the wire width, and L_w is the wire length [17]. This expression does not account for coupling capacitance to adjacent wires, but is sufficient because the wires carrying clock signals in the proposed layout are relatively isolated from other wires. Table 2 shows the SBC13HX datasheet values for C_{int} for Metal 1 – Metal 6 wires.

Table 2. TowerJazz SBC13HX Process Capacitances

Variable	**Description (from datasheet)**	**Min.**	**Nom.**	**Max.**	**Units**
C_{ox}	Gate oxide capacitance - thin oxide	8.6	9.5	10.5	fF/μm
C_{ol}	Gate overlap drain/source	365	395	435	aF/μm
C_j	P+/N+ junction area capacitance	800	1000	1200	aF/μm^2
$C_{int,M1}$	Metal 1 to substrate	27.5	32.6	40.1	aF/μm^2
$C_{int,M2}$	Metal 2 to substrate	13.3	15.1	17.5	aF/μm^2
$C_{int,M3}$	Metal 3 to substrate	8.8	9.8	11.1	aF/μm^2
$C_{int,M4}$	Metal 4 to substrate	6.6	7.3	8.1	aF/μm^2
$C_{int,M5}$	Metal 5 to substrate	4.4	4.8	5.3	aF/μm^2
$C_{int,M6}$	Metal 6 to substrate	3.1	3.3	3.5	aF/μm^2

The energy provided by the source to charge the parasitic node capacitances in the circuit for each switching cycle is given in (3.11), where ΣC_L and ΣC_{wire} are the total transistor and wire capacitances connected to a switching node:

$$E_{par} = \frac{1}{2}\left(\sum C_L + \sum C_{wire}\right) V_{IN}^2 \tag{3.11}$$

E_{par} represents the switching loss factor for the charge pump.

The combined wire and transistor parasitic capacitances for the proposed charge pump circuit are shown in Table 3. The values given in Table 2 are used to calculate the total capacitance of the transistors and wires from equations (3.9) and (3.10).

Table 3. Total parasitic capacitances of proposed charge pump

Transistor Parasitic Capacitance		
Circuit	Total transistor width (μm)	Total capacitance (pF)
VCO	60.00	0.652
Clock generator	164.0	1.783
Power buffers	19640	213.5
	Total transistor capacitance:	216.9 pF

Wire Parasitic Capacitance		
Wire type	Total wire area (μm^2)*	Total capacitance (fF)
Metal 1	0	0
Metal 2	875.8	13.22
Metal 3	24240	238.5
Metal 4	1578	11.53
Metal 5	93940	4.791
Metal 6	1582	5.221
	Total wire capacitance:	746.6 fF

Total Parasitic Capacitance:	217.6 pF

* Only considering area of wire connected to clock signals

The primary contributor to E_{par} comes from the transistor capacitance of the large power buffers in the two-phase clock generator circuits, which are each nearly the size of a single 220pF pumping capacitor in the proposed layout.

3.1.3. Conduction Loss and Reversion Loss

In each pumping cycle, current flows through a charge transfer switch during the charging phase, and then through a load transfer switch during the pumping phase. The channel resistance of these switches causes power dissipation (conduction loss), especially at subthreshold voltages. Additionally, in a cross-coupled charge pump, overlap between pumping phases can cause high voltage output nodes to be shorted to lower voltage internal nodes, causing reverse short-circuit current flow (reversion loss). These effects are illustrated in Figure 10.

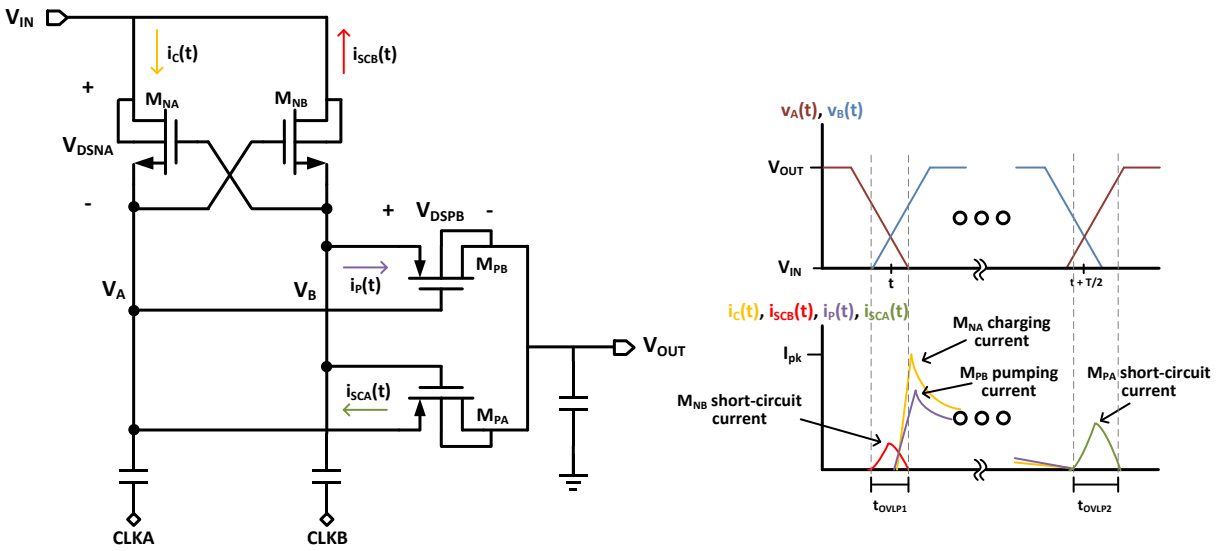

Figure 10. Conduction and reverse currents (only one half-phase shown)

A slight V_{DS} drop exists across the NMOS and PMOS transistors while they conduct charging or pumping current. This causes a conduction loss of

$$E_{cond} = \int_0^{T/2} i(t) v_{DS}(t) dt \tag{3.12}$$

in each transistor in each half-switching cycle. The conduction loss occurs regardless of whether there is overlap between clock periods or not, and is strongly dependent on how high the gate voltage is above the threshold voltage.

Short-circuit conditions occur when the tail ends of CLKA and CLKB overlap one another, or when there is insufficient dead-time between pumping phases. If the voltage at internal node V_A is high while V_B begins to be boosted by CLKB, current will flow backwards through the turned-on M_{NB} transistor to V_{IN}. This is illustrated as $i_{SCB}(t)$ in Figure 10. Similarly, if V_A begins to be boosted high while V_B is low, M_{PA} will conduct current backwards from V_{OUT} to V_A. The backwards charge flow caused by short-circuit conditions is expressed in (3.13), and

the reversion loss due to the power dissipated in transistors by reverse current is expressed in (3.14).

$$Q_{rev} = \int_0^T i_{sc}(t)dt \tag{3.13}$$

$$E_{rev} = \int_0^T i_{sc}(t)v_{DS}(t)dt \tag{3.14}$$

The backwards charge flow causes the output voltage to be less than the ideal voltage due to the loss of charge, but does not contribute significantly to energy loss.

For the numerical analysis at the end of Section 3.2, the values of E_{cond} and E_{rev} are obtained by integrating the simulated voltage and current waveforms of the transistor switches at V_{IN} = 500mV, R_L = 100kΩ, and T = 500kHz. In this condition, the NMOS transistors each have E_{cond} = 700.0fJ per cycle and E_{rev} = 629.8aJ per cycle. The PMOS transistors each have E_{cond} = 1.034pJ per cycle and E_{rev} = 12.27fJ per cycle.

3.2. Optimal Pumping Frequency

The efficiency of a charge pump, as with any power converter circuit, can be expressed in one of the forms given in (3.15).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{E_{out}}{E_{in}} = \frac{E_{out}}{E_{out} + E_{loss}} \tag{3.15}$$

E_{out} is a function of the pumping period:

$$E_{out}(T) = P_{out}T = \frac{V_{out}^2}{R_L}T \tag{3.16}$$

As discussed in Section 2.1, the output voltage for an N-stage charge pump as a function of pumping period T is,

$$V_{out}(T) = (N+1)V_{IN} - N\frac{I_L T}{2C} \tag{3.17}$$

(Equation (3.17) has been slightly adjusted from equation (2.2) to represent a cross-coupled two-phase topology, where V_T is not a factor and there are two pumping phases in each period.) Substituting $I_L = V_{OUT}/R_L$ into (3.17) and simplifying,

$$V_{out}(T) = \frac{(N+1)}{(1 + \frac{NT}{2R_L C})}V_{IN} \tag{3.18}$$

Substituting (3.18) into equation (3.16) and simplifying gives a complete expression for output energy as a function of pumping period:

$$E_{out}(T) = \frac{TV_{IN}^2(N+1)^2}{R_L\left(1 + \frac{NT}{2R_L C}\right)^2} \tag{3.19}$$

The overall efficiency of the charge pump as a function of pumping period can be expressed as:

$$\eta(T) = \frac{E_{out}(T)}{E_{out}(T) + E_{loss}(T)} \tag{3.20}$$

where $E_{out}(T)$ and E_{loss} are defined in (3.19) and (3.1), respectively. Equation (3.20) assumes that E_{loss} is relatively independent of the pumping period compared to the E_{out} term, as T only appears in the charge distribution portion of E_{loss}. By taking the derivative of $\eta(T)$, setting it equal to 0, and solving for T, the optimal pumping period can be found. However, this results in an unwieldy equation, so a numerical analysis where $\eta(T)$ is plotted using component values is performed instead.

To plot $\eta(T)$ as a function of T, parameter values are plugged into the $E_{out}(T)$ and E_{loss} terms of (3.20) for V_{IN} = 500mV, R_L = 100kΩ, and I_{OUT} = 15μA. Table 4 gives a summary of the terms and the numerical parameters for the proposed charge pump that are plugged in to equations (3.19), (3.8), (3.11), and (3.12) and simplified. The table gives perspective to the size of the various contributions to switching loss. As observed in Section 3.1.3, the reversion loss is small compared to the conduction loss, so it is considered negligible and is not included in the table.

Table 4. E_{out} and E_{loss} terms for proposed charge pump at V_{IN} = 500mV, R_L = 100kΩ

Energy Term	**Energy output (E_{out})**	**Charge redistribution loss (E_{rds})**	**Parasitic capacitance loss (E_{par})**	**Conduction loss (E_{cond})**
Equation	(3.19)	(3.8)	(3.11)	(3.12)
Parameters	V_{IN} = 500mV R_L = 100kΩ N = 3 C = 220pF	N = 3 $C_1 = C_2$ = 220pF V_{IN} = 500mV	V_{IN} = 500mV C_L = 216.9pF C_{wire} = 746.6fF	E_{condN} = 1.034pJ per PMOS E_{condP} = 700.0fJ per NMOS
Predicted output or loss per switching cycle (J)	$E_{out}(T) = \frac{40\mu * T}{(1 + 68.2k * T)^2}$	$E_{rds}(T) = \frac{V_{OUT}}{800k} T(1 - 22.7k * T)$	$E_{par} = 27.20p$	$E_{cond} = 3.468p$

The terms in Table 4 are plugged in to equation (3.20) and plotted as a function of switching period (T) to obtain the graph in Figure 11.

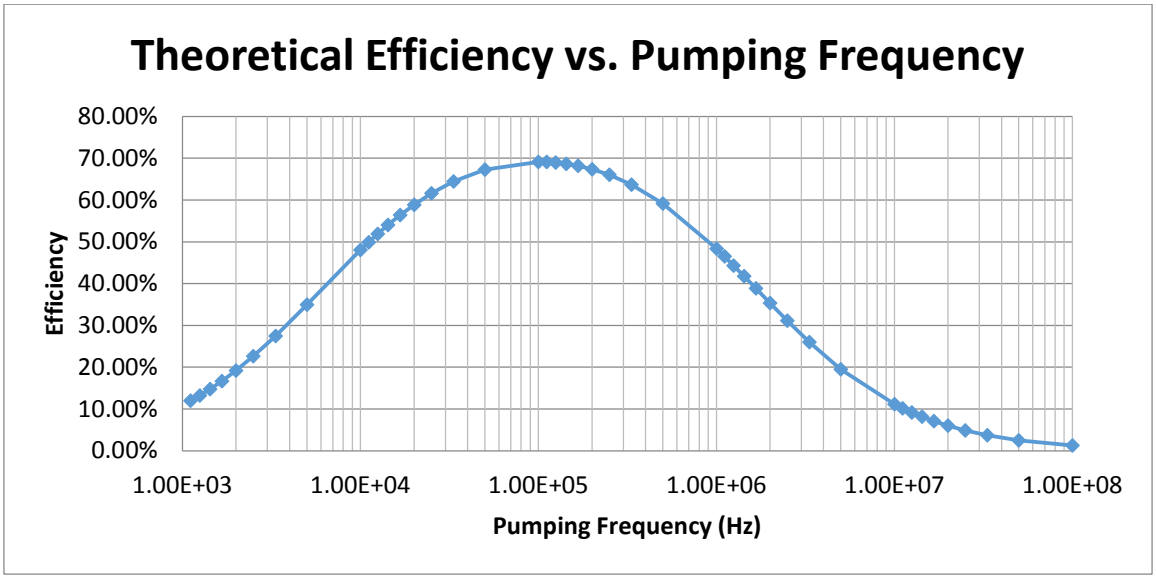

Figure 11. Numerical analysis of optimal pumping frequency

The optimal pumping frequency predicted in Figure 11 is 125kHz for a predicted efficiency of 68.94%. The simulated optimal pumping frequency shown in Figure 2 for V_{IN} = 500mV and R_L = 100kΩ is 562kHz for an efficiency of 71%. The theoretical analysis predicts values that are close to what is seen in simulations. The difference between the theoretical and simulated optimal frequency is small considering the range of frequencies (1kHz – 100MHz). Thus, the switching losses discussed in this section are an accurate representation of all the losses encountered in a charge pump, and optimizing equation (3.20) can be used to get a close estimate of what the pumping frequency should be designed as for a given circuit. The equations in this section also indicate that optimal pumping frequency will change with input voltage and loading condition. This motivates the need for a charge pump with a pumping frequency that adapts to changes in load to track the optimal frequency as closely as possible.

4. PROPOSED CHARGE PUMP ARCHITECTURE AND SUB-BLOCK DESIGN

4.1. Top-level Description

The proposed charge pump implements a load-adaptive pumping frequency scheme to achieve high-efficiency operation over a wide range of input voltage and output loading conditions. The charge pump frequency adapts to the size of the load at the output: if the load is large, the pumping frequency increases to transfer more current to the output, and if the load is small, the pumping frequency decreases to reduce switching loss while still maintaining the desired output voltage. The proposed charge pump consists of five subcircuits: the primary charge pump chain, a three-state auxiliary charge pump, an error amplifier, a voltage controlled ring oscillator (VCO), and a clock generator with power buffers. For convenience, Figure 3 is shown again here so it may be referred to in the following description.

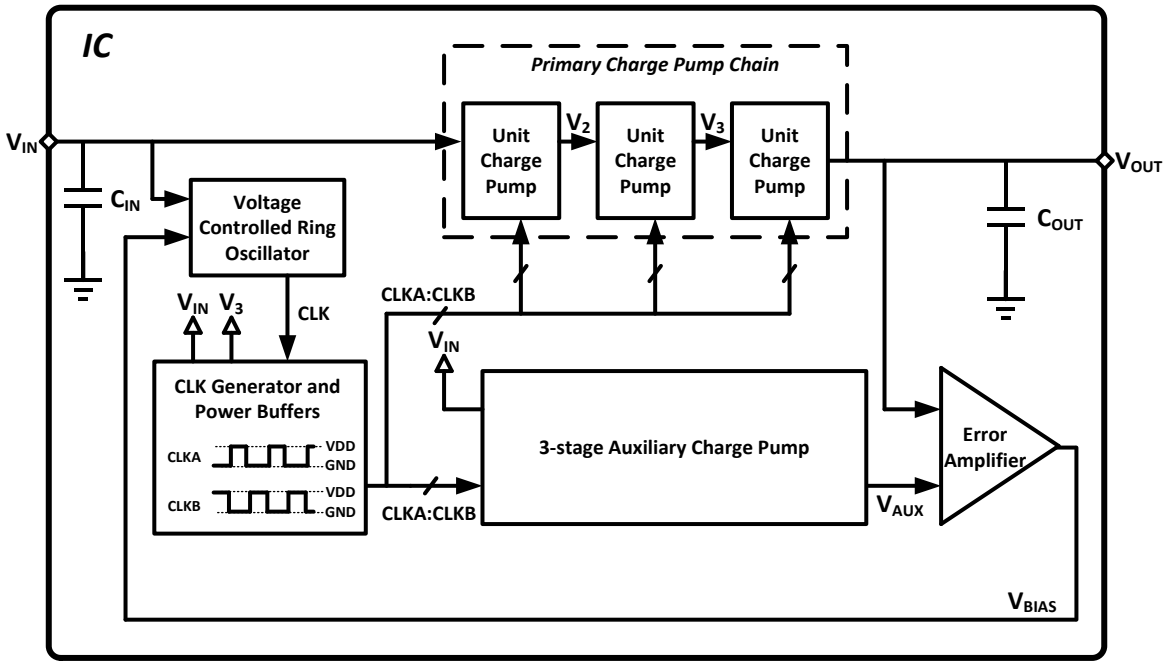

Figure 12. Block diagram of proposed load-adaptive charge pump (repeated)

Charge is transferred from the input to the output capacitor through a three-stage charge pump that is driven by large clock buffers. In steady-state operation, V_{OUT} is ideally quadruple the input voltage, i.e. $V_{OUT} \approx 4*V_{IN}$. However, V_{OUT} will vary between V_{IN} to $4*V_{IN}$ depending on the load condition and the pumping frequency. The output of the auxiliary charge pump is also ideally quadruple the input voltage, i.e. $V_{AUX} \approx 4*V_{IN}$. V_{AUX} consistently remains close to $4*V_{IN}$ because the output of the auxiliary charge pump is not connected to a load. Thus, V_{AUX} is used as a reference voltage that is compared to V_{OUT}. V_{AUX} and V_{OUT} are fed to the error amplifier, which generates a DC bias voltage (V_{BIAS}) ranging from $0.2*V_{IN}$ to V_{IN}. The larger the difference between V_{AUX} and V_{OUT}, the higher V_{BIAS} is. The bias voltage is routed back to the VCO, whose frequency is linearly dependent on V_{BIAS} when V_{BIAS} is in the range of $0.2*V_{IN}$ to V_{IN}. The variable clock frequency generated by the VCO is fed to the CLK generator circuit, which creates two anti-phase non-overlapping clock signals, CLKA and CLKB, which switch between 0V and V_{IN}. CLKA and CLKB are driven by large power buffers, these buffers drive the pumping current for the primary charge pump and the auxiliary charge pump.

When the output load is increased (decreased), the following sequence occurs:

1. V_{OUT} drops (rises) in response to the increased (decreased) load, while V_{AUX} remains constant
2. V_{BIAS} increases (decreases) due to the increased (decreased) difference between V_{AUX} and V_{OUT}
3. CLK frequency increases (decreases) as V_{BIAS} increases (decreases)
4. Increased (decreased) pumping frequency causes more (less) current to be delivered to the output, increasing (maintaining) V_{OUT} close to the ideal output voltage

The circuit is designed to meet the following specifications:

- Operate over an input voltage range of $300mV < V_{IN} < 800mV$
- Produce an output voltage in the range of $1.2*V_{IN} < V_{OUT} < 4*V_{IN}$ for the following loading and input voltage conditions:
    - $R_L > 250k\Omega$ for $300mV \leq V_{IN} < 400mV$
    - $R_L > 10k\Omega$ for $400mV \leq V_{IN} < 600mV$
    - $R_L > 1k\Omega$ for $600mV \leq V_{IN} < 800mV$
- Chip area $< 1mm^2$
- No off-chip components or external control signals

4.2. Sub-Block Design and Layout

4.2.1. Voltage Controlled Ring Oscillator

A schematic of the voltage controlled ring oscillator is shown in Figure 13.

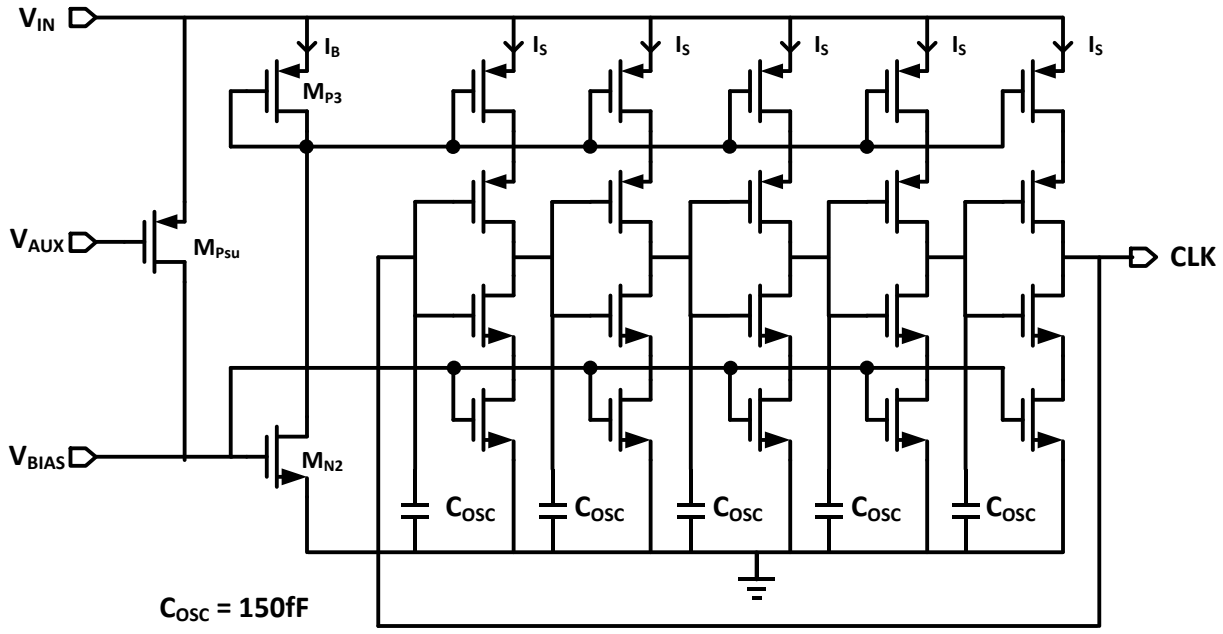

Figure 13. VCO with current starvation and startup transistor

The voltage controlled oscillator is implemented using a five stage current-starved ring oscillator. The oscillation frequency is given in Equation (4.1), where I_S is the current through each stage and N is the number of stages:

$$f_{osc} = \frac{I_s}{2NV_{IN}C_{osc}} \tag{4.1}$$

V_{BIAS} sets the current through the bias transistors M_{P1} and M_{N1} (I_B), which is then mirrored to the inverter stages as I_S. I_S, and therefore the oscillation frequency, is directly proportional to V_{BIAS}. The oscillator is designed such that only nano-amps of current flow in the bias stage to keep power consumption low. The widths of the PMOS and NMOS transistors have a ratio of $W_P/W_N = 2/1$ to achieve equal rise and fall times for the CLK signal. The circuit is

sensitive to the size of C_{osc}. Making C_{osc} too large prevents the oscillator from being able to generate a fast enough frequency when V_{IN} is low (300 – 350mV). However, making it too small will cause the CLK frequency to be too fast when V_{IN} is large (700 – 800mV), even when the current is limited by V_{BIAS}. The size of C_{osc} is selected as 150fF. The simulated CLK frequencies produced at V_{IN} = 300mV, 500mV, and 700mV as V_{BIAS} is varied from 100 – 800mV is shown in Figure 14.

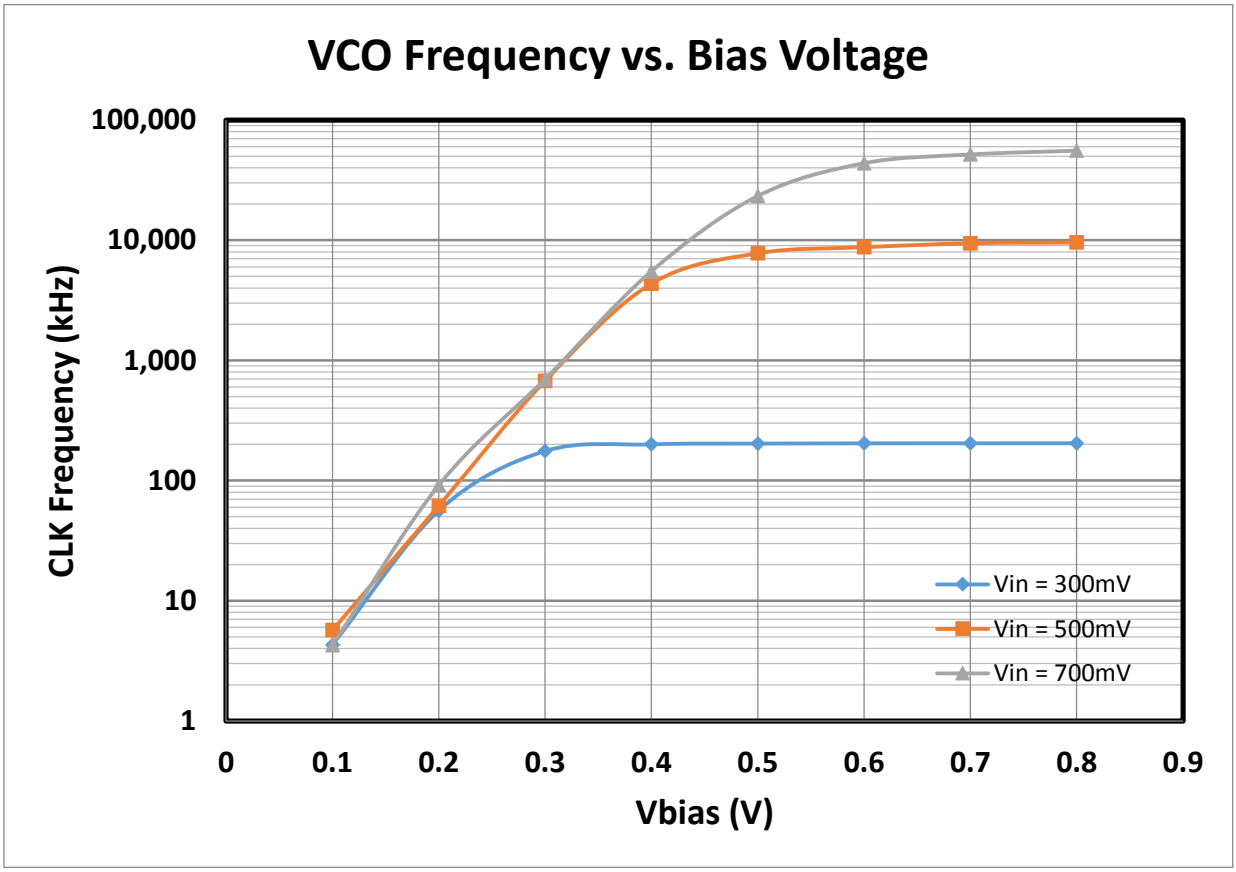

Figure 14. Simulated VCO frequencies over a range of bias voltages

The startup transistor M_{Psu} connects V_{BIAS} to V_{IN} until V_{AUX} raises high enough to cut the transistor off. This way, the VCO runs at full speed when power is initially applied to the circuit, and V_{OUT} reaches steady state much more quickly.

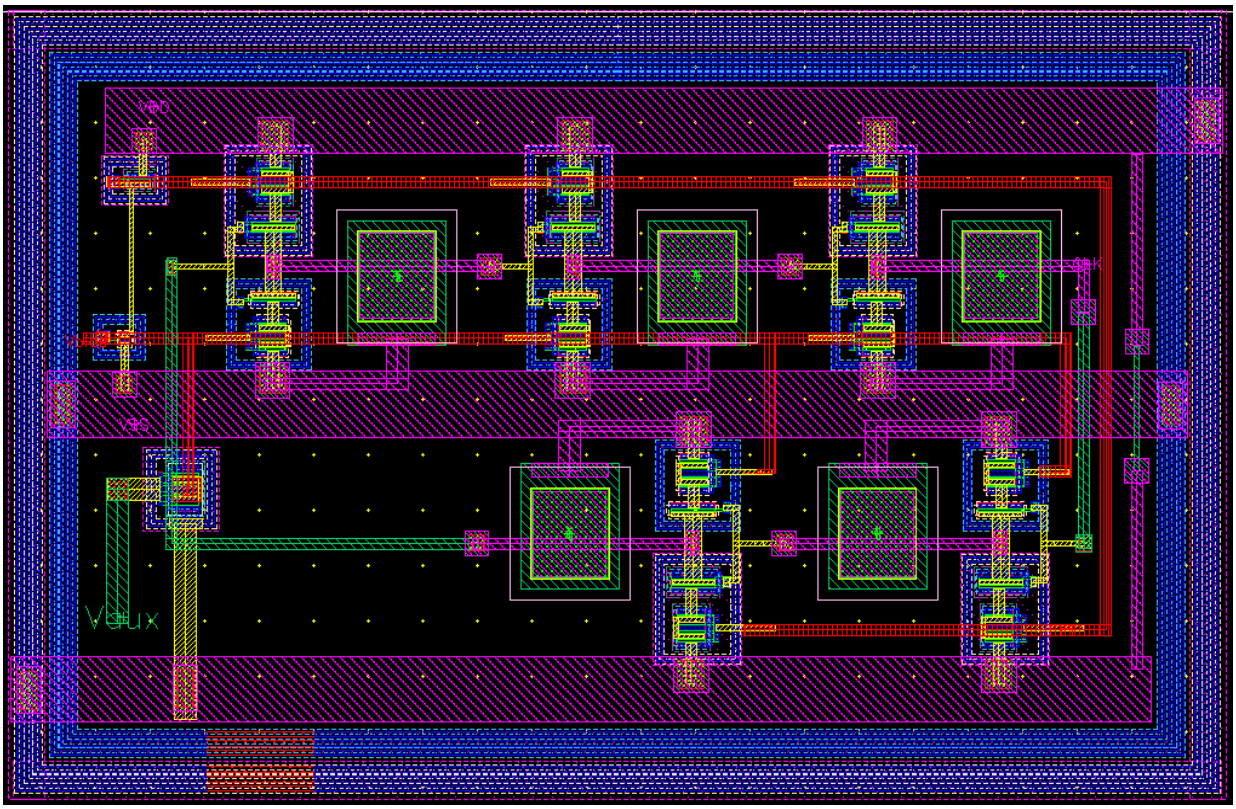

Figure 15. Voltage controlled ring oscillator layout

The layout of the voltage controlled ring oscillator is shown in Figure 15. The last two stages of the oscillator are folded backwards so the layout can be compact. The circuit is surrounded by a triple PTAP guard ring and a triple NTAP guard ring to prevent latchup conditions and to reduce the amount of switching noise that is coupled on to the substrate.

4.2.2. Clock Generator and Pump Drivers

The two-phase clock generator circuit with pump drivers is shown in Figure 16.

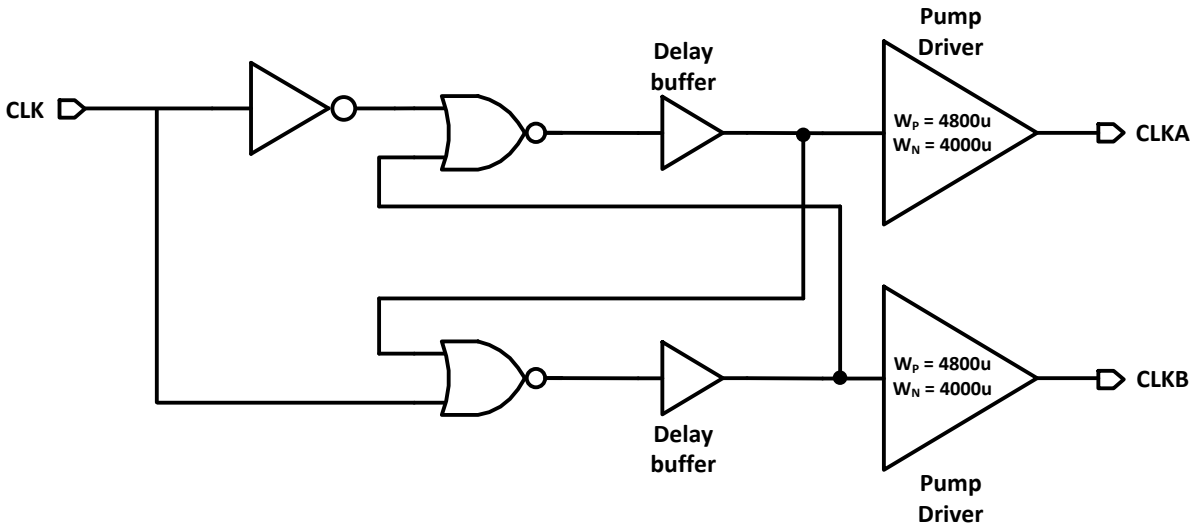

Figure 16. Two-phase clock generator circuit

The two-phase clock generating circuit is implemented using a cross-coupled RS flip-flop circuit with large output buffers to drive the pumping current. The 50% duty cycle CLK input signal is used to generate the two time-aligned, anti-phase CLKA and CLKB signals with non-overlapping dead time. The two phases are laid out symmetrically so that the skew between CLKA and CLKB is minimized.

The delay buffers are implemented as two back-to-back inverters with a delay capacitor attached to the gate of the second inverter. The length of the non-overlapping time can be adjusted by increasing or decreasing the size of the capacitor. The delay must be carefully selected: if the dead time is too short, reverse short-circuit current will occur in the charge pump, but if the dead time is too long, current transfer in each pumping cycle will be limited. The dead time caused by this delay cell is checked over Slow, Nominal, and Fast corner simulations and

over a temperature range of -40°C to 85°C to verify that the dead time is adequate over all temperature and process corners.

The pump driver consists of four back-to-back inverters, where the size of the transistors increases over each stage to optimize drive strength and delay. The first inverter has W_P/W_N = 20µ/15µ, the second inverter has W_P/W_N = 50µ/35µ, the third inverter has W_P/W_N = 600µ/300µ, and the output inverter has W_P/W_N = 4800µ/4000µ. These sizes were selected via iterative simulations to obtain the best square wave output over a range of input voltages.

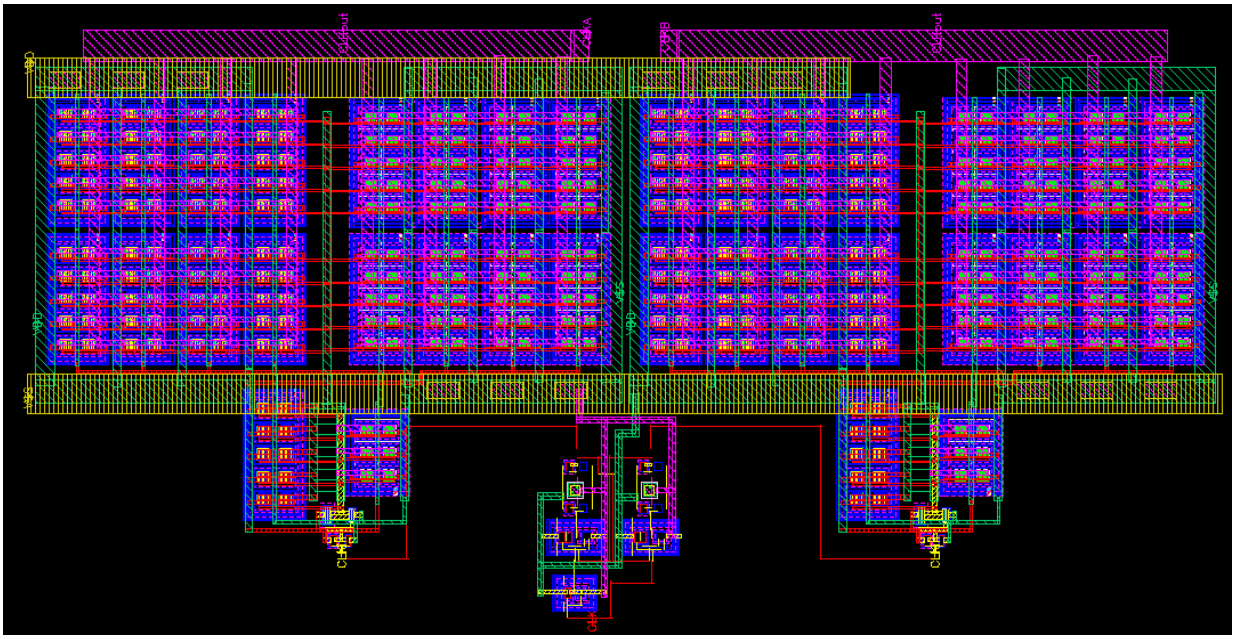

Figure 17. Two-phase clock generator circuit layout

The layout of the clock generator circuit is shown in Figure 17. The PMOS power buffers are laid out in small cells with a gate width of 6µm and 10 fingers for a total width of 60µm per cell, while the NMOS cells have a gate width of 5µm and 10 fingers for a total width of 50µm per cell. Each individual cell has a P-TAP and N-TAP double guard ring, and each group of ten cells has a triple P-TAP and triple N-TAP guard ring. The source and drains are connected through upper metal layers so that wire resistance can be minimized.

4.2.3. Primary Charge Pump Cell

The primary charge pump chain consists of three back-to-back unit charge pump circuits shown in Figure 18.

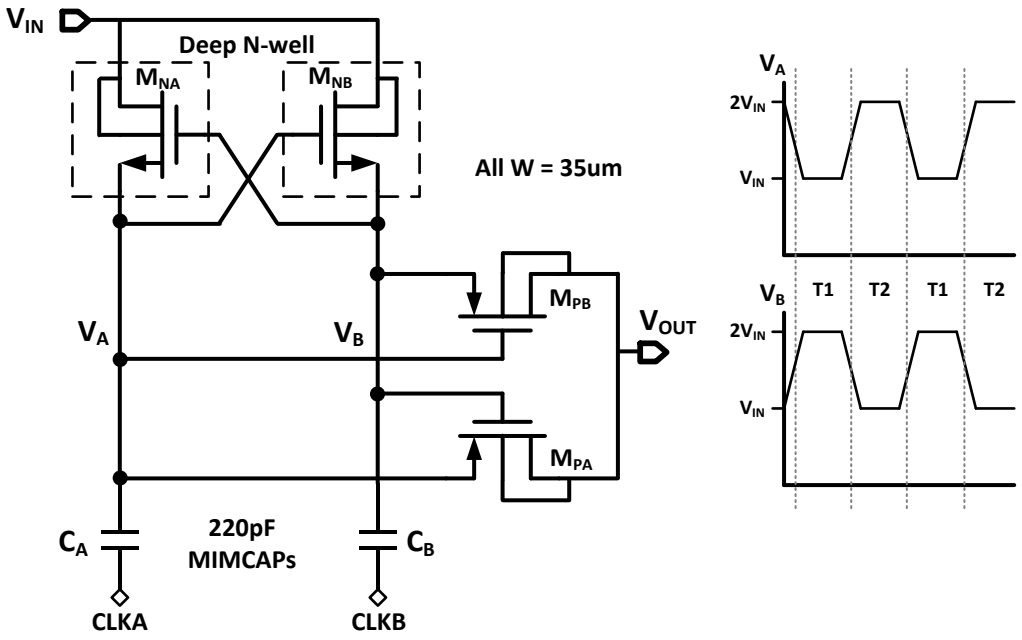

Figure 18. Primary charge pump unit cell

During the charging interval T1, CLKA is 0V, M_{NA} has $V_{GS} = V_{IN}$ and is turned on, and charge flows from V_{IN} into C_A, charging V_A to V_{IN}. M_{PA} has $V_{GS} = 0V$ and is turned off, so charge is unable to flow backwards from V_{OUT} to V_A. During the pumping interval T2, CLKA switches to V_{IN}, M_{NA} has $V_{GS} = 0V$ and is turned off, so charge is unable to flow backwards from V_A to V_{IN}. M_{PA} has $V_{GS} = -V_{IN}$ and is turned on, so charge flows from the boosted V_A node to the output node. Thus, in each switching cycle, charge is pumped from the input to the output. The same process occurs with V_B, but in opposite phase with V_A.

The process described above works well when V_{IN} is greater than the threshold voltage of the transistors. However, as V_{IN} decreases below V_T, the transistors operate in the subthreshold

region, causing significant conduction loss. To reduce the conduction loss and lower the minimum operating input voltage, the transistor bodies can be biased to reduce their threshold voltage, which increases their current drivability and transient response [18]. The NMOS threshold voltage varies with the bulk-source voltage per equation (4.2):

$$V_{TN} = V_{T0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{4.2}$$

where V_{T0} is the unbiased threshold voltage (at $V_{SB} = 0$), γ is the bulk threshold parameter, ϕ_F is the strong inversion surface potential, and V_{SB} is the source-to-bulk voltage of the transistor. To achieve transistor biasing, the bodies of M_{NA} and M_{NB} are tied to their drains in deep N-well. During interval T1, M_{NA} has $V_{SB} = 0$, so $V_{TN} = V_{T0}$ and conductance while M_{NA} is turned on is improved. During interval T2 when M_{NA} is turned off, $V_{SB} = -V_{IN}$, so V_T is lowered, causing the reverse leakage current to be slightly increased. However, the reverse leakage current is negligible even with the decreased V_T. If the NMOS bodies are tied to their source, $V_{SB} = 0$ and $V_{TN} = V_{T0}$ during every phase of the switching cycle. However, during the pumping phase when $V_A = 2V_{IN}$, the body voltage is higher than the drain voltage, and current flows through the forward biased body-to-drain p-n junction, causing significant charge loss. Thus, the bodies are connected to the drain to minimize threshold voltage during the on phase while preventing reverse current from flowing through the body during the off phase.

The size of pumping capacitors C_A and C_B should be as large as possible while still being able to fit in the allocated silicon area. As seen in equations (2.2) and (2.3), the larger the pumping capacitors are, the more load current the charge pump can provide, and the lower the pumping frequency needs to be to maintain the output voltage. Thus, larger pump capacitors will

increase charge pump power throughput and efficiency. For the proposed charge pump, the pumping capacitors are selected to be 220pF each using the design equations in [15].

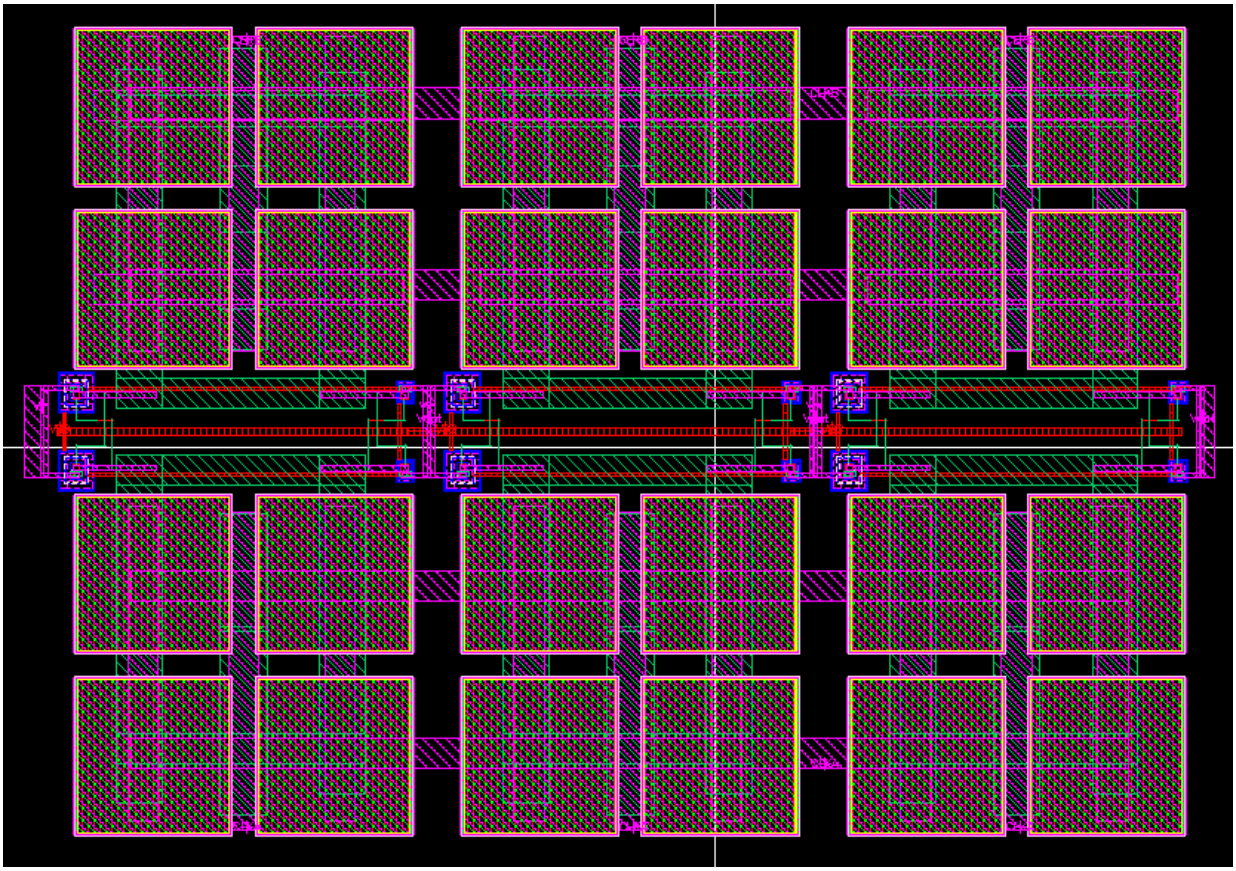

Figure 19. Primary charge pump layout

The layout of the primary charge pump is shown in Figure 19. Each of the 220pF capacitors are implemented using four 50x50µm three-layer MIMCAPs. The 50x50µm dimensioning is chosen to avoid stress DRC errors for large metal planes. The primary charge pump is the largest sub-block, occupying a 786x526µm area in the final layout. V_{OUT} is routed over Metal 3 to the N-TAP guard rings that bias the deep N-wells used for the NMOS transistors.

4.2.4. Auxiliary Charge Pump

The auxiliary charge pump is shown in Figure 20.

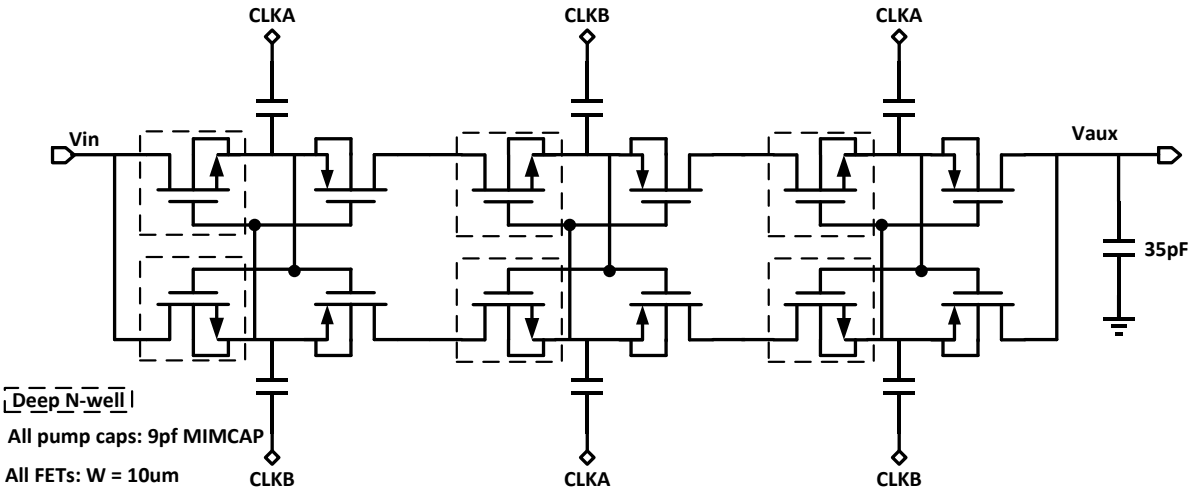

Figure 20. Auxiliary charge pump circuit

The design is based off a previously published Washington State University paper for a quick-startup, low input voltage charge pump [18]. The three-stage, cross-coupled auxiliary charge pump is essentially a smaller version of the primary charge pump. None of the power consumed by this circuit is transferred to the output, so it is designed to be low-power as possible. Component sizes are kept small for low-power operation, because the auxiliary charge pump does not need to provide high throughput power. The NMOS transistors bodies are connected to the drain in deep N-well to improve conduction, as discussed in Section 4.2.3 for the primary charge pump. The output of the charge pump is only loaded by the error amplifier circuit, so the output voltage is typically close to the ideal voltage, $V_{AUX} = 4*V_{IN}$.

This method of using an auxiliary charge pump to generate a high reference voltage was selected over using a bandgap or other type of low reference voltage component as is done in

[14]. The primary reason for this is to prevent having to divide down the output voltage using a power-consuming voltage divider. A resistive voltage divider circuit would add to the load at the output of the primary charge pump, which can see loads as light as 1MΩ. Thus, the voltage divider resistors would need to be much greater than 1MΩ to avoid affecting circuit performance. Also, reference voltage generators can consume microwatts of power, while the auxiliary charge pump consumes power only in the hundreds of nanowatts.

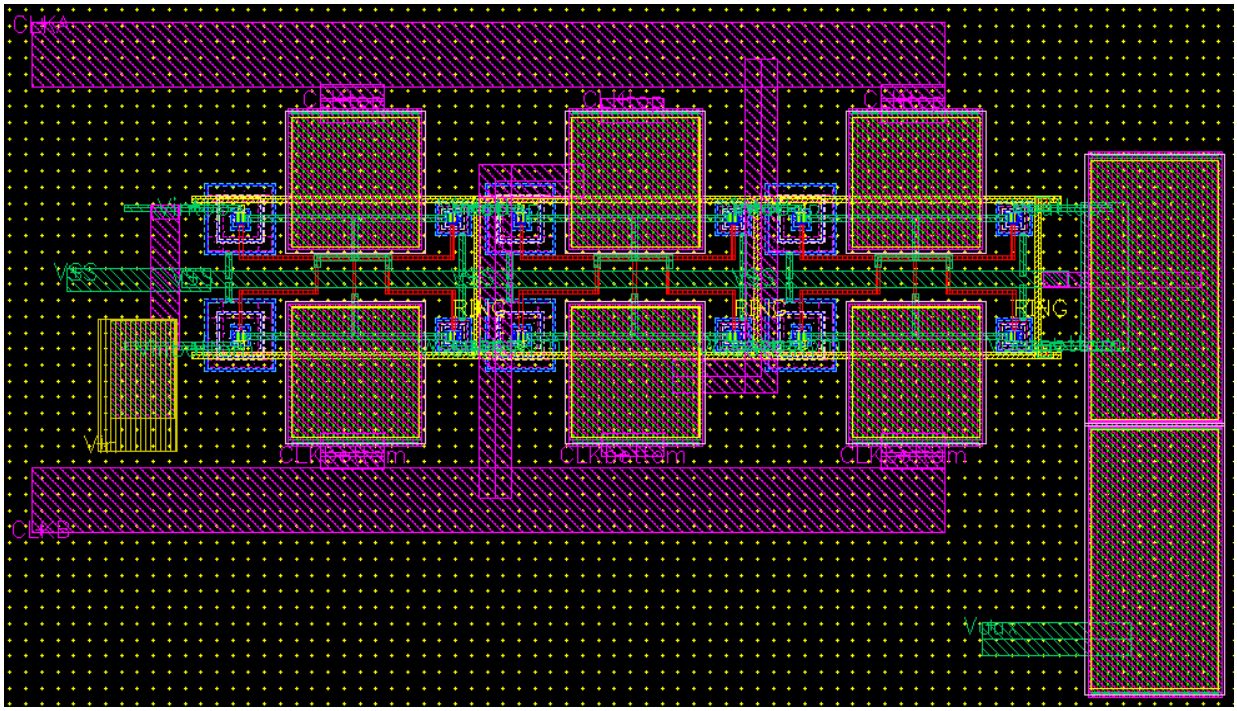

Figure 21. Auxiliary charge pump layout

The layout of the auxiliary charge pump is shown in Figure 21. The flying capacitors are implemented using high-density three-layer MIMCAPs. The output voltage V_{AUX} is routed over Metal 2 to the N-TAP guard rings that bias the deep N-wells used for the NMOS transistors. The CLKA and CLKB Metal 5 wire widths are 20μm wide, a discussion on how this wire width was selected is given in Section 5.1. The positioning of the output capacitor allows this circuit to fit compactly next to the output amplifier circuit in the top-level layout.

4.2.5. Output Error Amplifier

The output error amplifier is shown in Figure 22.

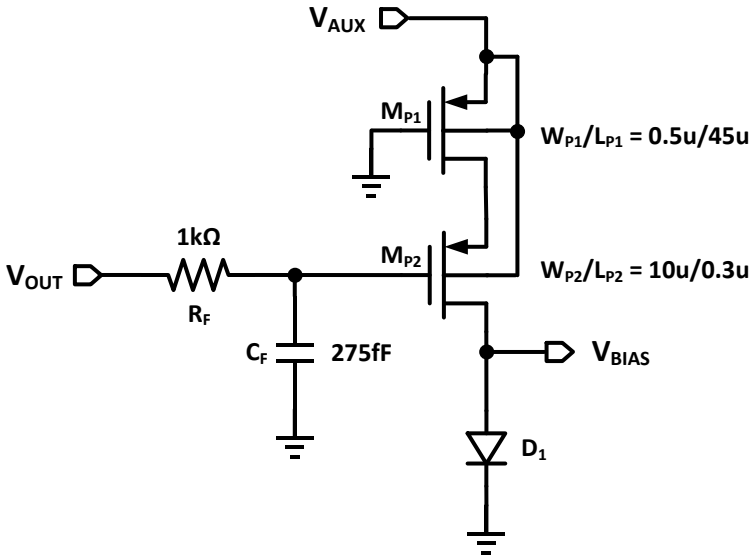

Figure 22. Output error amplifier

The error amplifier is a common-source amplifier with a long-channel PMOS (M_{P1}) used for source degeneration and a diode-connected NMOS (M_{N1}) as the load. The resistance of M_{P1} will vary depending on the source, drain, and body voltages, but in general, it can be assumed to be a relatively large fixed resistance (R_P) for a given bias condition. The diode is used to increase the linearity of the amplifier and to prevent V_{BIAS} from decreasing below a diode drop. The value of V_{BIAS} can be determined by finding the value of I_D in equation (4.3) and substituting it in to equation (4.4), where $v_d = V_{BIAS}$, V_t is the diode thermal voltage, and I_S is the diode saturation current.

$$I_D = \frac{1}{2} K_P' \frac{W_{P2}}{L_{P2}} (V_{SG} - |V_{TP}|)^2 \tag{4.3}$$

$$v_d = nV_t \ln\left(\frac{I_D}{I_S} + 1\right) \tag{4.4}$$

If V_{AUX} is fixed and V_{OUT} decreases, V_{BIAS} increases. As V_{OUT} decreases, more bias current flows through the amplifier, which puts more load on the auxiliary charge pump and decreases V_{AUX} slightly. However, the decrease in V_{AUX} is not large enough to significantly affect the value of V_{BIAS}. R_F and C_F are used to smooth the response of V_{OUT} when the load changes suddenly.

V_{BIAS} is a very critical node in the proposed charge pump circuit, as it directly sets the pumping frequency, and therefore the throughput power, output voltage, and efficiency. Ideally, at V_{IN} = 500mV and when the charge pump output load switches from 1MΩ to 100kΩ to 10kΩ, V_{BIAS} should increase from a minimal (about 150mV) to a medium (about 250mV) to a maximum (about 500mV) voltage. With these bias voltages fed to the VCO, the pumping frequency is 33.6kHz, 369kHz, and 7.78MHz, respectively (see Figure 14). Thus, the ideal load-adaptive performance would be obtained, where frequency is low at light loads and fast at heavy loads.

This is achieved using the P+/N diode D1. The minimal V_{BIAS} voltage occurs when V_{OUT} is near V_{AUX}, causing M_{P2} to be cut off such that very little current flows through the amplifier and V_{BIAS} is set by the diode threshold voltage of D1. The minimal V_{BIAS} voltage should be low enough that the pumping frequency is in the tens of kilohertz range at light loads. If the minimal V_{BIAS} voltage is too high, the pumping frequency becomes higher than it needs to be, and high efficiency operation at light loads is not achieved. The diode voltage, and therefore the minimal V_{BIAS} voltage, can be lowered by increasing the size of the diode, which increases the I_S (saturation current) term in equation (4.4) [19]. As the output load increases, V_{OUT} drops and more current flows through the diode, so V_{BIAS} increases in accordance with Equation (4.4). At

very heavy loads (when V_{OUT} is much lower than V_{AUX}), the increase in current through diode does not cause much increase in diode voltage, so V_{BIAS} saturates.

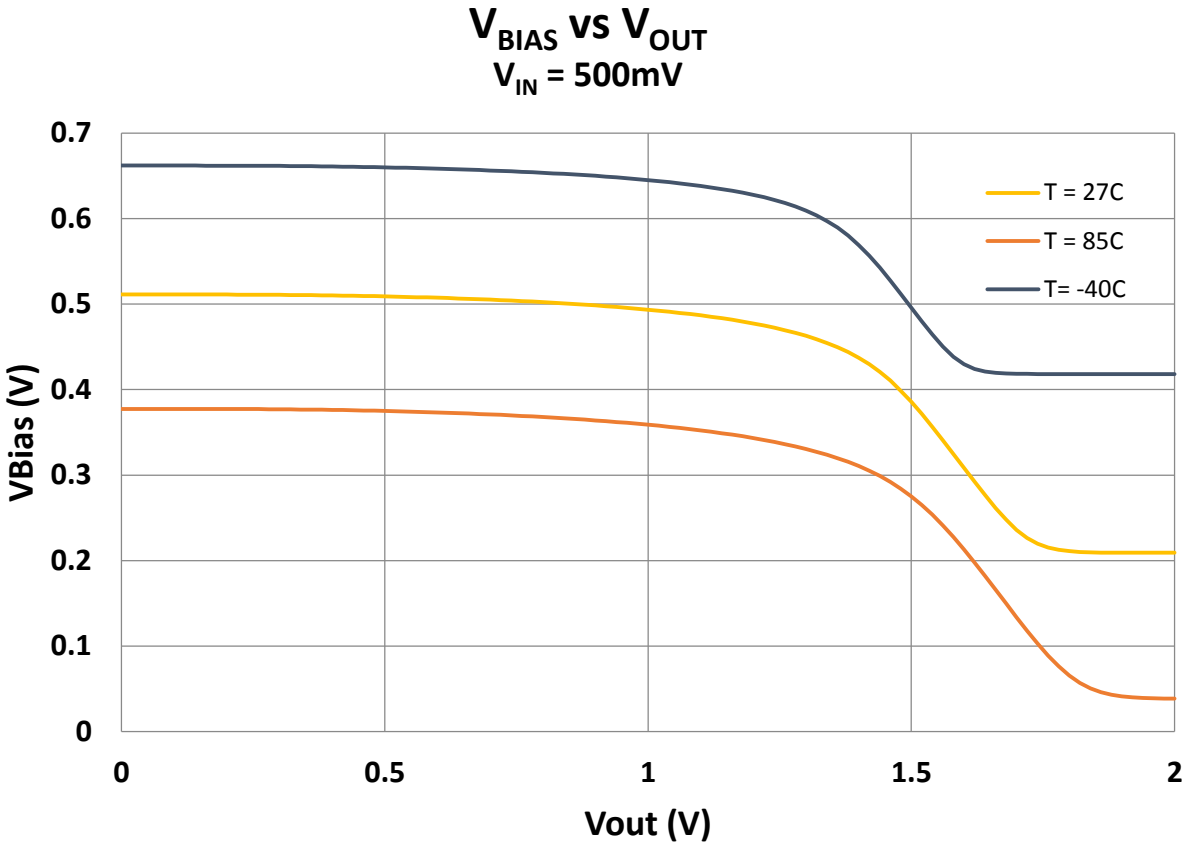

Figure 23. Range of error amplifier output voltages

The simulated value of Vbias when V_{AUX} = 1.9V and V_{OUT} ranges from 0 – 2V (corresponding with an input voltage of V_{IN} = 500mV) is shown in Figure 23. At 27°C, V_{BIAS} ranges from 209.1 – 509.1mV, which corresponds with a pumping frequency range of 61.6kHz – 7.78MHz.

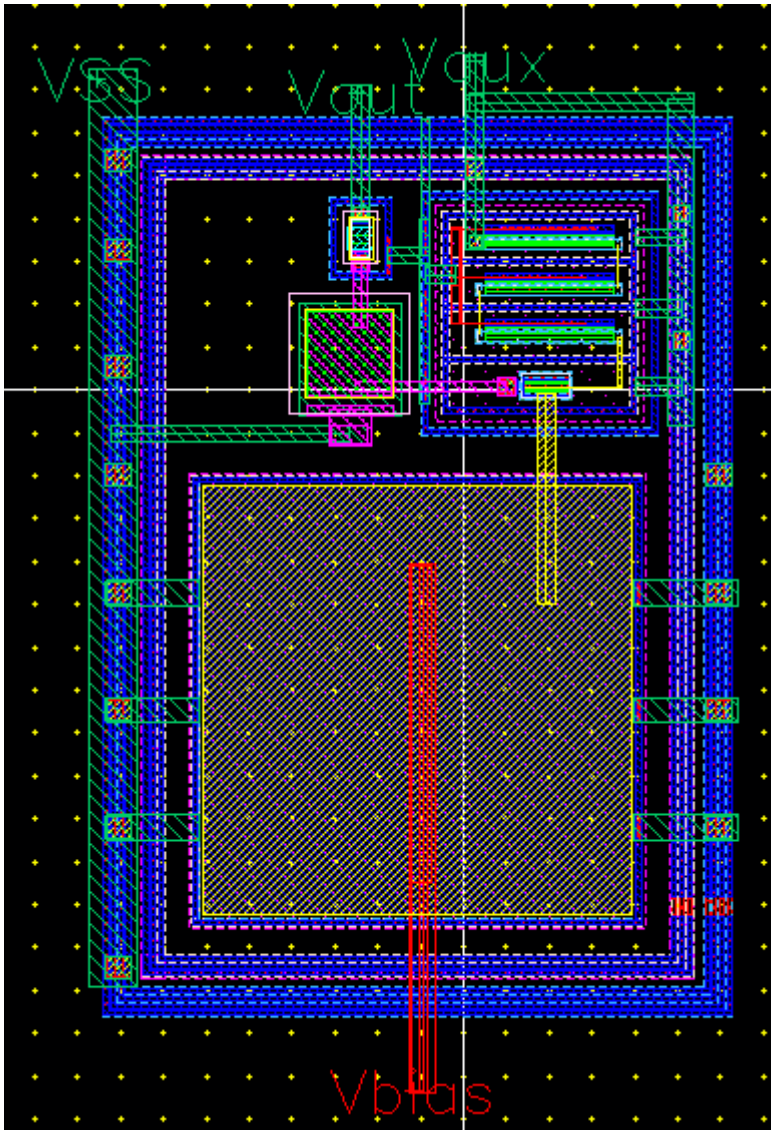

Figure 24. Output error amplifier layout

The layout of the error amplifier is shown in Figure 24. A 50x50µm diode is used for D1. The size of D1 is chosen using incremental simulations to achieve the optimal minimum V_{BIAS} voltage that corresponds to the highest efficiency at light load conditions. Additional P-TAP guard rings are used around the circuit, because it is an analog circuit that must be decoupled from digital switching noise.

5. TOP-LEVEL LAYOUT AND CIRCUIT PERFORMANCE

5.1. Top-level Layout Description

The proposed charge pump topology is implemented in the TowerJazz SBC13HX 0.18μm technology process. The Cadence Layout XL tool is used to create the circuit layout and perform design rule checks (DRC), layout-versus-schematic (LVS), and parasitic extraction (PEX). The top-level layout is shown in Figure 25, where the individual sub-blocks are indicated by red outlines.

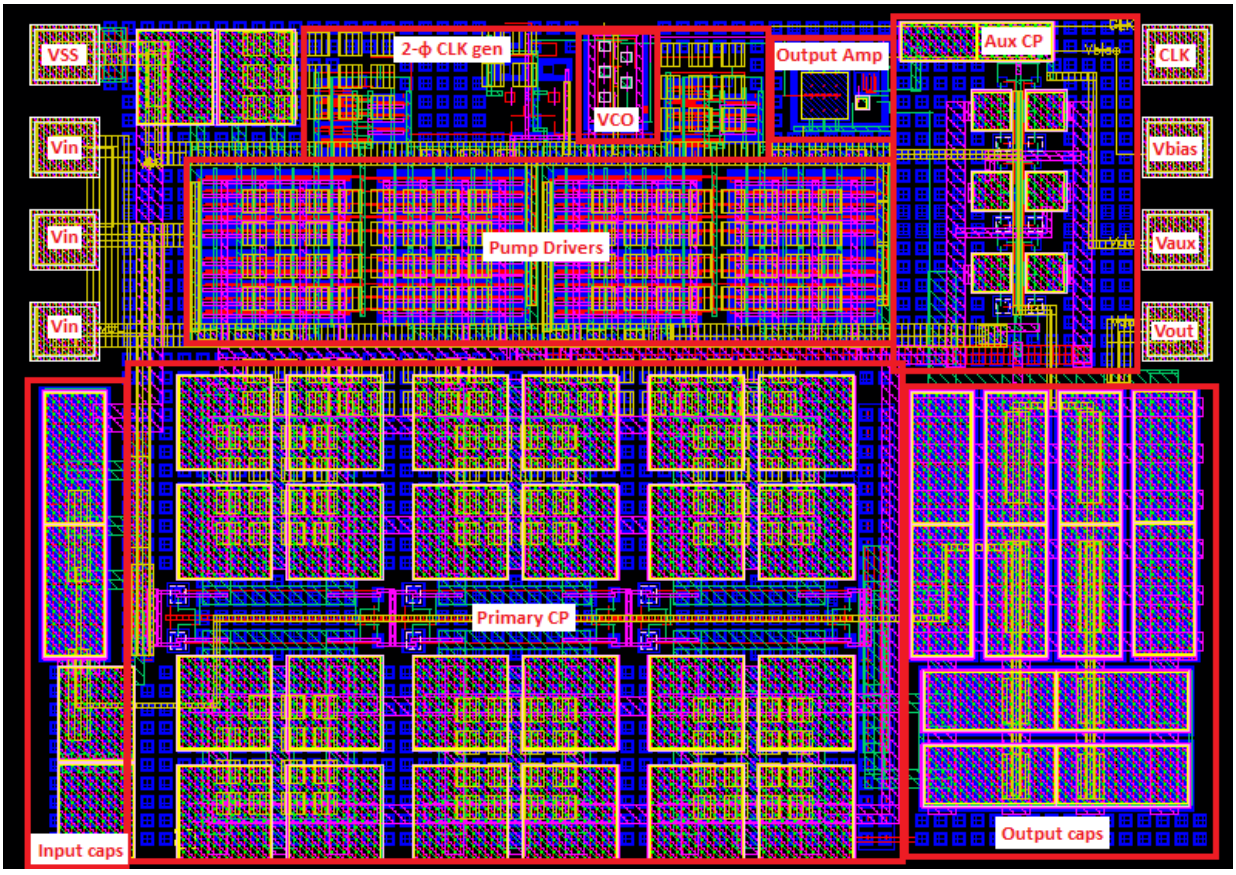

Figure 25. Top-level charge pump layout

The overall layout area (not including the test pads) is 1.066mm^2. The individual sub-blocks are arranged to fit together as compactly as possible. The circuit floor plan minimizes routing between sub-blocks for high-current traces, so resistive wire loss is reduced. V_{IN} and

VSS are distributed throughout the circuit over 25μm wide Metal 6 wire from the test pad. Input capacitance of 400pF is used near the V_{IN} and VSS pads to provide power supply decoupling and bulk charge storage for the circuit. 1100pF of output capacitance is selected using the design equations in [15] to meet the voltage ripple specification ($V_{ripple,pp} < 0.1*V_{OUT}$), even at low pumping frequencies. The output capacitors and one of the input capacitors are implemented using a maximum-density custom capacitor cell, which has a three-layer 63x140μm MIMCAP over an equivalent area of MOSCAPs. The capacitor cell achieves a capacitive density of approximately 8.65fF/μm^2.

The CLKA and CLKB pumping signals are routed from the pump drivers to the primary and auxiliary charge pumps over Metal 5 wire. The resistance and capacitance of the CLKA and CLKB wires directly decrease the charge pumps efficiency, because a large amount of current flows through them and they switch from 0V to V_{IN} every clock cycle. Per the SBC13HX datasheet, Metal 5 wire has a nominal sheet resistance of 18mΩ/square and a capacitance to substrate of 4.8aF/μm^2. The capacitive term is much smaller than the resistive term and does not contribute to energy loss or wire delay, so the capacitive energy loss caused by increasing the wire width is less than the prevented resistive energy loss. Thus, the CLKA and CLKB Metal 5 wire widths are selected as 20μm, which reduces resistive loss without using too much layout area.

The P-substrate is connected to a Metal 1 grid (the blue squares shown in Figure 25), which is connected by interleaved Metal 2 wires (not shown in the figure). The Metal 1 – Metal 2 mesh is connected to VSS at the GND pad, but nowhere else. This way, the P-substrate is tied firmly to ground. The Metal 1 P-TAP guard rings are only connected to VSS through the

distributed Metal 6 VSS wire, not through the substrate grid. With this setup, the amount of switching noise that couples from the substrate to the guard ring protected circuits is reduced.

A PPPG-type test pad is used for the V_{IN} and VSS inputs in the upper left corner, while a PPPP-type test pad is used for the CLK, V_{BIAS}, V_{AUX}, and V_{OUT} connections. The CLK, V_{BIAS}, and V_{AUX} signals provide useful insight to the operating condition of the charge pump, so they are routed to test pads even though they are not external signals. The PPPG test pad is useful for the power inputs, because each P pad has 0.1μF of capacitance to the G pad, so additional power supply decoupling is provided. However, these pads would be unsuitable for the other internal nodes CLK and V_{BIAS}, because 0.1μF would add too much loading to the circuits, so PPPP pads are used.

5.2. Post-layout Simulation Results

The charge pump circuit is simulated over a range of input voltages and a range of load resistors at the output. The simulations are performed using post-layout extractions of coupling capacitances (C+CC), which are obtained using the PEX tool in the Virutoso Layout XL software. To test the load-adaptive functionality, a test bench circuit is used that increases the load by a factor of ten halfway through the simulation by connecting an additional resistor in parallel with the output resistor to decrease the overall load resistance, as shown in Figure 26.

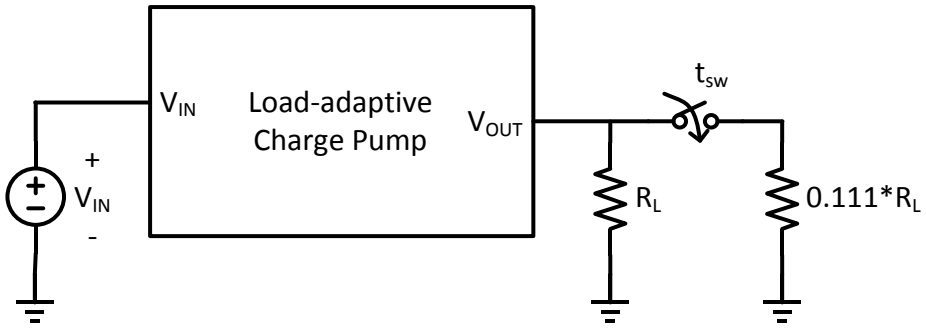

Figure 26. Charge pump simulation test bench

A plot of the load-adaptive response for the case where V_{IN} = 500mV and R_L switches from 500kΩ to 50kΩ is shown in Figure 27.

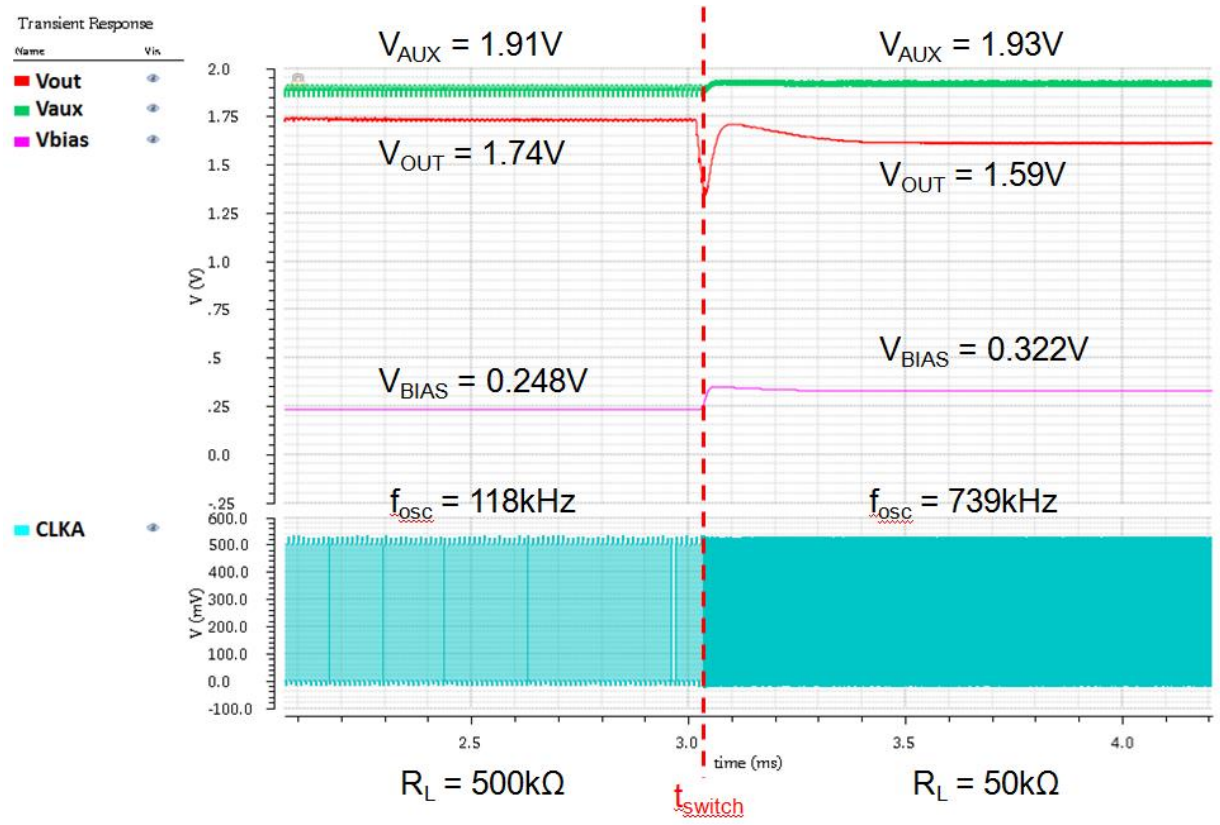

Figure 27. Load-adaptive response

The steady-state voltages when R_L = 500kΩ are V_{AUX} = 1.91V, V_{OUT} = 1.74V, and V_{BIAS} = 248mV, and the pumping frequency is 118kHz. The low pumping frequency allows V_{OUT} to be kept at a high voltage while avoiding excess switching loss. When the load increases to R_L = 50kΩ, the circuit adjusts to a new steady state (the perturbation in the output voltage is caused by the instantaneous increase in load, which is unrealistic for a real-world scenario). At the new steady-state, V_{AUX} = 1.93V, V_{OUT} = 1.59V, and V_{BIAS} = 332mV, while the pumping frequency is 739kHz. The circuit adapts to the change in load and increases the pumping frequency to provide more current to the output, maintaining the output voltage. In both cases, the efficiency remains above 60%. Table 5 shows simulated pumping frequency, output voltage, output ripple, voltage

conversion efficiency, output power, and efficiency for various input voltages as the output load changes.

Table 5. Post-layout simulation results over input voltage and loading conditions

V_{IN} (mV)	R_L (Ω)	Freq. (Hz)	V_{OUT} (V)	$V_{RIPPLE,pp}$ (mV)	VCE	P_{OUT} (μW)	Efficiency
200	5 M	13.62 K	0.3076	0.6202	38.45%	0.01892	16.97%
	20 M	10.22 K	0.6409	0.5059	80.11%	0.02054	27.07%
250	5 M	31.74 K	0.7998	0.6577	79.98%	0.1279	35.39%
	20 M	9.384 K	0.9427	1.346	94.27%	0.4443	37.03%
300	250 K	150.8 K	0.3412	1.243	28.43%	0.4657	16.03%
	500 K	150.2 K	0.5560	3.281	46.33%	0.6183	23.82%
	1 M	122.1 K	0.8396	0.8700	69.97%	0.7049	34.53%
	2 M	52.74 K	1.035	1.540	86.25%	0.5356	49.10%
	4 M	53.02 K	1.120	1.000	93.33%	0.3136	38.50%
400	100 K	1.104 M	1.073	1.276	67.06%	11.52	34.40%
	250 K	337.4 K	1.398	9.480	87.38%	7.818	55.70%
	500 K	186.6 K	1.504	1.800	94.00%	4.524	45.17%
	1 M	157.0 K	1.524	2.909	95.25%	2.323	46.98%
	2 M	133.0 K	1.553	3.430	97.06%	1.206	35.05%
500	10 K	5.861 M	0.9847	2.143	49.24%	97.06	29.21%
	50K	738.7 K	1.588	10.39	79.40%	50.43	61.81%
	100 K	329.7 K	1.627	12.67	81.35%	26.50	64.56%
	200 K	178.4 K	1.676	19.24	83.80%	14.04	64.84%
	500 K	117.6 K	1.791	18.69	89.55%	6.415	60.84%
	1 M	47.49 K	1.748	23.79	87.40%	3.056	60.56%
600	10 K	4.541 M	1.850	6.760	77.08%	342.6	56.87%
	100 K	310.8 K	1.996	19.41	83.17%	39.88	64.46%
	1 M	223.0 K	2.310	20.70	96.25%	5.336	34.21%
700	1 K	24.57 M	0.901	3.992	32.17%	811.3	22.24%
	10 K	3.382 M	2.250	13.80	80.36%	506.8	63.17%
	100 K	326.0 K	2.317	39.42	82.75%	53.73	62.46%
800	1 K	29.63 M	1.354	4.191	42.31%	1833	29.85%
	10 K	2.753 M	2.536	23.73	79.25%	643.1	64.01%
	100 K	2.108 M	3.083	13.09	96.34%	95.05	37.23%

The charge pump achieves good efficiency and output voltage over a range of loading conditions and input voltages, and also has a high throughput power. The minimum operating voltage is 200 mV, where the charge pump is able to achieve at least 50% VCE in a loadless condition. The load condtions for V_{IN} = 200mV and V_{IN} = 250mV are only checked to verify sufficient operation at low input voltages, so they are tested with very light loading. A peak efficiency of 64.84% occurs at V_{IN} = 500mV and R_L = 200kΩ, and above 60% efficiency is maintained over the range of R_L = 50kΩ to 1MΩ. The adaptive pumping frequency works as expected: as the load increases, pumping frequency increases and the voltage conversion efficiency is maintained. Also, the pumping frequency is prevented from being too high at high input voltages as was observed in Section 1.2.

However, several limitations are observed. At extremely light loading conditions, the bias voltage is not able to drop below the diode threshold voltage, so pumping frequency does not go low enough to keep switching loss minimal relative to the output power, and efficiency suffers. Also, at higher input voltages (700mV, 800mV) the pumping frequency remains high due to the nature of the VCO, so efficiency is degraded at light loads. It is still an improvement over a free-running topology, where the pumping frequency would be above 60MHz over all loading conditions at high voltages. At heavy loading conditions and low input voltages, the conduction losses in the FETs limit throughput power and degrade efficiency. However, positive voltage conversion ratios are still achieved at heavy loads.

The model libraries provided with the TowerJazz PDK include statistical models for component parameter variation over process and temperature. These are used to simulate the charge pump at V_{IN} = 500mV over a temperature range of -40°C to 85°C and at Fast-Slow process corners to verify its tolerance to temperature- and process-dependent component

parameters. The output error amplifier sub-block is the most sensitive to temperature changes because it uses a p-n diode to set the minimum bias voltage, and diode threshold voltages are exponentially dependent on temperature. The VCO and clock generator circuits are sensitive to shifting process parameters, because the increased or decreased drive strength caused by process variation heavily affects the timing of the oscillator stages and the dead-time generating blocks. The results are shown in Table 6.

Table 6. Performance over temperature and process corners

Temperature Extremes (-40°C and 85°C)						
Vin (mV)	**Temperature (°C)**	**R_L (Ω)**	**Freq. (Hz)**	**Vout (V)**	**Efficiency**	**Vbias (mV)**
500	-40	100 K	570.9 K	1.625	57.47%	395.2
		1 M	278.4 K	1.946	34.79%	365.7
	85	100 K	247.9 K	1.561	62.74%	215.7
		1 M	24.31 K	1.567	53.17%	117.6

Process Corners (Fast and Slow)						
Vin (mV)	**Corner**	**R_L (Ω)**	**Freq. (Hz)**	**Vout (V)**	**Efficiency**	**Ave. dead-time (ns)**
500	Fast	100 K	652.4 K	1.775	57.86%	14.44
		1 M	222.1 K	1.913	31.7%	24.19
	Slow	100 K	392.5 K	1.353	50.44%	62.23
		1 M	21.15 K	1.525	62.17%	34.41

The diode threshold voltage is higher at -40°C than at room temperature, so V_{BIAS} is higher and pumping frequency is faster. Thus, efficiency is degraded at light loads compared to nominal operation. Similarly, the diode voltage is lower at 85°C, so V_{BIAS} is lower and pumping frequency is slower. Voltage conversion efficiency suffers, but power efficiency remains relatively unchanged. At the Fast process corner, where the critical dimensions of polysilicon gates are smaller and therefore offer less resistance and fast switching speed, the VCO generates a higher pumping frequency and dead-time is decreased. The dead-time remains high enough to

prevent reversion loss, but the higher pumping frequency degrades efficiency at light loading. Conversely, at the slow process corner, the slow switching speed causes decreased pumping frequency and longer dead-time. This causes the output voltage to be lower than nominal, but does not significantly affect efficiency.

5.3. Performance Comparison to State-of-the-Art Charge Pumps

Various state-of-the-art energy harvesting charge pumps have been published that address the challenges of subthreshold operation and switching loss. There are a wide variety of applications for energy harvesting charge pumps, so many different input voltage and output load specifications exist. Charge pumps with similar voltage ranges and performance requirements to the charge pump proposed in this thesis have been selected for comparison. A performance comparison table is presented in Table 7.

Table 7. State-of-the-art performance comparison

Parameter	**Kim [13]**	**Shih [14]**	**Mondal* [20]**	**Abdelaziz* [11]**	**This work***
Process	0.13-µm CMOS	0.13-µm CMOS	0.18-µm CMOS	0.25-µm CMOS	0.18-µm CMOS
Silicon area	0.66mm^2	0.42mm^2	0.48mm^2	N/A	1.07mm^2
External components	6x 10nF pump caps	None	None	None	None
Num. stages	3	3	1	6	3
Pumping capacitors	10nF	25pF	195pF	25pF	220pF
V_{IN} range (V)	0.15 – 0.5	0.27 – 0.48	0.39 – 0.43	0.3 – 0.8	0.2 – 0.8V
V_{OUT} range (V)	0.6 – 2	1.6 (max) 1.4 (reg.)	1.0	3.0 – 9.0	0.5 – 3.2
Optimal load range	0 – 0.61mW	1.4 – 11.3uW	0.6 – 1.1mW	3 – 11uW	0.3uW – 1.8mW
Switch. Freq.	250kHz	800kHz	17 – 23 MHz	1 MHz	10kHz – 30MHz
Max. Efficiency	72.5% @ V_{IN} = 0.45V	65% @ V_{IN} = 0.45V	70% @ V_{IN} = 0.39V	66.39% @ V_{IN} = 0.3V	64.84% @ V_{IN} = 0.5V
Pros	High P_{out}, High efficiency, Low V_{IN}	Regulated V_{OUT}, Low area	High efficiency, Low area, High P_{out}	Wide V_{IN} range, High efficiency at low V_{IN}	Wide V_{IN} range, Wide load range, High P_{out}
Cons	Off-chip components	Low P_{out}, Narrow V_{IN} range	Narrow V_{IN} range	Low P_{out}	High area

* Simulated results only

A comparison of efficiency vs. output load is shown in Figure 27. The proposed charge pump maintains a high efficiency over a wide loading range than [11] or [14].

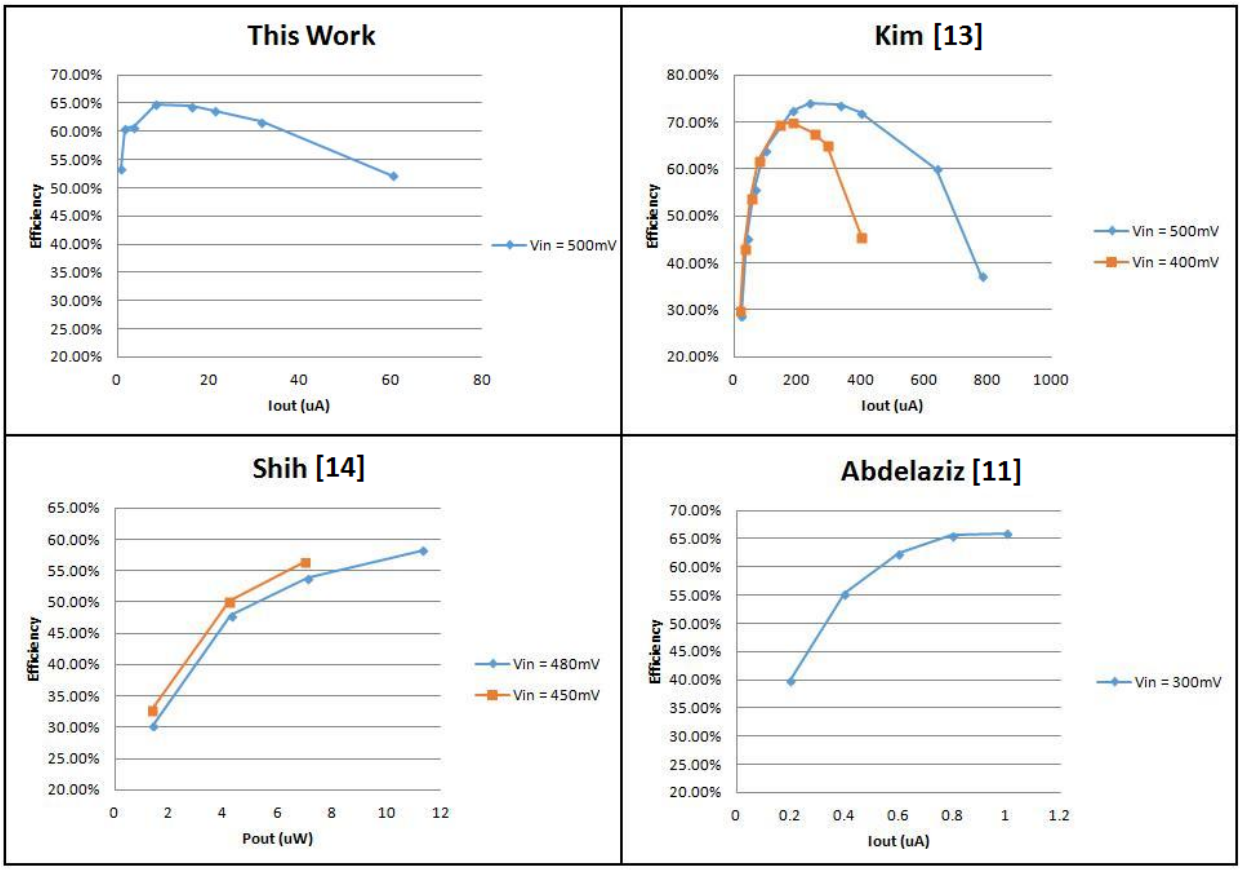

Figure 28. Comparison of efficiency vs. output loading for state-of-the-art

5.4. Conclusion

The proposed load-adaptive charge pump achieves the objective of maintaining high efficiency over a wide range of loading conditions and input voltages by adjusting the rate of the pumping frequency to the size of the output load. It is laid out in a TowerJazz SBC13HX 0.18μm process and simulated using layout extraction data. The circuit has an operating voltage range of 0.2 – 0.8V and responds to changes in load that are two orders of magnitude between heavy and light loading conditions. It achieves peak efficiencies above 60% and improves efficiency at light loads compared to fixed-frequency charge pumps. It is believed to be the first circuit to implement load-adaptive functionality by comparing the output voltage to a self-generated reference voltage and using the resulting bias voltage to control pumping frequency. Its performance over a wide range of conditions makes it a flexible voltage upconverter for a variety of energy harvesting sources and system applications.

While the charge pump has good performance over a wide range of loads, the efficiency suffers at extremely light and extremely heavy loads. Also, as the input voltage increases, the range of loads where peak efficiency can be achieved begins to narrow. With additional investigation, high efficiency performance could potentially be extended further into extremely light loading conditions with the use of a more linear output error amplifier that has an output voltage range of 0 to V_{IN}. Other unique charge pump topologies such as nested and tree topologies [20] may provide room for improved power throughput and efficiency at subthreshold input voltages.

Energy harvesting is becoming a promising option for powering new IoT technologies, WSN nodes, and biometric sensor devices. The need for high-efficiency and compact DC-DC converters that can operate at low voltages to power these devices is growing prominent. Future

research in charge pump technology will be focused on finding techniques to drive down the minimal input voltage and increase throughput power in subthreshold operation. Energy harvesting voltage upconverters such as charge pumps will be a critical component in development and application of microscale wireless technologies.

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